Mullard

Book 1 Part 2

Transistors BFQ10 to OC36 including 2N numbers

September 1974

Mullard technical handbook

Book one

Semiconductor devices

Part two

Transistors BFQ10 to OC36
including 2N numbers

September 1974

Book 1 comprises the following parts—

Part 1 Transistors and accessories
Part 2 Transistors and accessories
Part 3 Diodes, photodiodes and phototransistors
Part 4 Rectifier diodes, rectifier diode stacks, medium and high-power voltage regulator diodes, transient suppressor diodes
Part 5 Thyristors, thyristor stacks and accessories
Part 6 Digital integrated circuits
Part 7 Linear integrated circuits

Made and printed in England by Wightman & Co., Ltd.

BOOK 1 (Part 2)

SEMICONDUCTOR DEVICES

Transistors
BFQ10 to OC36
(including 2N types)

MULLARD LTD., MULLARD HOUSE, TORRINGTON PLACE,
LONDON, WC1E 7HD

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DATA HANDBOOK SYSTEM

The Mullard data handbook system is made up of three sets of books, each comprising several parts.

The three sets of books, easily identifiable by the colours on their covers, are as follows:

Book 1	(blue)	Semiconductor devices and integrated circuits
Book 2	(orange)	Valves and tubes
Book 3	(green)	Passive components, materials, and assemblies.

Each part is completely reviewed annually; revised and reprinted where necessary. Revisions to previous data are indicated by an arrow in the margin.

The data contained in these books are as accurate and up to date as it is reasonably possible to make them at the time of going to press. It must however be understood that no guarantee can be given here regarding the availability of the various devices or that their specifications may not be changed before the next edition is published.

The devices on which full data are given in these books are those around which we would recommend equipment to be designed. Where appropriate, other types no longer recommended for new equipment designs, but generally available for equipment production are listed separately with abridged data. Data sheets for these types may be obtained on request. Older devices on which data may still be obtained on request are also included in the index of the appropriate part of each book.

Requests for information on the data handbook system and for individual data sheets should be made to

Central Technical Services
Mullard Limited
New Road
Mitcham
Surrey CR4 4XY
Telephone: 01-648 3471 Telex: 22194

Information regarding price and availability of devices must be obtained from our authorised agents or from our representatives.

SELECTION GUIDE

1. SMALL/MEDIUM SIGNAL TRANSISTORS

Germanium types

Type No.	N-P-N	P-N-P	General Purpose	Switching	Low Noise	V_{CE} max (V)			h_{FE} min			P_{tot} max (mW)	Case
						⩾15	⩾30	⩾60	⩽30	<60	⩾60		
AC127	★		★				★			★		340	TO–1
AC128		★	★				★				★	1000	TO–1
AC176	★		★				★			★		700	TO–1
AC187	★		★			★					★	1000	TO–1
AC188		★	★			★					★	1000	TO–1

P-N-P Silicon alloy types

Type No.	General Purpose	Switching	V_{CE} max (V)			h_{FE} min			P_{tot} max (mW)	Case
			⩾15	⩾30	⩾60	⩽30	<60	⩾60		
BCY30	★	★			★	★			250	TO–5
BCY31	★	★			★		★		250	TO–5
BCY32	★	★			★			★	250	TO–5
BCY33	★	★		★		★			250	TO–5
BCY34	★	★		★			★		250	TO–5
BCY38	★	★		★		★			410	TO–5
BCY39	★	★			★	★			410	TO–5
BCY40	★	★		★			★		410	TO–5
BCY54	★	★		★			★		410	TO–5

SMALL/MEDIUM SIGNAL TRANSISTORS (cont.)

N-P-N Silicon planar types

Type No.	General Purpose	Switching	Low Noise	V_{CE} max (V)			f_T (GHz)			P_{tot} max (mW)	Case
				⩾15	⩾30	⩾60	<0·4	<1·0	>1·0		
BC107†	★	★			★		★			300	TO–18
BC108†	★	★		★			★			300	TO–18
BC109†	★		★	★			★			300	TO–18
BC147	★				★		★			300	lock-fit
BC148	★			★			★			300	lock-fit
BC149	★		★	★			★			300	lock-fit
BC547	★				★		★			300	TO–92
BC548	★			★			★			300	TO–92
BC549	★		★	★			★			300	TO–92
BCW31R	★			★			★			200	μ min
BCW32R	★			★			★			200	μ min
BCW33R	★			★			★			200	μ min
BCW71R	★				★		★			200	μ min
BCW72R	★				★		★			200	μ min
BCX19	★	★			★		★			310	μ min
BCX20	★	★		★			★			310	μ min
BCX31	★					★	★			1000	lock-fit
BCX32	★					★	★			1000	lock-fit
BCX33	★				★		★			1000	lock-fit
BCX34	★				★		★			1000	lock-fit
BF180	★		★					★		150	TO–72
BF181	★		★	★				★		150	TO–72
BF194	★		★	★			★			220	lock-fit
BF195	★		★	★			★			220	lock-fit
BF196	★		★	★			★			250	lock-fit
BF197	★			★				★		250	lock-fit
BF200	★		★	★			★			150	TO–72
BF336	★					★	★			3000	TO–39
BF337	★					★	★			3000	TO–39
BF338	★					★	★			3000	TO–39
BF355		★				★	★			3000	TO–39
BF362	★			★				★		120	T pack
BF363	★			★				★		120	T pack
BFR63	★		★	★					★	3500	Capstan
BFR64	★		★	★					★	3500	Capstan
BFR90	★		★	★					★	180	T pack
BFR91	★		★	★					★	180	T pack

†Also available to BS 9365–F112

SMALL/MEDIUM SIGNAL TRANSISTORS (cont.)

N-P-N Silicon planar types (cont.)

Type No.	General Purpose	Switching	Low Noise	V_{CE} max (V)			f_T (GHz)			P_{tot} max (mW)	Case
				⩾15	⩾30	⩾60	<0·4	<1·0	>1·0		
BFR92	★		★	★					★	180	μ min
BFR93	★		★						★	180	μ min
BFS17R	★		★	★					★	200	μ min
BFS20R	★			★				★		200	μ min
BFT24	★		★	‡					★	30	T pack
BFT25	★		★	‡					★	30	μ min
BFW16A	★		★	★					★	1500	TO–39
BFW17A	★			★					★	1500	TO–39
BFW30	★		★	★					★	250	TO–72
BFX84	★	★				★	★			800	TO–5
BFX85	★	★				★	★			800	TO–5
BFX86	★	★			★		★			800	TO–5
BFX89	★		★	★					★	200	TO–72
BFY50†	★	★				★	★			800	TO–5
BFY51†	★	★				★	★			800	TO–5
BFY52†	★	★			★		★			800	TO–5
BFY53	★			★			★			800	TO–5
BFY90	★		★	★					★	200	TO–72
BSS40		★			★		★			360	TO–18
BSS41		★			★		★			360	TO–18
BSV52R		★			★			★		200	μ min
BSW66		★				★	★			800	TO–5
BSW67		★				★	★			800	TO–5
BSW68		★				★	★			800	TO–5
BSX19	★	★			★			★		360	TO–18
BSX20	★	★			★			★		360	TO–18
BSX21	★					★	★			300	TO–18
BSX59		★			★		★			800	TO–5
BSX60		★		★			★			800	TO–5
BSX61		★			★		★			800	TO–5
BSY95A		★		★			★			300	TO–18
2N1613	★	★				★	★			800	TO–5
2N1711	★	★			★		★			800	TO–5
2N2297	★	★			★		★			800	TO–5
2N2369A		★		★				★		360	TO–18
2N3053		★			★		★			800	TO–5

†Also available to BS 9365–F012

‡V_{CEO} max = 5V

SMALL/MEDIUM SIGNAL TRANSISTORS (cont.)

P-N-P Silicon planar types

Type No.	General Purpose	Switching	Low Noise	V_{CE} max (V)			f_T (MHz)			P_{tot} max (mW)	Case
				⩾15	⩾30	⩾60	<200	<400	>400		
BC157	★				★		★			300	lock-fit
BC158	★			★			★			300	lock-fit
BC159	★		★	★			★			300	lock-fit
BC327	★				★		★			625	Plastic
BC328	★			★			★			625	Plastic
BC557	★				★		★			300	TO–92
BC558	★			★			★			300	TO–92
BC559	★		★	★			★			300	TO–92
BCW29R	★		★	★			★			200	μ min
BCW30R	★		★	★			★			200	μ min
BCW69R	★				★		★			200	μ min
BCW70R	★				★		★			200	μ min
BCX17	★	★			★		★			310	μ min
BCX18	★	★		★			★			310	μ min
BCX35	★					★	★			1000	lock-fit
BCX36	★					★	★			1000	lock-fit
BCX37	★				★		★			1000	lock-fit
BCY70†	★	★	★		★			★		350	TO–18
BCY71†	★		★		★			★		350	TO–18
BCY72†	★	★	★	★				★		350	TO–18
BF324	★		★		★				★	250	TO–92
BF450	★		★		★			★		250	TO–92
BF451	★		★		★			★		250	TO–92
BFX29‡	★	★				★	★			600	TO–5
BFX30‡		★				★				600	TO–5
BFX87	★	★			★		★			600	TO–5
BFX88	★	★			★		★			600	TO–5
BSV68		★				★	★			250	TO–18
2N2904	★	★			★			★		600	TO–5
2N2904A	★	★				★		★		600	TO–5
2N2905	★	★			★			★		600	TO–5
2N2905A	★	★				★		★		600	TO–5
2N2906	★	★			★			★		400	TO–18
2N2906A	★	★				★		★		400	TO–18
2N2907	★	★			★			★		400	TO–18
2N2907A	★	★				★		★		400	TO–18

† Also available to BS9365-F009

‡ Also available to BS9365-F010/F011

2. L.F./H.F. POWER TRANSISTORS
Silicon types

Type No.	N-P-N	P-N-P	General Purpose	Switching	H.F.	V_{CE} max (V)		h_{FE} min	P_{tot} max (W)	Case
						⩾35	⩾70	⩾30		
BD131	★		★		★	★		★	15	TO–126
BD132		★	★		★	★		★	15	TO–126
BD133	★		★		★	★		★	15	TO–126
BD135	★		★		★	★		★	6·5	TO–126
BD136		★	★		★	★		★	6·5	TO–126
BD137	★		★		★	★		★	6·6	TO–126
BD138		★	★		★	★		★	6·5	TO–126
BD139	★		★		★		★	★	6·5	TO–126
BD140		★	★		★		★	★	6·5	TO–126
BD181	★		★			★			117	TO–3
BD182	★		★			★			117	TO–3
BD183	★		★				★		117	TO–3
BD184	★		★				★		117	TO–3
BD201	★		★			★		★	55	Plastic
BD202		★	★			★		★	55	Plastic
BD203	★		★			★		★	55	Plastic
BD204		★	★			★		★	55	Plastic
BD232	★		★		★		300V		7	TO–126
BD233	★		★			★			25	TO–126
BD234		★	★			★			25	TO–126
BD235	★		★			★			25	TO–126
BD236		★	★			★			25	TO–126
BD237	★		★				★		25	TO–126
BD238		★	★				★		25	TO–126
BD433	★		★					★	36	TO–126
BD434		★	★					★	36	TO–126
BD435	★		★					★	36	TO–126
BD436		★	★					★	36	TO–126
BD437	★		★			★		★	36	TO–126
BD438		★	★			★		★	36	TO–126
BDX35	★			★	★	★		★	15	TO–126
BDX36	★			★	★	★		★	15	TO–126
BDX37	★			★	★		★	★	15	TO–126
BDY20	★		★	★		★			115	TO–3
BDY38	★		★			★		★	115	TO–3

L.F./H.F. POWER TRANSISTORS (cont.)
Silicon types (cont.)

Type No.	N-P-N	P-N-P	General Purpose	Switching	H.F.	V_{CE} max (V)		h_{FE} min	P_{tot} max (W)	Case
						⩾35	⩾70	⩾30		
BDY90	★		★	★	★		★	★	40	TO–3
BDY91	★		★	★	★		★	★	40	TO–3
BDY92	★		★	★	★	★		★	40	TO–3
BDY93	★		★	★			★		30	TO–3
BDY94	★		★	★			★		30	TO–3
BDY95	★		★	★			★		30	TO–3
BDY96	★		★	★			350V		40	TO–3
BDY97	★		★	★			300V		40	TO–3
BDY98	★		★	★			250V		40	TO–3
BSV64	★			★	★	★		★	5	TO–39
BU126	★		★				750V		30	TO–3
BU133	★		★				750V		30	TO–3
BU204	★		★				1300V		10	TO–3
BU205	★		★				1500V		10	TO–3
BU206	★		★				1700V		10	TO–3
BU207	★		★				1300V		12·5	TO–3
BU208	★		★				1500V		12·5	TO–3
BU209	★		★				1700V		12·5	TO–3
2N3055	★		★			★			115	TO–3
2N3442	★		★				★		117	TO–3
2N4347	★		★				★		100	TO–3

Germanium types

Type No.	N-P-N	P-N-P	General Purpose	Switching	H.F.	V_{CE}max (V)			h_{FE} min	P_{tot}max (W)	Case
						⩾15	⩾30	⩾60	⩾40		
AD149		★	★				★			22·5	TO–3
AD161	★		★			★			★	4	SO–55
AD162		★	★			★			★	6	SO–55
OC28		★	★	★				★		30	TO–3
OC29		★	★	★			★		★	30	TO–3
OC35		★	★	★			★			30	TO–3
OC36		★	★	★				★		30	TO–3

3. R.F. POWER DEVICES
N-P-N Transistors

Type No.	V.H.F.	U.H.F.	V_{CE}max (V)		P_o(C.W.) (W at MHz)				Case
			⩾18	⩾33	175	400	470	1000	
BLX13	★			★	25†				Capstan
BLX14	★			★	50†				Stripline
BLX65	★	★	★		2		2		TO–39
BLX66	★	★	★		3		2·5		Capstan
BLX67	★	★	★		3		3		Capstan
BLX69		★	★				20		Capstan
BLX91		★		★			1·4	1·4	Capstan
BLX92		★		★			3	2.5	Capstan
BLX93		★		★			8	5	Capstan
BLX94		★		★			20		Capstan
BLY33	★			★	2‡				TO–39
BLY34	★		★		3				TO–39
BLY35	★			★	7				TO–60
BLY36	★		★		13				TO–60
BLY53A	★	★	★		7·2		7		Capstan
BLY55	★		★		4				TO–60
BLY83	★			★	7				Capstan
BLY84	★		★		13				Capstan
BLY85	★		★		0·2				Capstan
BLY89A	★		★		25				Capstan
BLY90	★		★		50				Stripline
BLY93A	★			★	25				Capstan
BLY94	★			★	50				Stripline
BLY97	★			★	0·14				Capstan
2N3375	★	★		★	7·5§	3			TO–60
2N3553	★			★	2·5				TO–60
2N3632	★			★	13·5				TO–60
2N3866	★	★		★		1			TO–39
2N4427	★	★	★		1		0·4		TO–39

† At 70MHz ‡ A.M. (Carrier) § At 100MHz

Broad Band U.H.F. Amplifier Modules

Type No.	Frequency range (MHz)	V. supply (V)	Po min at Pdr (W)	(W)
BGY22	380–512	13·5	2·5	0·05
BGY22A	420–480	12·5	2·5	0·05
BGY23	380–512	13·5	7	2·5
BGY23A	420–480	12·5	7	2·5

4. DARLINGTON TRANSISTORS

Type No.	N-P-N	P-N-P	V_{CE} max (V)				h_{FE} min at I_C		P_{tot} max	Case
			45	60	80	100		(A)	(W)	
BCX21	★		★				2000	0·15	3·5	TO–39
BDX42	★		★				1500	0·5	5	TO–126
BDX43	★			★			1500	0·5	5	TO–126
BDX44	★				★		1500	0·5	5	TO–126
BSS50	★		★				1500	0·5	5	TO–39
BSS51	★			★			1500	0·5	5	TO–39
BSS52	★				★		1500	0·5	5	TO–39
BD262		★		★			750	1·5	36	TO–126
BD262A		★			★		750	1·5	36	TO–126
BD262B		★				★	750	1·5	36	TO–126
BD263	★			★			750	1·5	36	TO–126
BD263A	★				★		750	1·5	36	TO–126
BD263B	★					★	750	1·5	36	TO–126
BDX62		★		★			1000	3	90	TO–3
BDX62A		★			★		1000	3	90	TO–3
BDX62B		★				★	1000	3	90	TO–3
BDX63	★			★			1000	3	90	TO–3
BDX63A	★				★		1000	3	90	TO–3
BDX63B	★					★	1000	3	90	TO–3
BDX64		★		★			1000	5	117	TO–3
BDX64A		★			★		1000	5	117	TO–3
BDX64B		★				★	1000	5	117	TO–3
BDX65	★			★			1000	5	117	TO–3
BDX65A	★				★		1000	5	117	TO–3
BDX65B	★					★	1000	5	117	TO–3

5. FIELD-EFFECT TRANSISTORS
(n-channel, depletion)

Type No.	Junction gate	Insulated gate	General purpose	Switching	Low noise	Low 'On' resistance	U.H.F.	V_{DS}max (V)	Case
BF245A	★		★		★			30	TO–92
BF245B	★		★		★			30	TO–92
BF245C	★		★		★			30	TO–92
BFQ10		★	★		★			30	TO–71
BFQ11		★	★		★			30	TO–71
BFQ12		★	★		★			30	TO–71
BFQ13		★	★		★			30	TO–71
BFQ14		★	★		★			30	TO–71
BFQ15		★	★		★			30	TO–71
BFQ16		★	★		★			30	TO–71
BFR29		★	★		★			30	TO–72
BFR30	★		★					25	μ min
BFR31	★		★					25	μ min
BFS28		★	★		★		★	20	TO–72
BFW10	★		★		★			30	TO–72
BFW11	★		★		★			30	TO–72
BFW61	★		★					25	TO–72
BSV78	★			★		★		40	TO–18
BSV79	★			★		★		40	TO–18
BSV80	★			★		★		40	TO–18
BSV81		★		★		★		30	TO–72
2N3823	★		★		★			30	TO–72
2N3966	★			★				30	TO–72
2N4091	★			★		★		40	TO–18
2N4092	★			★		★		40	TO–18
2N4093	★			★				40	TO–18
2N4391	★			★		★		40	TO–18
2N4392	★			★		★		40	TO–18
2N4393	★			★				40	TO–18
2N4856	★			★		★		40	TO–18
2N4857	★			★		★		40	TO–18
2N4858	★			★		★		40	TO–18
2N4859	★			★		★		30	TO–18
2N4860	★			★		★		30	TO–18
2N4861	★			★		★		30	TO–18

6. MICROMINIATURE TRANSISTORS

Type No.	N-P-N	P-N-P	General Purpose	Switching	Low Noise	V_{CE}max (V)			f_T (MHz)			P_{tot}max (mW)
						⩾15	⩾30	⩾60	<200	<500	>1000	
BCW29R		★	★		★	★			★			200
BCW30R		★	★		★	★			★			200
BCW31R	★		★			★				★		200
BCW32R	★		★			★				★		200
BCW33R	★		★			★				★		200
BCW69R		★	★				★		★			200
BCW70R		★	★				★		★			200
BCW71R	★		★				★			★		200
BCW72R	★		★				★			★		200
BCX17		★	★	★			★		★			310
BCX18		★	★	★		★			★			310
BCX19	★		★	★			★		★			310
BCX20	★		★	★		★			★			310
BFR30†			★			★						200
BFR31†			★			★						200
BFR92	★		★		★	★					★	180
BFR93	★		★		★						★	180
BFS17R	★		★		★	★					★	200
BFS20R	★		★			★				★		200
BFT25	★		★		★	‡					★	30
BSV52R	★			★		★				★		200

†Field effect transistors
‡V_{CEO} max = 5V

GENERAL SECTION A

INDEX

TYPE NOMENCLATURE

Section 1

Mullard semiconductor devices are registered by Pro Electron.
The type nomenclature of a discrete device or, in certain cases, of a range of devices, consists of two letters followed by a serial number. The serial number may consist of three figures or of one letter and two figures depending on the main application of the device.

The first letter indicates the semiconductor material used:

A — germanium
B — silicon
C — compound materials such as gallium arsenide
D — compound materials such as indium antimonide
R — compound materials such as cadmium sulphide

The second letter indicates the general function of the device:

A — detection diode, high speed diode, mixer diode.
B — variable capacitance diode
C — transistor for a.f. applications (not power types)
D — power transistor for a.f. applications
E — tunnel diode
F — transistor for r.f. applications (not power types)
G — multiple of dissimilar devices; miscellaneous devices
L — power transistor for r.f. applications
N — photo-coupler
P — radiation sensitive device such as photodiode, phototransistor, photo-conductive cell, or radiation detector diode
Q — radiation generating device such as light-emitting diode
R — controlling and switching device (e.g. thyristor) having a specified break-down characteristic (not power types)
S — transistor for switching applications (not power types)
T — controlling and switching power device (e.g. thyristor) having a specified breakdown characteristic
U — power transistor for switching applications
X — multiplier diode such as varactor or step recovery diode
Y — rectifier diode, booster diode, efficiency diode
Z — voltage reference or voltage regulator diode, transient suppressor diode

The remainder of the type number is a **serial number** indicating a particular design or development and is in one of the following two groups:

(a) Devices intended primarily for use in consumer applications (radio and television receivers, audio amplifiers, tape recorders, domestic appliances, etc.).
The serial number consists of three figures.

(b) Devices intended mainly for applications other than (a), e.g. industrial, professional and transmitting equipments.
The serial number consists of one letter (Z, Y, X, W, etc.) followed by two figures.

Range Numbers

Where there is a range of variants of a basic type of rectifier diode, thyristor or voltage regulator diode the type number as defined above is often used to identify the range; further letters and figures are added after a hyphen to identify individual types within the range. These additions are as follows:

Rectifier Diodes and Thyristors

The group of figures indicates the rated repetitive peak reverse voltage, V_{RRM}, or the rated repetitive peak off-state voltage, V_{DRM}, whichever value is lower, in volts for each type.

The final letter R is used to denote a reverse polarity version (stud anode) where applicable. The normal polarity version (stud cathode) has no special final letter.

Voltage Regulator Diodes, Transient Suppression Diodes

The first letter indicates the nominal percentage tolerance in the operating voltage V_Z.

A — ±1%
B — ±2%
C — ±5%
D — ±10%
E — ±15%

The letter is omitted on transient suppressor diodes.

The group of figures indicates the typical operating voltage V_Z for each type at the nominal operating current I_Z rating of the range. For transient suppressor diodes the figure indicates the maximum recommended standoff voltage V_R.

The letter V is used to denote a decimal sign.

The final letter R is used to denote a reverse polarity version (stud anode) where applicable. The normal polarity version (stud cathode) has no special final letter.

Examples:

BF362	Silicon r.f. transistor intended primarily for 'consumer' applications.
ACY17	Germanium a.f. transistor primarily for 'industrial' applications.
BTW24-800R	Silicon thyristor for 'industrial' applications. In BTW24 range with 800V maximum repetitive peak voltage, reverse polarity, stud connected to anode.
BZY88-C5V6	Silicon voltage regulator diode for 'industrial' applications. In BZY88 range with 5·6V operating voltage ±5% tolerance.
RPY71	Photoconductive cell for 'industrial' applications.

OLD SYSTEM

Some earlier semiconductor diodes and transistors have type numbers consisting of two or three letters followed by a group of one, two or three figures.

The first letter is always 'O', indicating a semiconductor device.

The second (and third) letter(s) indicate the general class of device:

A — diode or rectifier
AP — photodiode
AZ — voltage regulator diode
C — transistor
CP — phototransistor

The group of figures is a serial number indicating a particular design or development.

Section II

LIST OF SYMBOLS FOR SEMICONDUCTOR DEVICES

These symbols are based on British Standard Specification No. 3363: "Letter Symbols for Semiconductor Devices." A full description of the system is contained in this publication.

QUANTITY SYMBOLS

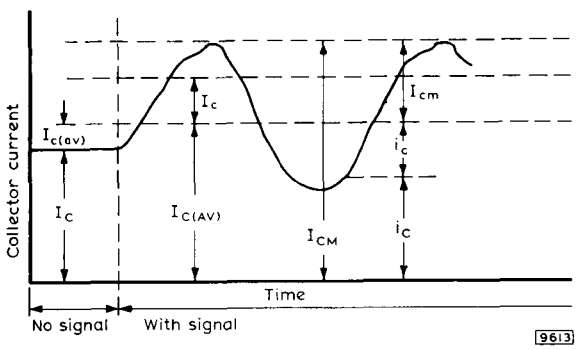
V	Voltage
I	Current
P	Power

ii, v, p with subscripts e, b, c — instantaneous value of the varying component.

i, v, p with subscripts E, B, C — instantaneous total value.

I, V, P with subscripts e, b, c — the r.m.s. value of the varying component, or with appropriate additional subscript the peak (m) or average (d.c.) (av) value of the varying component.

I, V, P with subscripts E, B, C — the no-signal (d.c.) value or, with the appropriate additional subscripts the total average value (AV) with signal or the total peak value (M).



Examples:

I_E	d.c. emitter current no signal.
I_e	r.m.s. value of varying component of emitter current.
i_e	Instantaneous value of varying component of emitter current.
i_E	Instantaneous value of total emitter current.
$I_{E(AV)}$	Average (d.c.) value of total emitter current with signal applied.
$I_{e(av)}$	Average (d.c.) value of the varying component of the emitter current.
I_{em}	Peak value of the varying component of the emitter current.
I_{EM}	Peak value of the total emitter current.

Subscripts for quantity sumbols

A, a	Anode terminal	I, i	Input
AV, av	Average	J, j	Junction
B, b	Base terminal	K, k	Cathode terminal
BO	Breakover	M, m	Peak value
BR	Breakdown	O, o	Open-circuit, output
C, c	Collector terminal, conversion, capacitive	OV	Average value of overload
		R, r	Resistive, reverse, repetitive
D, d	Delay, Off-state (i.e. non trigger) drain terminal	S, s	Short-circuit, series, shield, source
		T, t	On-state (i.e. triggered)
E, e	Emitter terminal	W, w	Working
F, f	Forward	X, x	Specified circuit, reactive
G, g	Gate terminal	Z, z	Reference or regulator (i.e. Zener), impedance
H, h	Holding		

The letter O is used with three terminal devices as a third subscript only to denote that the terminal not indicated in the subscript is open-circuited.

The letter S is also used with three terminal devices as a third subscript to denote that the terminal not indicated in the subscript is shorted to the reference terminal.

Sequence of subscripts

The first subscript denotes the terminal at which the current or terminal voltage is measured.

The second subscript denotes the reference terminal or circuit mode that the current or terminal voltage is measured.

Where the reference terminal or circuit is understood the second subscript may be omitted where its use is not required to preserve the meaning of the symbol.

The supply voltage shall be indicated by repeating the terminal subscript. The reference terminal may then be designated by the third subscript.

Examples V_{EE}, V_{CC}, V_{BB}, V_{EEB}

In devices having more than one terminal of the same type, the terminal subscripts shall be modified by adding a number following the subscript and on the same line.

Example B2

In multiple unit devices the terminal subscripts shall be modified by a number preceding the terminal subscript.

Example 2B

Where ambiguity might arise the complete terminal designations shall be separated by hyphens or commas.

Example $V_{1C1-2C1}$

the voltage at the first collector of the first unit referred to the voltage at the first collector of the second unit.
The first subscript in the matrix notation shall identify the element of the four pole matrix.

i	input
o	output
f	forward transfer
r	reverse transfer

A second subscript may be used to identify the circuit configuration.

e	common emitter
b	common base
c	common collector

Example $V_{ie} = h_{ie}.\ I_{ie} + h_{re}.V_{oe}$

When the common terminal is understood the second subscript may be omitted.

Static value of parameters shall be indicated by the upper case (capital) subscripts.

Example h_{IE}, h_{IB}

The four pole matrix parameters of the device are represented by lower case symbols with the appropriate subscripts

h_{ib}

The four pole matrix parameters of external circuits and of circuits in which the device forms only a small part are represented by upper case symbols with the appropriate subscripts.

H_i, Z_o

Symbols for the components of small-signal equivalent circuits used to represent devices are qualified by lower case symbols.

r_b, r_e, $r_{bb'}$

ELECTRICAL PARAMETERS

	Device	Associated circuit
Resistance	r	R
Reactance	x	X
Impedance	z	Z
Admittance	y	Y
Conductance	g	G
Susceptance	b	B
Mutual inductance	m	M
Inductance	l	L
Capacitance	c	C
Distortion	D	
Frequency limits	f max.	
	f min.	
Bandwidth	Δf	
Bandwidth (for associated circuits)		B
Noise factor		N

List of Symbols for Semiconductor Devices

C_d	diode capacitance (reverse bias)
C_f	diode capacitance (forward bias)
C_{ib}	transistor input capacitance (grounded base)
C_{ie}	transistor input capacitance (grounded emitter)
C_j	junction capacitance (of the intrinsic diode)
C_{min}	diode capacitance (at breakdown voltage)
C_o	diode capacitance (zero bias)
C_{ob}	transistor output capacitance (grounded base)
C_{oe}	transistor output capacitance (grounded emitter)
C_p	parasitic (parallel) capacitance
C_s	stray capacitance
C_{Te}	capacitance of the emitter depletion layer
C_{Te}	capacitance of the collector depletion layer
f_{co}	varactor diode cut-off frequency
f_{hfb}, f_{hfe}	transistor cut-off frequency (the frequency at which the parameter indicated by the subscript is 0.7 times its low frequency value)
f_l	frequency of unity current transfer ratio modulus
f_{max}	maximum frequency of oscillations
f_r	tunnel diode resistive cut-off frequency
f_T	transition frequency (common emitter gain-bandwidth product)
g_j	tunnel diode negative conductance (of the intrinsic diode)
g_p	small signal power gain
G_p	large signal power gain
h_{IB}, h_{IE}, h_{IC}	the static value of the input resistance with the output voltage held constant
h_{ib} (h_{11}), h_{ie} (h_{11}), h_{ic}	The small-signal value of the input impedance with the output short-circuited to alternating current
h_{RB}, h_{RE}, h_{RC}	The static value of the reverse voltage transfer ratio with the input current held constant
h_{rb} (h_{12}), h_{re} (h_{12}), h_{rc}	The small-signal value of the reverse voltage transfer ratio with the output voltage held constant
h_{FB}, h_{FE}, h_{FC}	The static value of the forward current transfer ratio with the output voltage held constant
h_{fb} (h_{21}), h_{fe} (h_{21}), h_{fc}	The small-signal forward current transfer ratio with the output short-circuited to alternating current
h_{OB}, h_{OE}, h_{OC}	The static value of the output conductance with the input current held constant
h_{ob} (h_{22}), h_{oe} (h_{22}), h_{oc}	The small-signal value of the output admittance with the input open-circuited to alternating current
$h_{FE(sat)}$	transient forward current transfer ratio in saturation
h_{FEL}	inherent forward current transfer ratio $= \frac{I_C - I_{CBO}}{I_B + I_{CBO}}$

I_B , I_C , I_E	total d.c. current
$I_{B(AV)}$ $I_{C(AV)}$ $I_{E(AV)}$	average (d.c.) value of total current
I_{BBX}	base current (with both junctions reverse biased)
I_{BEX} , I_{CEX}	base (respectively collector) cut off current in a specified circuit
I_{BM}, I_{CM} , I_{EM}	peak value of total current
I_b , I_c , I_e	r.m.s. value of varying component of current
I_{bm} , I_{cm} , I_{em}	peak value of varying component of current
i_B , i_C , i_E	instantaneous total value of current
i_b , i_c , i_e	instantaneous value of varying component of current
$I_{(BO)}$	thyristor breakover current (d.c.)
I_{CBO}	collector cut-off current (emitter open-circuited)
I_{CBS} , I_{CES}	collector cut-off current (emitter short-circuited to base)
I_{CBX}	collector current with both junctions reverse biased with respect to base
I_{CEO}	collector cut-off current (base open-circuit)
I_{CER}	collector cut-off current (with specified resistance between base and emitter)
I_D	thyristor continuous (d.c.) off-state current, field effect transistor drain current
I_{EBO}	emitter cut-off current (collector open-circuit)
I_{EBX}	emitter current with both junctions reverse biased with respect to base
I_F	D.C. forward current
i_F	instantaneous forward current
$I_{F(AV)}$	average forward current
I_{FG}	thyristor forward gate current
I_{FGM}	thyristor peak forward gate current
I_{FM}	peak forward current
$I_{F(OV)}$, I_{FOM}	overload mean forward current
I_{FRM}	repetitive peak forward current
I_{FSM}	surge (non-repetitive) forward current
I_{GD}	thyristor gate non-trigger current
I_{GT}	thyristor gate trigger current
I_{GQ}	thyristor gate turn-off current
I_H	thyristor holding current (d.c.)
I_L	thyristor latching current
I_O	average output current
I_{ORM}	repetitive peak output current
I_P	tunnel diode peak point current
I_p/I_V	tunnel diode peak to valley point current ratio
I_R	continuous (d.c.) reverse leakage current
i_R	instantaneous reverse leakage current
I_{RG}	thyristor reverse gate current
I_{RRM}	repetitive peak reverse current
I_{RSM}	non-repetitive peak reverse current
I_S	source current
I_T	thyristor continuous (d.c.) on-state current
$I_{T(OV)}$	thyristor overload mean on-state current
$I_{T(AV)}$	thyristor average on-state current
I_{TRM}	thyristor repetitive peak on-state current
I_{TSM}	thyristor non-repetitive peak on-state current

I_V	tunnel diode valley point current
I_Z	voltage regulator (zener) diode continuous (d.c.) operating current
$I_{Z(AV)}$	voltage regulator (zener) diode average operating current
I_{ZM}	voltage regulator (zener) diode peak current
L_c	conversion loss
L_s	series inductance
N_f	flicker noise
N_{if}	noise figure at intermediate frequency
N_o	overall noise figure
N_r	noise temperature ratio
P_G	thyristor average gate power
P_{GM}	thyristor peak gate power
P_{tot}	total power dissipated within the device
Q_s	recovered (stored) charge
$r_{bb'}$	extrinsic base resistance
R_S	source resistance
r_S	series resistance
R_{th}	thermal resistance
r_Z	voltage regulator (zener) diode differential resistance
S_{ts}	tangential signal sensitivity
S_Z	voltage regulator (zener) diode temperature coefficient of the operating voltage
T_{amb}	ambient temperature
T_{case}	case temperature
T_j	junction temperature
T_{mb}	mounting base temperature
T_{stg}	storage temperature
t_d	delay time
t_f	fall time
t_{fr}	forward recovery time
t_{gt}	thyristor gate controlled turn-on time
t_{gq}	thyristor gate controlled turn-off time
t_p	pulse duration
t_q	thyristor circuit-commutated turn-off time
t_{on}	turn-on time
t_{off}	turn-off time
t_r	rise time
t_{rr}	reverse recovery time
t_s	storage time
θ_h	thermal resistance of heat sink
θ_i	contact thermal resistance
θ_{j-amb}	thermal resistance junction to ambient
θ_{j-case}	thermal resistance junction to case
θ_{j-mb}	thermal resistance junction to mounting base
τ_C	collector time coefficient of a switching transistor
τ_S	carrier storage time coefficient of a switching transistor
τ_F	fall time factor
τ_R	rise time factor

$V_{BE(sat)}$	base-emitter saturation voltage
$V_{(BO)}$	thyristor breakover voltage
$V_{(BR)}$	breakdown voltage
$V_{(BR)CBO}$	breakdown voltage collector to base (emitter open-circuited)
$V_{(BR)CBS}$	breakdown voltage collector to base (emitter and base short-circuited)
$V_{(BR)CEO}$	breakdown voltage collector to emitter (base open circuited)
$V_{(BR)CER}$	breakdown voltage collector to emitter (with specified resistance between base and emitter)
$V_{(BR)CES}$	breakdown voltage collector to emitter (emitter and base-short-circuited)
$V_{(BR)CEX}$	breakdown voltage collector to emitter (with specified circuit between base and emitter)
$V_{(BR)EBO}$	breakdown voltage emitter to base (collector open-circuited)
$V_{(BR)R}$	reverse breakdown voltage
V_{CB}	collector-base voltage (d.c.)
V_{CBO}	collector-base voltage (with emitter open-circuited)
V_{CBfl}	collector-base floating potential
V_{CC}	collector supply voltage (d.c.)
V_{CE}	collector to emitter voltage (d.c.)
V_{CEO}	collector to emitter voltage (with base open-circuited)
V_{ce}	collector to emitter r.m.s. voltage
$V_{CE(knee)}$	collector knee voltage.
$V_{CE(sat)}$	collector to emitter saturation voltage
$V_{CE(sust)}$	collector to emitter sustaining voltage
V_D	thyristor continuous (d.c.) off-state voltage
V_{DG}	drain to gate voltage
V_{DM}	thyristor peak off-state voltage
V_{DRM}	thyristor repetitive peak off-state voltage
V_{DS}	drain to source voltage
V_{DSM}	thyristor non-repetitive off-state voltage
V_{DWM}	thyristor crest (peak) working off-state voltage
V_{EB}	emitter-base voltage (d.c.)
V_{EBO}	emitter-base voltage (with collector open circuited)
V_{eb}	emitter-base r.m.s. voltage
V_{EBfl}	emitter-base floating potential
V_{ECfl}	emitter-collector floating potential
V_F	D.C. forward voltage
v_F	instantaneous total value of the forward voltage
V_{FG}	thyristor forward gate voltage
V_{FGM}	thyristor peak forward gate voltage
V_{fr}	signal diode forward recovery voltage
V_{GB}	gate to substrate voltage
V_{GD}	thyristor gate non-trigger voltage
V_{GS}	gate to source voltage
V_{GT}	thyristor gate trigger voltage
V_I	input voltage
V_{IRM}	repetitive peak input voltage
V_{ISM}	non-repetitive peak input voltage
V_{IWM}	crest working input voltage
V_O	output voltage

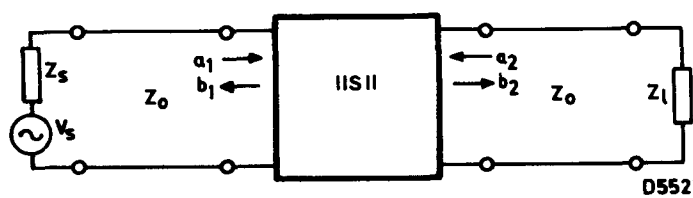
V_P	peak point voltage
V_{PP}	projected peak point voltage
V_R	D.C. reverse voltage
v_R	instantaneous total value of the reverse voltage
V_{RG}	thyristor reverse gate voltage
V_{RGM}	thyristor peak reverse gate voltage
V_{RM}	peak reverse voltage
V_{RRM}	repetitive peak reverse voltage
V_{RSM}	non-repetitive peak reverse voltage
V_{RWM}	crest (peak) working reverse voltage
V_T	thyristor continuous (d.c.) on-state voltage
$V_{T(TO)}$	thyristor threshold voltage
V_V	valley point voltage
V_Z	voltage regulator (zener) diode operating voltage
Z_{if}	intermediate frequency impedance
Z_v	video impedance

y-parameters

Common base	Common emitter		
y_{ib} (y_{11})	y_{ie} (y'_{11})	Input admittance	Output short-circuited
g_{ib} (g_{11})	g_{ie} (g'_{11})	Input conductance	
c_{ib} (c_{11})	c_{ie} (c'_{11})	Input capacitance	
ϕ_{ib}	ϕ_{ie}	Phase angle of input admittance	
y_{ob} (y_{22})	y_{oe} (y'_{22})	Output admittance	Input short-circuited
g_{ob} (g_{22})	g_{oe} (g'_{22})	Output conductance	
c_{obs} (c_{22})	c_{oes} (c'_{22})	Output capacitance	
ϕ_{ob}	ϕ_{oe}	Phase angle of output admittance	
$\lvert y_{fb}\rvert$ ($\lvert y_{21}\rvert$)	$\lvert y_{fe}\rvert$ ($\lvert y'_{21}\rvert$)	Transfer admittance	Output short-circuited
g_{fb}	g_{fe}	Transfer conductance	
c_{fb}	c_{fe}	Transfer capacitance	
ϕ_{fb} (ϕ_{21})	ϕ_{fe} (ϕ'_{21})	Phase angle of transfer admittance	
$\lvert y_{rb}\rvert$ (y_{12})	$\lvert y_{re}\rvert$ (y'_{12})	Feedback admittance	Input short-circuited
g_{rb}	g_{re}	Feedback conductance	
c_{rb}	c_{re}	Feedback capacitance	
ϕ_{rb} (ϕ_{12})	ϕ_{re} (ϕ'_{12})	Phase angle of feedback admittance	

Scattering parameters

In distinction to the conventional h, y and z parameters, s-parameters relate to travelling wave conditions. The figure below shows a two-port network with the incident and reflected travelling wave quantities a_1, b_1, a_2 and b_2, which are square roots of power.



a_1^2 = the power incident at the input $\left(= \frac{V_{i1}^2}{Z_o}\right)$

a_2^2 = the power incident at the output $\left(= \frac{V_{i2}^2}{Z_o}\right)$

b_1^2 = the power reflected from (or generated at) the input $\left(= \frac{V_{r1}^2}{Z_o}\right)$

b_2^2 = the power reflected from (or generated at) the output $\left(= \frac{V_{r2}^2}{Z_o}\right)$

Z_o = the characteristic impedance of the transmission line in which the two-port is connected

V_i = incident voltage

V_r = reflected (generated) voltage

The four-pole equations for s-parameters are:

$$b_1 = s_{11}a_1 + s_{12}a_2$$
$$b_2 = s_{21}a_1 + s_{22}a_2$$

Using the subscripts i for 11, o for 22, f for 21 and r for 12, it follows that

$$s_i = s_{11} = \left.\frac{b_1}{a_1}\right|_{a_2 = 0}$$

$$s_f = s_{21} = \left.\frac{b_2}{a_1}\right|_{a_2 = 0}$$

$$s_o = s_{22} = \left.\frac{b_2}{a_2}\right|_{a_1 = 0}$$

$$s_r = s_{12} = \left.\frac{b_1}{a_2}\right|_{a_1 = 0}$$

a_1 can be made zero by terminating the input side with $Z_s = Z_o$ (no input power and no reflection from the source).

a_2 can be made zero by terminating the output side with $Z_1 = Z_o$ (no reflection from the load).

Because $\frac{b_1}{a_1} = \frac{V_{r1}}{V_{i1}}$ it can be seen that s_i is the input reflection coefficient; in the same way s_o is the output reflection coefficient.

The s-parameters can be named and expressed as follows:

$s_i = s_{11}$ = Input reflection coefficient (for the given characteristic impedance) – Ratio between the square root of the power reflected from the input and the square root of the power incident at the input, output terminated with the characteristic impedance.

$s_f = s_{21}$ = Forward transmission coefficient (for the given characteristic impedance) – Ratio between the square root of the power generated at the output and the square root of the power incident at the input, output terminated with the characteristic impedance.

$s_o = s_{22}$ = Output reflection coefficient (for the given characteristic impedance) – Ratio between the square root of the power reflected from the output and the square root of the power incident at the output, input terminated with the characteristic impedance.

$s_r = s_{12}$ = Reverse transmission coefficient (for the given characteristic impedance) – Ratio between the square root of the power generated at the input and the square root of the power incident at the output, input terminated with the characteristic impedance.

Section III. Explanation of Handbook Data

1. FORM OF ISSUE

The semiconductor data published in the Handbook follows the same pattern, as much as possible, concerning, (a) the forms of issue, (b) the ratings system and (c) the ratings presentation.

1.1 Types of Data

The Handbook data is published either as tentative or final data.

Tentative Data

Tentative data aims at providing information on new devices as early as possible to allow the customer to proceed with circuit design. The tentative data may not include all the characteristics or ratings which will be incorporated later in the final data and some of the numerical values quoted may be slightly adjusted later on.

Final Data

The transfer from tentative data to final data involves the addition of those numerical values and curves which were not available at tentative data stage and small adjustments to those values already quoted in tentative data. Reissue of final data may be made from time to time to incorporate additional information resulting from prolonged production experience or to meet new applications.

1.2 Presentation of Data

The information on the published data sheets is presented in the following form:

—description of basic application and physical characteristics of the device.
—quick reference data giving the most important ratings and characteristics.
—outline and dimensions. Reference to standard outline nomenclature if applicable and lead connections.
—Ratings. Voltage, current, power and thermal ratings.
—Characteristics.
—Application information or operating conditions.
—Mechanical and environmental data if applicable.
—Charts showing ratings and characteristics.

2. RATINGS

A rating is a limiting condition of usage specified for a device by the manufacturer, beyond which the serviceability may be impaired.

A rating system is a set of principles upon which ratings are established and which determines their interpretation. There are three systems which have been internationally accepted and which allocate responsibility between the device manufacturer and the circuit designer differently.

2.1 Rating Systems

Unless otherwise stated the ratings given in semiconductor data sheets follow the absolute maximum rating system.
The definitions of the three systems accepted by the International Electrotechnical Commission are as follows:

ABSOLUTE MAXIMUM RATING SYSTEM

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any device of a specified type as defined by the published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for variations in equipment or environment, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other devices in the equipment.

The equipment manufacturer should design so that initially and throughout life no absolute maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to variations in supply voltage, environment, equipment components, equipment control adjustment, load, signal or characteristics of the device under consideration and of all other devices in the equipment.

DESIGN-CENTRE RATING SYSTEM

Design-centre ratings are limiting values of operating and environmental conditions applicable to a bogey device of a specified type as defined by its published data, and should not be exceeded under normal conditions. These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to variations in supply voltage, environment, equipment components, equipment control adjustment, load, signal or characteristics of all other devices in the equipment. The equipment manufacturer should design so that initially no design-centre value for the intended service is exceeded with a bogey device in equipment operating at the stated normal supply voltage.

DESIGN-MAXIMUM RATING SYSTEM

Design-maximum ratings are limiting values of operating and environmental conditions applicable to a bogey device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the device under consideration.

The equipment manufacturer should design so that initially and throughout life no design-maximum value for the intended service is exceeded with a bogey device under the worst probable operating conditions with respect to variations in supply voltage, environment, equipment components, equipment control adjustment, load, signal or characteristics of the device under consideration and of all other devices in the equipment.

3 Transistor ratings

The ratings are presented as voltage, current, power and temperature ratings. The list of these ratings and their definitions is given as follows:

3.1 Transistor voltage ratings

Collector to base voltage ratings

V_{CB} max	The maximum permissible instantaneous voltage between collector and base terminals. The collector voltage is negative with respect to base in PNP transistors and positive w.r.t. base in NPN types.
V_{CB} max ($I_E = 0$)	The maximum permissible instantaneous voltage between collector and base terminals, when the emitter terminal is open circuited.

Emitter to base voltage ratings

V_{EB} max	The maximum permissible instantaneous reverse voltage between emitter and base terminal. The emitter voltage is negative w.r.t. base for PNP transistor and positive w.r.t. base for NPN types.
V_{EB} max ($I_C = 0$)	The maximum permissible instantaneous reverse voltage between emitter and base terminals when the collector terminal is open circuited.

Collector to emitter voltage ratings

V_{CE} max	The maximum permissible instantaneous voltage between collector and emitter terminals. The collector voltage is negative w.r.t. emitter in PNP transistors and positive w.r.t. emitter in NPN types. This rating is very dependent on circuit conditions and collector current and it is necessary to refer to the curve of V_{CE} versus I_C for the appropriate circuit condition in order to obtain the correct rating
V_{CE} max (Cut-off)	The maximum permissible instantaneous voltage between collector and emitter terminals when the emitter current is reduced to zero by means of a reverse emitter base voltage, i.e. the base voltage is normally positive w.r.t. emitter for PNP transistor and negative w.r.t. emitter for NPN types.

NOTE: The term "cut-off" is sometimes replaced by $V_{BE} > x$ volts, or $\frac{R_B}{R_E}$, $\leqslant y$ which are equivalent conditions under which the device may be cut-off.

V_{CE} max (I_C = x mA) The maximum permissible instantaneous voltage between collector and emitter terminals when the collector current is at a high value, often the max. rated value.

V_{CE} max ($I_B = 0$) The maximum permissible instantaneous voltage between collector and emitter terminals when the base terminal is open circuited or when a very high resistance is in series with the base terminal. Special care must be taken to ensure that thermal runaway due to excessive collector leakage current does not occur in this condition.

Due to the current dependency of V_{CE} it is usual to present this information as a voltage rating chart which is a curve of collector current versus collector to emitter voltage (see Fig. 1).
This curve is divided into two areas:

A permissible area of operation under all conditions of base drive provided the dissipation rating is not exceeded (area 1) and an area where operation is allowable under certain specified conditions (area 2).
To assist in determining the rating in this second area, further curves are provided relating the voltage rating to external circuit conditions, for example:

$$\frac{R_B}{R_E},\ R_B,\ Z_{Bg},\ V_{BE},\ I_B \text{ or } \frac{V_{BB}}{R_B}$$

An example of this type of curve is given in Fig. 2 as V_{CE} versus $\frac{R_B}{R_E}$ for two different values of collector current.

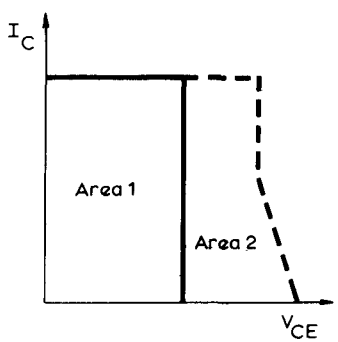


Fig.1

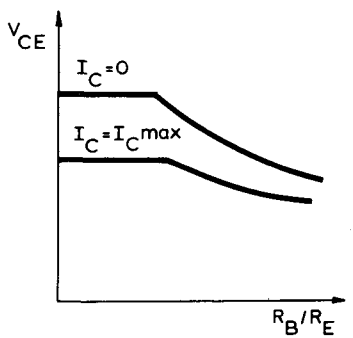


Fig.2

It should be noted that when R_E is shunted by a capacitor, the collector voltage V_{CE} during switching must be restricted to a value which does not rely on the effect of R_E.
In the case of an inductive load and when an energy rating is given, it may be permissible to operate outside the rated area provided the specified energy rating is not exceeded.

3.2 Transistor Current Ratings

Collector current ratings

I_C max	The maximum permissible collector current. Without further qualification, the dc value is implied.
$I_{C(AV)}$ max	The maximum permissible average value of the total collector current.
I_{CM}	The maximum permissible instantaneous value of the total collector current.

Emitter current ratings

I_E max	The maximum permissible emitter current. Without further qualification, the dc value is implied.
$I_{E(AV)}$ max	The maximum permissible average value of the total emitter current.
$I_{ER(AV)}$ max	The maximum permissible average value of the total emitter current when operating in the reverse emitter-base breakdown region.
I_{EM}	The maximum permissible instantaneous value of the total emitter current.
I_{ERM}	The maximum permissible instantaneous value of the total reverse emitter current allowable in the reverse breakdown region.

Base current ratings

I_B max	The maximum permissible base current (without further qualification, the dc value is implied).
$I_{B(AV)}$ max	The maximum permissible average value of the total base current.
$I_{BR(AV)}$ max	The maximum permissible average value of the total reverse base current allowable in the reverse breakdown region.
I_{BM}	The maximum permissible instantaneous value of the total base current. The rating also includes the switch off current.
I_{BRM}	The maximum permissible instantaneous value of the total reverse current allowable in the reverse breakdown region.

3.3 Transistor Power Ratings

P_{tot} max: The total maximum permissible continuous power dissipation in the transistor and includes both the collector-base dissipation and the emitter-base dissipation. Under steady state conditions the total power is given by the expression:

$$P_{tot} = V_{CE} \times I_C + V_{BE} \times I_b$$

In order to distinguish between "steady state" and "pulse" conditions the terms "steady state power (P_S)" and "pulse power (P_P)" are often used. The permissible total power dissipation is dependent upon temperature and its relationship is shown by means of a chart as shown in figure 3.

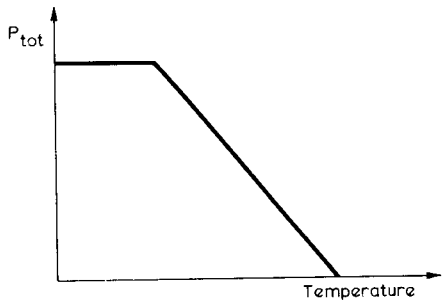


Fig.3

The temperature may be ambient, case or mounting base temperatures. Where a cooling clip or a heatsink is attached to the device, the allowable power dissipation is also dependent on the efficiency of the heatsink.

The efficiency of this clip or heatsink is measured in terms of its thermal resistance (θ_h) normally expressed in degrees centigrade per watt (deg. C/W). For mounting base rated device, the added effect of the contact resistance (θ_i) must be taken into account.

The effect of heatsinks of various thermal resistance and contact resistance is often included in the above chart.

Thus for any heatsink of known thermal resistance and any given ambient temperature, the maximum permissible power dissipation can be established. Alternatively, knowing the power dissipation which will occur and the ambient temperature, the necessary heatsink thermal resistance can be calculated.

A general expression from which the total permissible steady state power dissipation can be calculated is:

$$P_{tot} = \frac{T_j - T_{amb}}{\theta_{j-amb}}$$

where θ_{j-amb} is the thermal resistance from the transistor junction to the ambient. For case rated or mounting base rated devices, the thermal resistance θ_{j-amb} is made up of the thermal resistance junction to case or mounting base (θ_{-mb}), the contact thermal resistance (θ_i) and the heatsink thermal resistance (θ_h).

For the calculation of pulse power operation P_p, the maximum pulse power is obtained by the aid of a chart as shown in figure 4.

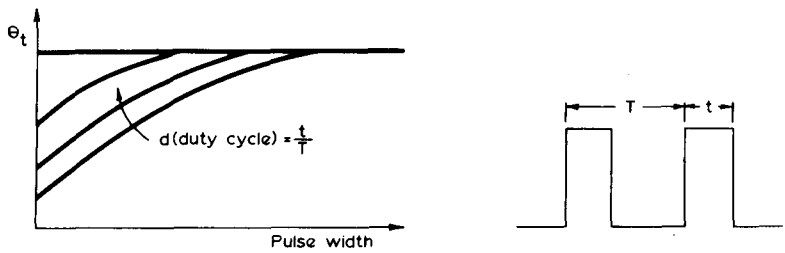


Fig.4

the general expression from which the maximum pulse power dissipation can be calculated is:

$$P_p = \frac{T_j - T_{amb} - P_s \times \theta_{j-amb}}{\theta_t + d(\theta_{case-amb})}$$

where θ_t and d are given in the above chart and $\theta_{case-amb}$ is the thermal resistance between case and ambient for case rated device. For mounting base rated device, it is equal to $\theta_h + \theta_i$ and is zero for free air rated device because the effect of the temperature rise of the case over the ambient for a pulse train is already included in θ_t.

3.4 Temperature Ratings

T_j max	The maximum permissible junction temperature which is used as the basis for the calculation of power ratings. Unless otherwise stated, the continuous value is implied.
T_j max (continuous operation)	The maximum permissible continuous value.
T_j max (intermittent operation)	The maximum permissible instantaneous junction temperature usually allowed for a total duration of 200 hours.
T_{mb}	The temperature of the surface making contact with a heatsink. This is confined to devices where a flange or stud for fixing onto a heatsink forms an integral part of the envelope.
T_{case}	The temperature of the envelope. This is confined to devices to which may be attached a clip-on cooling fin.

Section IV. Mounting and Soldering Recommendations

1. MOUNTING OF "LOCKFIT" TRANSISTORS

1.1 Mounting on printed-wiring boards

The "Lockfit" encapsulation is usable with printed-wiring boards having either the standard e-grid or the more closely spaced ε-grid. The relevant dimensions of these boards are given in Table 1.

TABLE 1
Dimensions of Printed-wiring Boards

Board	Grid	Hole diameter	Maximum board thickness
e-board	2·54mm (0·1in)	1·05±0·05mm (up to 1·30mm allowable)	1·7mm
ε-board	0·635mm (0·025in)	0·80±0·03mm	1·1mm

The pins of "Lockfit" transistors each have three enlargements along their length, as shown in Fig. 1. At the tip is a spade-shaped (lock 'B'); partway up is a tapered cross-piece (lock 'A') that projects further left and right than lock 'B'; and nearest to the body of the assembly is another cross-piece (lock 'C') that extends even further left and right than lock 'A'.

Hole spacing in either type of grid allows the insertion of the "Lockfit" pins; but as the holes of the closely spaced ε-grid are necessarily of smaller diameter than those of the other grid, the pins cannot be (or should not be) pushed in beyond the middle expansion – lock 'A'. Thus the functions of the three locks are as indicated in Fig. 1a for e-grid boards and Fig. 1b for ε-grid boards.

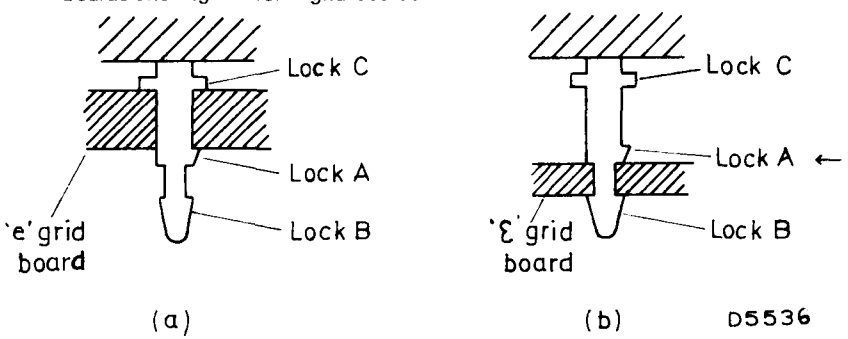


Fig. 1 – *Detail of "Lockfit" pins, and function of three "locks" when used with (a) e-grid and (b) ε-grid printed-wiring boards*

1.1.1 Mounting procedure with e-grid boards

The best insertion procedure with the e-(2·54mm) grid is as follows:
(1) Place the rear two pins into their corresponding printed-circuit board holes with the transistor at a slight angle to the vertical (Fig. 2a).
(2) Place the centre pin into the remaining hole by light pressure at a slight angle to the vertical on the device. Continue this light pressure until both the 'A' locks of the rear two leads are inside the holes (Fig. 2b).
(3) Tilt the device with light pressure from the rear until it is in a vertical position. Lock 'A' of the centre lead will now enter the hole (Fig. 2c).
(4) Move the device perpendicularly downwards with light pressure until all three 'A' locks snap into position beneath the printed-wiring board, and the 'C' locks rest on the upper side of the board (Fig. 2d.)

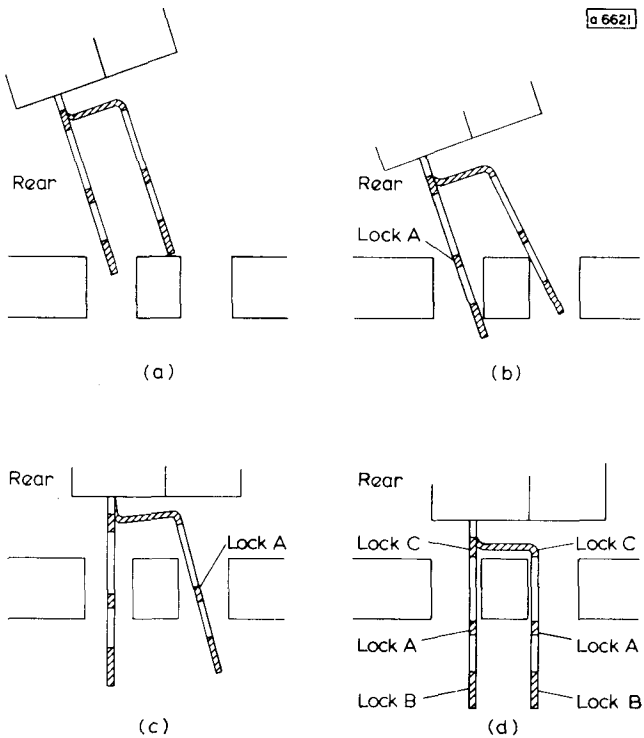


Fig. 2 – *Mounting procedure for "Lockfit" transistors using e-grid printed-wiring boards; procedure is similar for ε-grid boards*

1.1.2 Mounting prodedure with ε-grid boards

The best insertion procedure with the ε-(0·635mm) grid is as follows:
(1) Place the rear two pins into their corresponding printed-circuit board holes with the transistor at a slight angle to the vertical.
(2) Place the centre pin into the remaining hole by light pressure at a slight angle to the vertical on the device. Continue this light pressure until both the 'B' locks of the rear two leads are inside the holes.
(3) Tilt the device with light pressure from the rear until it is in a vertical position. Lock 'B' of the centre lead will now enter the hole.
(4) Move the device perpendicularly downwards with light pressure until all three 'B' locks snap into position beneath the printed-wiring board, and the 'A' locks rest on the upper side of the board.
No attempt should be made to force lock 'A' through this type of board.

1.2 Soldering

For both boards, the temperature should not exceed 300°C and the application time should not exceed 3 seconds.

INTRODUCTION TO TECHNICAL DATA

1. LEAD DESIGNATIONS

Source S, s. Drain D, d. Gate G, g. Substrate B, b.

2. SEQUENCE OF SUBSCRIPTS

The first subscript denotes the terminal at which the current or voltage is measured.

Where the reference terminal or circuit is understood, the second subscript may be omitted where its use is not required to preserve the meaning of the symbol.

The letter O is used with three terminal devices as a third subscript only to denote that the terminal not indicated in the subscript is open circuited. The letter S is used as a third subscript to denote that the terminal not indicated in the subscript is short circuited to the reference terminal. The letter X is used as a third subscript to denote measurements taken under specified circuit conditions.

2.1 Quantity Symbols

V — Voltage
I — Current
P — Power

i	d	
v with subscripts	s	instantaneous value of varying component
p	g	
i	D	
v with subscripts	S	instantaneous total value
p	G	
I	d	the r.m.s. value of the varying component or
V with subscripts	s	with appropriate subscript the peak (m) average
P	g	(d.c.) (av) value of the varying component
I	D	the no-signal (d.c.) value of or with the
V with subscripts	S	appropriate additional subscripts the total
P	G	average value (AV) with signal or the total peak value (M)

The letter symbol usually indicates by two subscripts the two reference terminals. The first subscript indicates the terminal which is positive with respect to the second subscript.
e.g.

$V_{DS} = 6V$: Drain is 6V positive w.r.t. Source

$V_{DS} = -6V$: Drain is 6V negative w.r.t. Source

Reversal of the subscripts also changes the polarity sign
For example the following statements are identical

$$V_{DS} = -6V;\ V_{SD} = 6V;\ -V_{DS} = 6V$$

The supply voltage shall be indicated by repeating the terminal subscript. The reference terminal may then be designated by the third subscript.

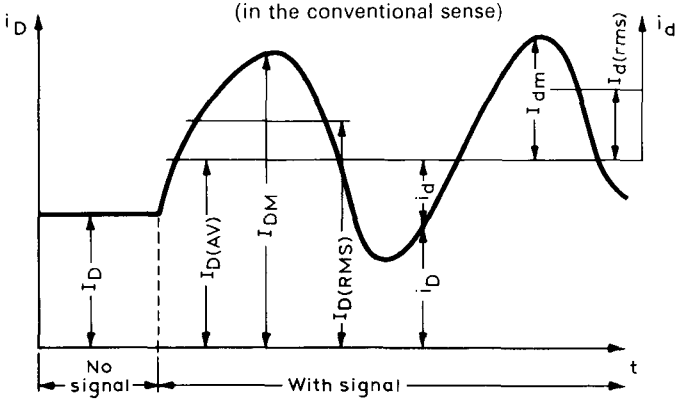
Examples V_{DD}, V_{SS}, V_{SSD}

2.3 Current

Conventionally, current which flows into the transistor terminals has a positive value.

e.g. $I_D = 1mA$ means 1mA flowing into the drain terminal (in the conventional sense)

$I_S = -1mA$ means 1mA flowing out of the source terminal (in the conventional sense)



Examples

I_D	d.c. drain current—no signal
$I_{D(AV)}$	Average (d.c.) value of total drain current with signal applied
I_{DM}	Peak value of total drain current
$I_{D(RMS)}$	Root-mean-square value of total drain current
i_D	Instantaneous value of total drain current
I_{dm}	Peak value of the varying component of the drain current
$I_{d(rms)}$	Root-mean-square value of varying component of drain current
i_d	Instantaneous value of varying component of the drain current

The following are examples of the implied relationship

$$I_{DM} = I_{D(AV)} + I_{dm};\ i_D = I_{D(AV)} + i_d;\ I_{D(RMS)} = \sqrt{I_{D(AV)}^2 + I_{d(rms)}^2}$$

To avoid any misunderstanding with maximum or minimum values the negative sign is always put in front of the letter symbol and not in front of the value given.

For example in quoting a limit value

$$-I_S \text{ max} = 50\text{mA}$$

and in quoting a spread value

$$-V_{P(GS)} \leqslant 1{\cdot}5\text{V}$$

In devices having more than one terminal of the same type the terminal subscripts shall be modified by adding one number following the subscript and on the same line.

Examples:

V_{G1S}, V_{G2S}, refers to a dual gate MOS device

$|V_{G1S1} - V_{G2S2}|$ refers to a matched pair of junction FET's

where the gate-source voltage of the first device is referred to the gate-source voltage of the second device, as a modulus of their difference over a given temperature range.

2.4 The first subscript in the matrix notation identifies the element of the four pole matrix.

i — input
o — output
f — forward transfer
r — reverse transfer.

A second subscript may be used to identify the circuit configuration.

d — common drain
s — common source
g — common gate

Examples

C_{is} C_{os} C_{rs}

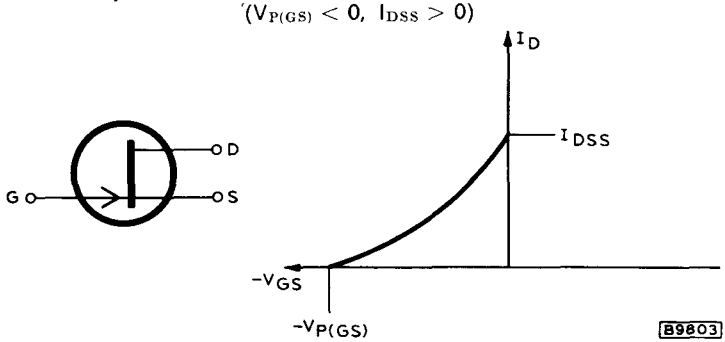
Input, output and reverse feedback capacitances in common source configuration.

3. TYPES OF FIELD EFFECT TRANSISTORS

3.1 Junction gate Field effect transistors

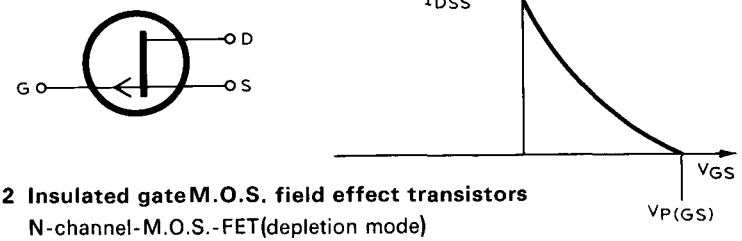
N-channel-junction FET

$(V_{P(GS)} < 0,\ I_{DSS} > 0)$



P-channel-junction FET

($V_{P(GS)} > 0$, $I_{DSS} < 0$)

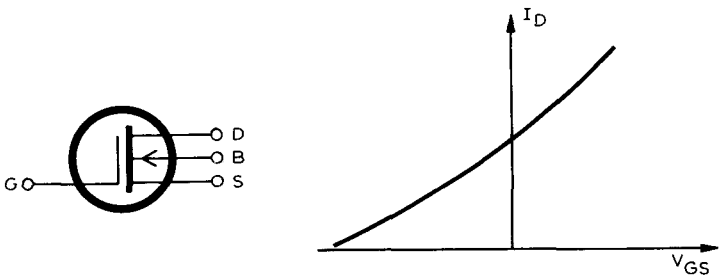


B9804

3.2 Insulated gate M.O.S. field effect transistors

N-channel-M.O.S.-FET (depletion mode)

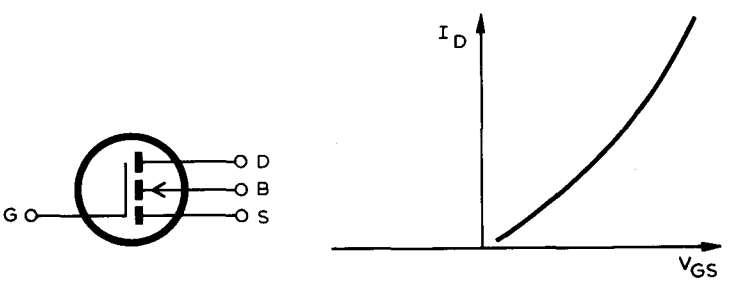
($V_{P(GS)} < 0$, $I_{DSS} > 0$)



B9805

N-channel-M.O.S.-FET (enhancement mode)

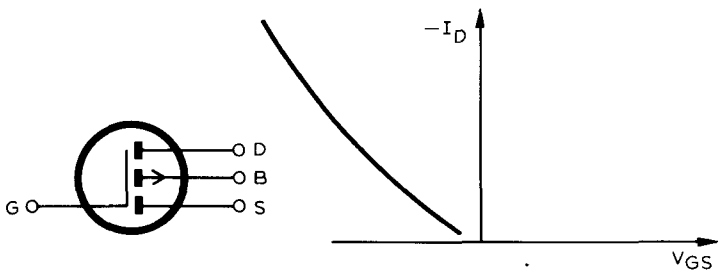
($V_{P(GS)} \geq 0$ $I_{DSS} \approx 0$)



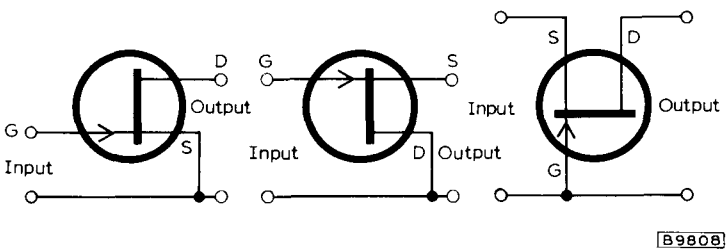
B9806

P-channel-M.O.S.FET (enhancement mode)

($V_{P(GS)} \leqslant 0$, $I_{DSS} \approx 0$)



4. BASIC CIRCUITS CONFIGURATIONS



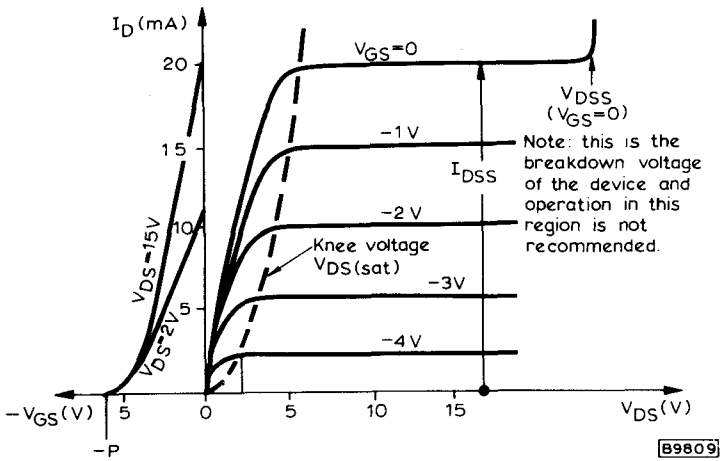
Grounded-source	Grounded-drain	Grounded-gate
The source is common to input and output	The drain is common to input and output	The gate is common to input and output

An additional subscript s, d or g may be used to identify the circuit configuration

Example C_{is} is input capacitance with grounded source

5. CHARACTERISTICS

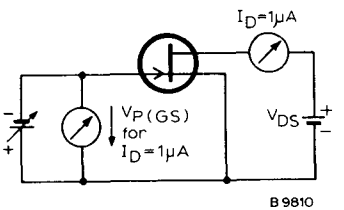
The characteristics are given in data sheets as either typical values and/or minimum and maximum values. Published curves are usually typical curves and are applicable only at the stated temperature.



5.1 Cut-off Voltage ($V_{P(GS)}$)

The cut-off voltage $V_{P(GS)}$ is the gate-source voltage for a given small value of drain current I_D at a stated drain source voltage V_{DS}

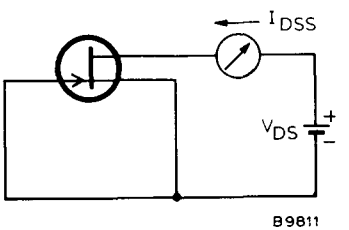
TEST CIRCUIT FOR $V_{P(GS)}$



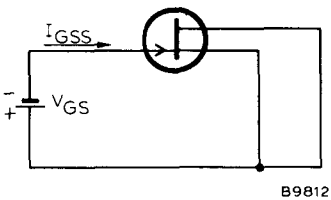
5.2 Drain-source short circuit current (I_{DSS})

The drain-source short circuit current $I_{(DSS)}$ is the current flowing between drain and source with the gate short-circuited to the source (V_{GS} = 0) and at a stated drain-source voltage (V_{DS})

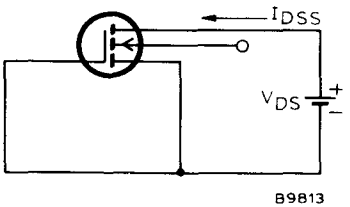
TEST CIRCUIT FOR I_{DSS}



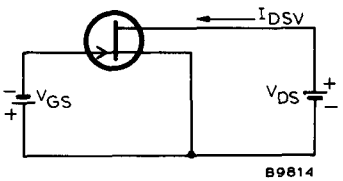
5.3 Leakage currents



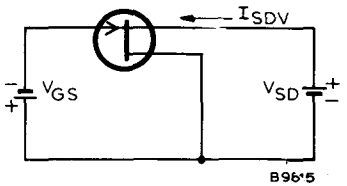
Gate-source leakage/current
I_{GSS}



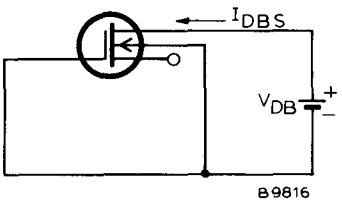
Drain-source leakage current
I_{DSS}
(enhancement mode device)



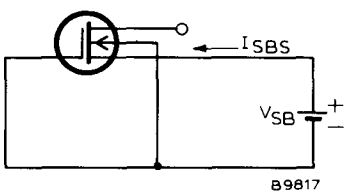
Drain-source leakage current
I_{DSV}, at specified V_{DS} and V_{GS}
and grounded source



Source-drain leakage current
I_{SDV} with specified V_{SD} and V_{GS}
with grounded drain



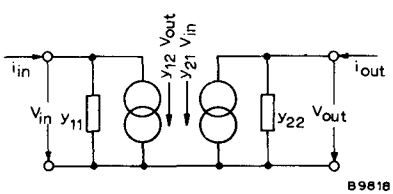
Drain-substrate leakage current
I_{DBS}



Source-substrate leakage current
I_{SBS}

6. SMALL SIGNAL-Y PARAMETERS

Four-pole equivalent circuit



$y_{11} = y_i = \frac{i_{in}}{V_{in}} V_{out} = 0$ input admittance with output short circuited

$y_{12} = y_r = \frac{i_{in}}{V_{out}} V_{in} = 0$ reverse transfer admittance with input short circuited

$y_{21} = y_f = \frac{i_{out}}{V_{in}} V_{out} = 0$ forward transfer admittance with output short circuited

$y_{22} = y_o = \frac{i_{out}}{V_{out}} V_{in} = 0$ Output admittance with input short circuited

A second subscript on the y-parameter indicates the circuit configuration

e.g. y_{is} = input admittance in common source configuration

where y_{is} is the complex form

$$y_{is} = g_{is} + jb_{is} \quad \text{and} \quad b_{is} = \omega c_{is}$$

For example

C_{is} = input capacitance in common source

and

C_{rs} = feedback capacitance in common source

The forward transfer admittance in common source configuration at low frequency (e.g. below about 1MHz) is indicated in the following forms

$$gm = g_{21s} = g_{fs} = |y_{fs}|$$

at high frequency this parameter is a complex quantity and the modulus $|y_{fs}|$ is usually given in the data with a specified frequency of measurement.

ABSOLUTE MAXIMUM RATING SYSTEM

7. Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any device of a specified type as defined by the published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for variation in equipment or environment, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other devices in the equipment.

The equipment manufacturer should design so that initially and throughout life no absolute maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to variations in supply voltage, environment, equipment components, equipment control adjustment, load, signal or characteristics of the device under consideration and of all other devices in the equipment.

7.1 Ratings (maximum permissible values)

V_{DS} max	—	Drain-source voltage
V_{DB} max	—	Drain-substrate voltage
V_{SB} max	—	Source-substrate voltage
V_{GD} max	—	Gate-drain voltage
V_{GS} max	—	Gate-source voltage
V_{GB} max	—	Gate-substrate voltage
I_D max	—	Drain current
I_S max	—	Source current
*I_G max	—	Gate Current

*applies only to junction F.E.T.'s if a forward-voltage is applied to the gate.

7.2 Power Dissipation

where T_j max = maximum permitted junction temperature
T_{amb} max = maximum permitted ambient temperature
T_{case} max = maximum permitted case temperature
$R_{th(j\text{-}amb)}$ = Thermal resistance junction to ambient
$R_{th(case\text{-}amb)}$ = Thermal resistance case to ambient.

The limiting value of the maximum permitted device dissipation P_{tot} max is stated for either

$$T_{amb} = \frac{T_j \text{ max} - T_{amb} \text{ max}}{R_{th(j\text{-}amb)}}$$

and

$$P_{tot} \text{ max} = \frac{T_j \text{ max} - T_{case} \text{ max}}{R_{th(case\text{-}amb)}}$$

8. SOLDERING AND WIRING RECOMMENDATIONS

8.1 When using a soldering iron, transistors may be soldered directly into the circuit, but heat conducted to the junction should, if possible, be kept to a minimum by the use of a thermal shunt.

8.2 Transistors may be dip-soldered at a solder temperature of 245°C for a maximum soldering time of five seconds. The case temperature during soldering must not at any time exceed the maximum storage temperature. These recommendations apply to a transistor mounted flush on a board having punched-through holes, or spaced at least 1·5mm above a board having plated-through holes.

8.3 Care should be taken not to bend the leads nearer than 1·5mm from the seal.

8.4 If devices are stored at temperatures above 100°C before incorporation into equipment, some deterioration of the external surface is likely to occur which may make soldering into the circuit difficult. Under these circumstances, the leads should be retinned using a suitable activated flux.

9. OPERATING NOTE (M.O.S. insulated gate F.E.T.'s)

Mounting and handling instructions

To exclude the possibility of damage to the gate oxide layer by an electrostatic charge building up on the high resistance gate electrode, the device is fitted with a conductive rubber ring around the leads. This ring should not be removed until after the device has been mounted in the circuit.

SECTION VI

Safe Operating ARea for power transistors

INTRODUCTION

One of the main restrictions in the operation of power transistors is the phenomenon known as 'second breakdown'. This is the name given to a transistor condition whereby the collector-emitter voltage abruptly switches from a high to a low voltage with increased current.

A diagram illustrating the output characteristics of a power transistor is shown in Fig. 1. It is not representative of any particular device but merely serves to demonstrate the I_C against V_{CE} characteristics of a transistor as it goes into second breakdown. On the horizontal axis the forward and reverse-biased base regions are clearly grouped, with the base open-circuit condition dividing the two regions.

The transistor will enter second breakdown at a certain critical current value

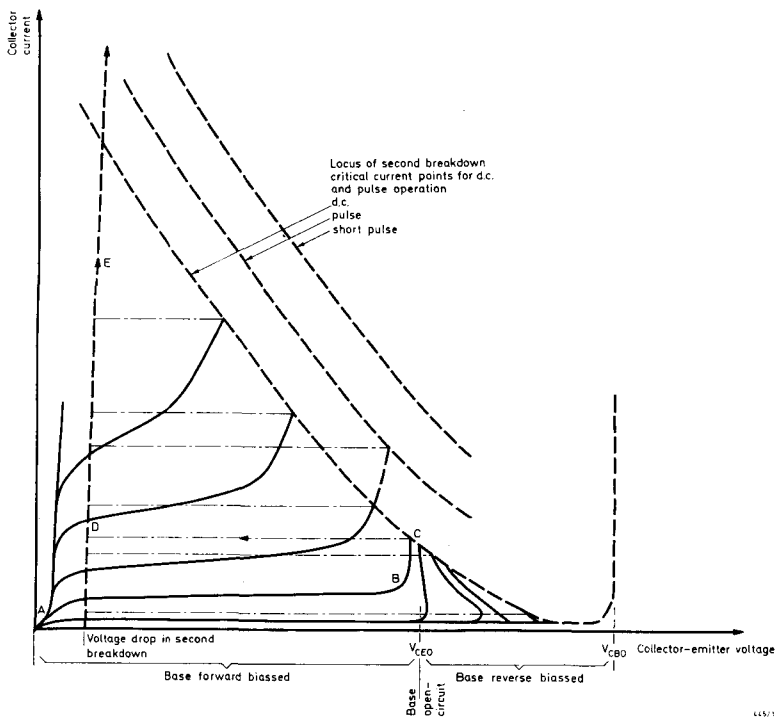


Fig. 1—Output characteristics of a power transistor

which is low at high collector-emitter voltages and higher at low voltages. Three loci for critical current values are shown on the diagram; these represent d.c., pulse, and short pulse operation. The extension of the second-breakdown locus for pulse operation is dependent on the pulse duration t_p and also, to a lesser extent, on the duty cycle d (see Figs. 2 and 3). Thus the greatest extension is permissible with single-shot pulses (d = 0·01) of short duration, say 10μs. (The value d = 0·01 can be considered as single-shot because there is ample time for cooling between power pulses).

Observation of second breakdown

Consider the I_C against V_{CE} characteristic ABCDE shown in Fig. 1. At point B the device goes into avalanche, otherwise known as first breakdown. At this point the collector current starts to rise sharply for very little increase in the collector-emitter voltage. If the current is allowed to increase up to a critical value at C the device will enter second breakdown. This is noted by an abrupt switching of the collector-emitter voltage to a low value at point D. In second breakdown the device offers only a very low resistance to collector current, and is invariably destroyed if the current is not specially limited by a circuit external to the transistor. Beyond point C the process is generally irreversible whereas up to point C in avalanche the trace can be returned with no serious alteration to the transistor properties. It is in the forward-biased mode of operation that the phenomenon of second breakdown has been extensively studied over recent years, and a method of presenting the Safe Operating ARea (abbreviated to SOAR) is now being published in Mullard data for power transistors.

In many applications, however, the reverse-bias breakdown characteristics are also of importance. For example, when a power transistor with an inductive load is turned off by reverse biasing the base, the collector voltage will rise above the supply voltage because of the stored inductive energy of the coil. For such applications transistors have been developed which permit excursions outside the V_{CEO}max rating under specified conditions.

With reverse bias on the base, second breakdown is always preceded by first-breakdown. At low collector currents the voltage across the transistor can exceed the V_{CEO} rating as shown in Fig. 1. In first breakdown, or avalanche, the device goes through a negative resistance region until a critical current value is reached at which point the collector-emitter voltage abruptly switches to a very low value in second breakdown.

Second breakdown in the transistor is usually caused by current concentration at a point in the emitter active area; this is described in detail elsewhere[1]

SIMPLE METHOD OF USING PUBLISHED SOAR CURVES

In addition to the methods described in the MTC article [1] sufficient SOAR information is provided in the published data of each power transistor to cover 90% of all applications.

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[1] TP 1454 reprinted from MTC No. 122 APRIL 1974

Thus, in most cases the user will merely select the appropriate SOAR curve already constructed—without having to calculate and manipulate M_{SB} values.

In general, the data provides SOAR curves for pulse durations in multiples of 1, 2, 5, and 10, starting at pulse durations in the region 10 to 50μs. The families of curves are plotted at duty cycles of 0·01 (single-shot) 0·1, 0·2, 0·5, and 1·0 (d.c.). The transient thermal impedance curves are also included so that the operating mounting-base temperature can be calculated. Typical SOAR data curves for duty cycles of 0·2, 0·5 are illustrated in Figs. 4 and 5.

These curves will be used in the examples that follow.

In the few applications (about 10%) which are not covered by the published SOAR curves, the user can derive M_{SB} curves from the single-shot and d.c. SOAR information, and construct the boundaries using the method fully described in the reference TP 1454

All Mullard data, including pulsed power ratings, assume the use of square waves and resistive loads. Therefore, the system for using the SOAR and transient thermal impedance curves to be described deals with this type of waveform first, and then methods for other practical cases will be considered. It is assumed that the electrical and time conditions are the fixed parameters of an application at the design stage, and that the thermal conditions can be most easily adjusted. The maximum

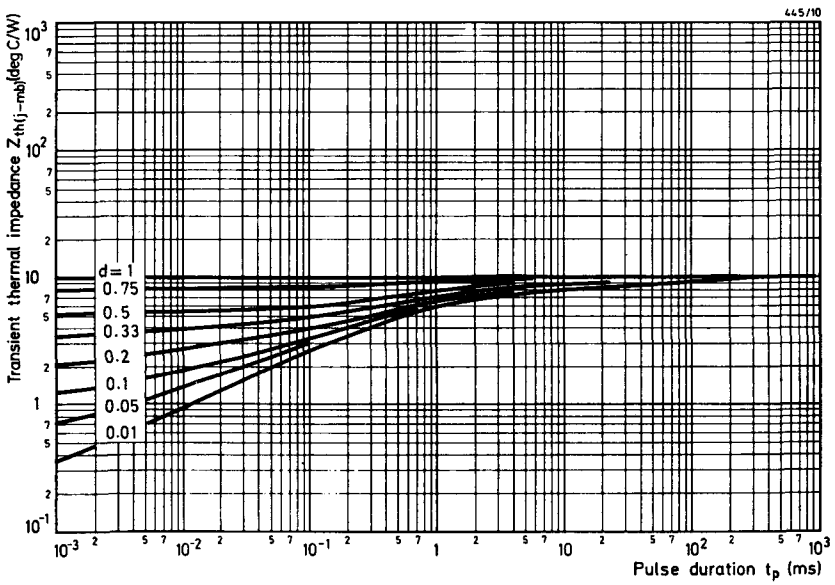


Fig. 2—Typical thermal impedance curves at various duty cycles

power must be calculated at the worst-case condition; when the worst-case condition is not obvious, all discrete sets of conditions need to be assessed.

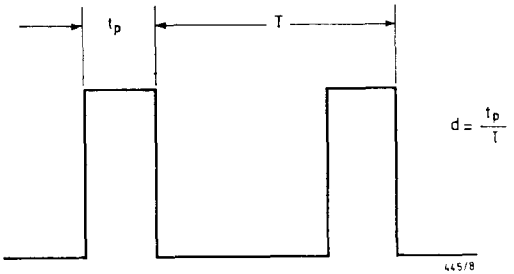


Fig. 3—Relationship between duty cycle (d), pulse duration (t_p) and period (T)

Construction of SOAR using published data

The procedure for constructing a SOAR for one specific set of conditions is described with reference to the curves shown in Figs. 4 and 5, and to the transient thermal impedance curves in Fig. 2.

1) Note the pulse duration t_p (for example, 1·7ms).
2) Note the time between pulses ($T-t_p$) (for example, 2·9ms).
3) Calculate the dutycycle d from the equation $d = t_p/T$ (in this example 0·37).
4) Note the peak collector current I_{CM} (for example 300mA).
5) Note the peak collector emitter voltage V_{CEM} (for example, 35V).
6) Select the SOAR curve with time conditions greater than or equal to the time conditions of the application (in this example, for $d = 0{\cdot}37$ use $d = 0{\cdot}5$ and for $t_p = 1{\cdot}7$ms use $t_p = 2{\cdot}0$ms).
7) Plot the point given by the specific I_{CM} and V_{CEM} values, shown as point Q in Fig. 5.
8) The point Q is acceptable if it is contained within the area of the 2ms/0·5 SOAR as shown in this example.

Thermal calculations

The maximum permissible mounting base temperature is now determined as follows:—

1) Determine peak power by multiplying I_{CM} by V_{CEM}.
2) Calculate the transient thermal impedance for 1·7ms at 0·37 duty cycle.

The equation used is:

$$Z_{th(td)} = \{R_{th} - Z_{th(to)}\}d + Z_{th(to)},$$

Where $Z_{th(td)}$ is the thermal impedance for pulse duration t at duty cycle d, and $Z_{th(to)}$ is the thermal impedance for pulse duration t at duty cycle $d = 0{\cdot}01$ (from Fig. 2).

3) Calculate the difference between the junction and mounting-base temperature from:

$$(T_j - T_{mb}) = Z_{th(td)} \times I_{CM} \times V_{CEM}.$$

4) Calculate the maximum permissible mounting-base temperature $T_{mb}max$ from:

$$T_{mb}max = T_j max - (T_j - T_{mb}).$$

5) A heatsink which limits the mounting-base temperature to this value is required. The thermal capacity of the heatsink will be such that the transient effect of the power will be averaged. Hence the thermal resistance is calculated using average power. Thus:

$$R_{th(h-a)} = \frac{T_{mb}max - T_{amb}}{I_{CM} \times V_{CEM} \times d} - R_{th(mb\ h)} \text{degC/W},$$

Where $R_{th(h-a)}$ is the thermal resistance of heatsink to ambient and $R_{th(mb-h)}$ is the contact thermal resistance.

6) The physical size of the required heatsink can be determined from heatsink published data or from the nomogram in Appendix 1.

Operating selected outside SOAR

Suppose the application had required an I_{CM} of 400mA instead of 300mA. In this case the point P on Fig. 4 would be given. Point P is outside the 2ms area which indicates that the condition may be unacceptable. Thus a closer approximation to the true conditions is necessary.

1) Using linear interpolation between the 1 and 2ms curves at d = 0·5 (Fig. 5) draw a SOAR curve for t_p = 1·7ms. If point P is within this area then the conditions are acceptable and the heatsink thermal resistance can be calculated.
2) If point P is outside the 1·7ms area, then determine the 1·7ms area on the family of curves for d = 0·2 (Fig. 4). A further linear interpolation between the two 1·7ms areas is then needed to approximate to the 1·7ms SOAR at duty cycle of 0·37.
3) If point P is outside this area, then the condition is unacceptable, and a different transistor should be considered.

The above method is not absolutely accurate, but the approximation errors involved are allowed for in the published data tolerances. More accurate calculations can be made by going back to first principles, and calculating the multiplying factor for the specific condition. [1]

[1] TP 1454 reprinted from MTC No. 122 APRIL 1974

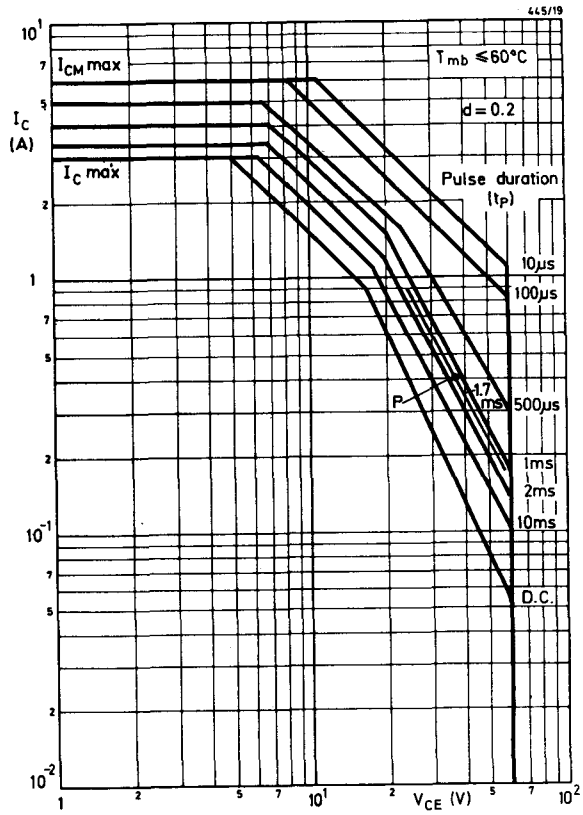


Fig. 4 —Typical SOAR family for d = 0·2 (20% duty cycle)

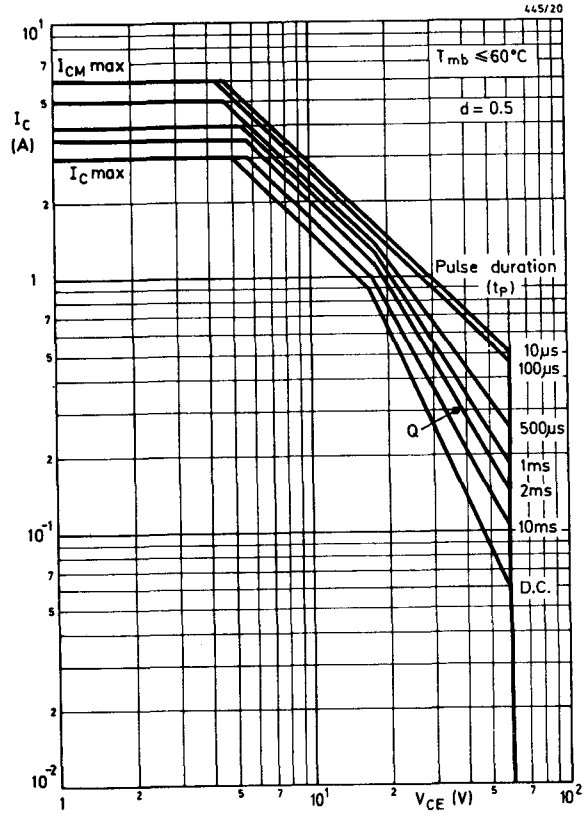


Fig. 5 —Typical SOAR family for d = 0·5 (50% duty cycle)

PRACTICAL APPLICATION

This section discusses a typical application in which power transistors are used.

Audio application

The example describes how the output transistors of an audio amplifier are checked for excursions outside the specified SOAR when the amplifier is being tested under a sinewave overdrive condition.

This example describes how the SOAR curves are used to check the suitability of the BD131 power transistors in a television audio amplifier application. The amplifier is a class A design capable of delivering an output of 2W. The circuit configuration is shown in Fig. 6.

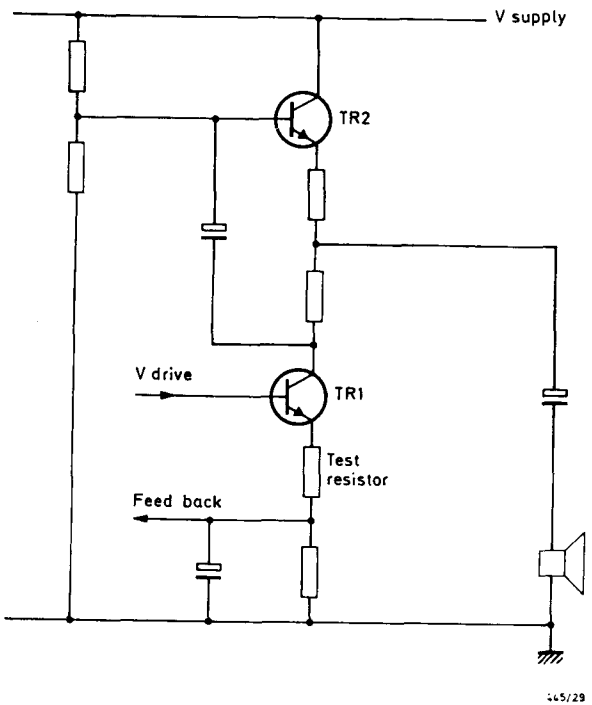


Fig. 6—Circuit configuration of television audio output stage

The amplifier provides the required output power but the second breakdown acceptability has to be checked, and the thermal requirements of the heatsinks are to be calculated.

In this example the SOAR acceptability is considered in the event of the transistors being overdriven by a sinewave signal of period 960μs. A test resistor of 0·1Ω is

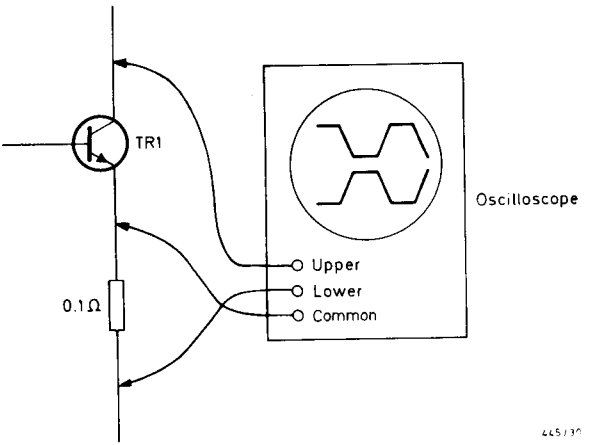


Fig. 7—Method of connecting dual-trace oscilloscope to obtain simultaneous display of I_C and V_{CE}

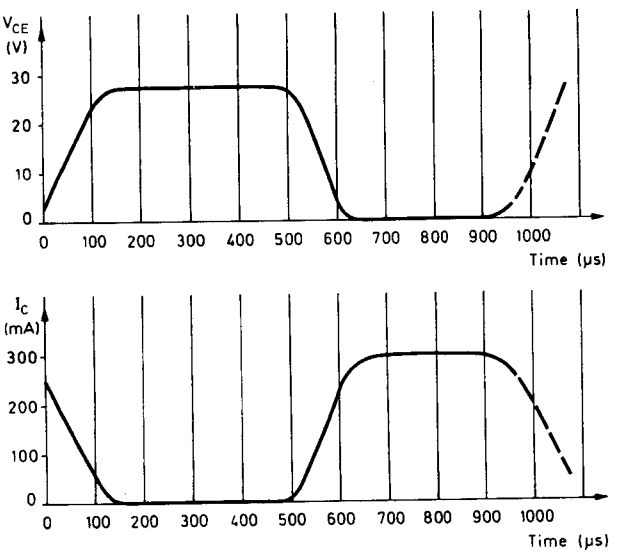


Fig. 8—V_{CE} and I_C characteristics

inserted in the emitter circuit of the lower transistor TR_1. A simultaneous display of the V_{CE} and I_C waveforms is then obtained by connecting the probes of a dual-trace oscilloscope in the manner shown in Fig. 7. The traces of V_{CE} and I_C taken from the oscilloscope are shown in Fig. 8 and the measurements from the waveforms are recorded in Table 1. These readings were recorded every 20μs through the complete cycle of 960μs. In the final column of Table 1, values of instantaneous power are calculated and plotted against time in Fig. 9. This curve is then converted into a series of equivalent squarewave pulses having the same peak power values as the actual pulses. The equivalent squarewave pulses are shown by the dashed line and are marked P_1, P_2, and P_3 in Fig. 9.

Each pulse is then checked individually. The duty cycle for each equivalent squarewave pulse is calculated, and the V_{CE} and I_C values recorded over the duration of the pulse are checked on the appropriate SOAR curve.

TABLE 1

Measured values of I_C and V_{CE} and derived $P_{(tot)}$ obtained from oscilloscope display

Time (μs)	I_C (mA)	V_{CE} (V)	$P_{(tot)}$ (W)
0	260	2	0·52
20	220	6	1·32
40	180	12	2·16
60	140	16	2·24
80	90	20	1·80
100	50	25	1·25
120	5	29	0·15
then no important changes until			
500	5	25	0·14
520	40	25	1·00
540	80	20	1·60
560	130	15	1·95
580	180	10	1·80
600	220	5	1·10
620	260	1	0·26
until			
940	280	1	0·28
960	260	2	0·52

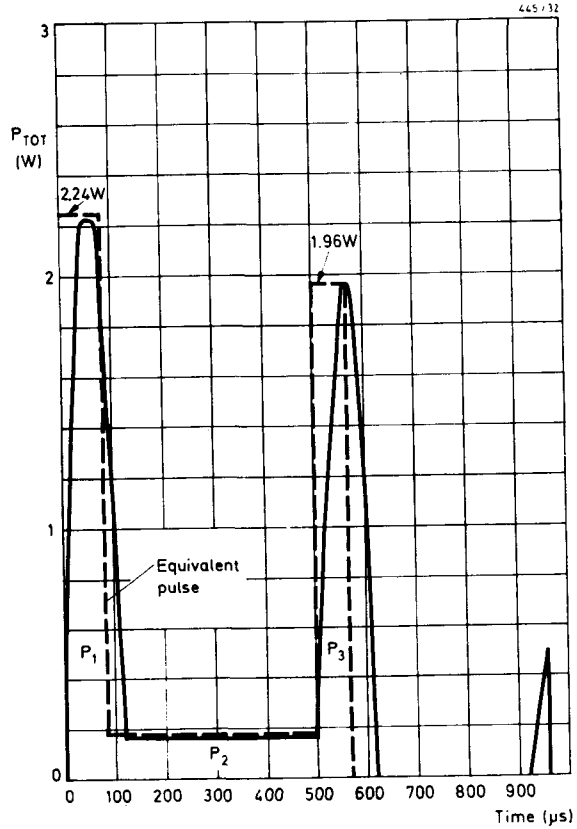


Fig. 9— P_{tot} against time characteristic showing equivalent squarewave pulses

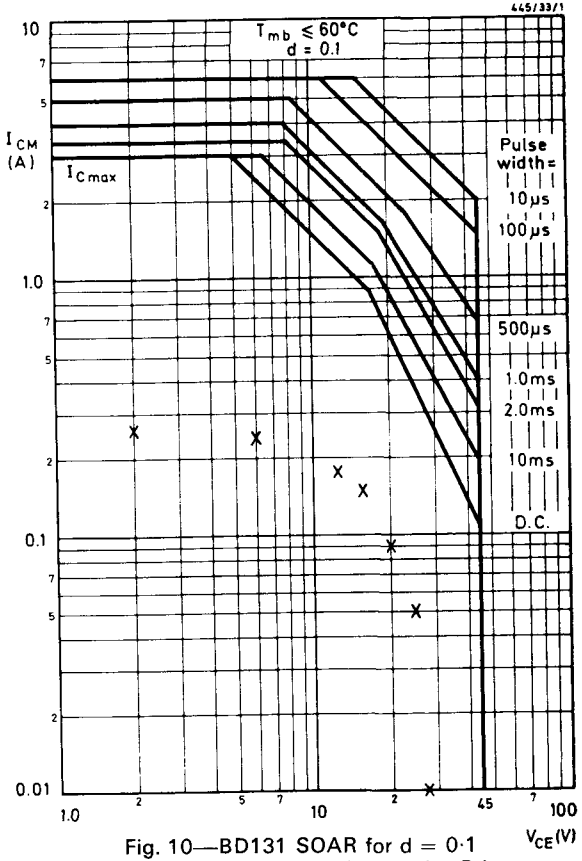


Fig. 10—BD131 SOAR for d = 0·1
(acceptability check for pulse P_1)

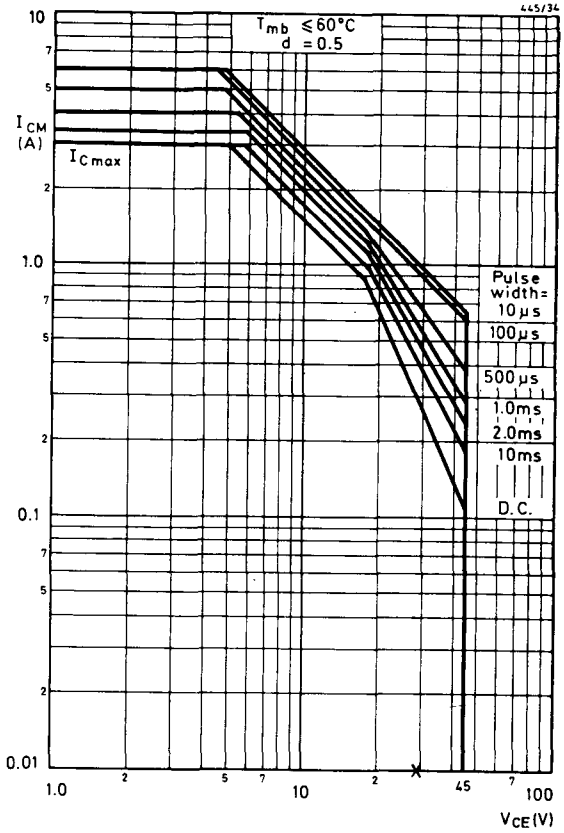


Fig. 11—BD131 SOAR for d = 0·5
(acceptability check for pulse P_2)

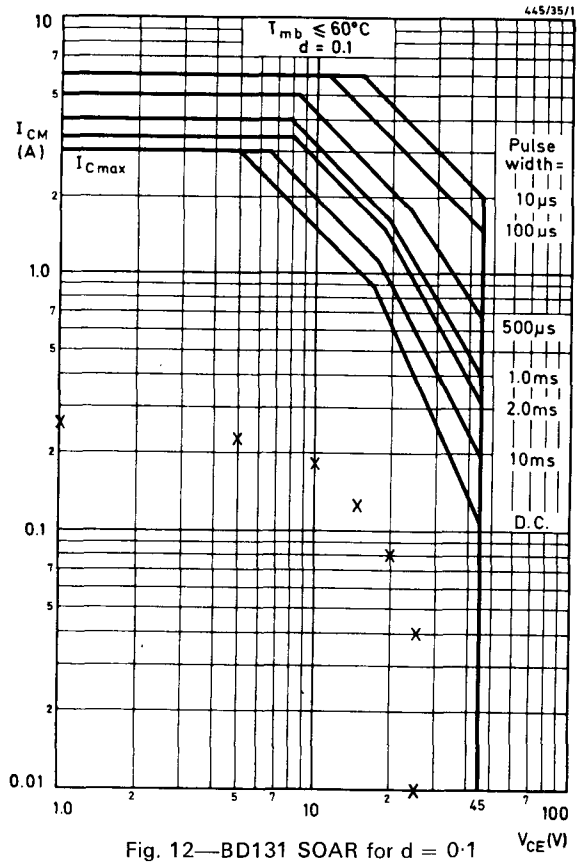


Fig. 12—BD131 SOAR for d = 0·1
(acceptability check for pulse P_3)

Consider pulse P_1: the equivalent pulse time t_{p1} is 82·5μs and the total cycle time T is 960μs. Therefore the duty cycle d_1 is 82·5/960 or 0·086. The V_{CE} and I_C values recorded up to the end of the pulse time t_{p1} are then plotted on the SOAR curve for d = 0·1 as shown in Fig. 10. The locus of this plot falls well within the t_p = 100μs limit, therefore this condition is acceptable. In figs. 10 to 12, the 5mA point is plotted on the 10mA line for convenience, this makes no difference to the result.

The same procedure is followed for checking the acceptability of pulses P_2 and P_3. For P_2 the duty cycle is 420/960 or 0·44; thus the V_{CE} and I_C measurements recorded for pulse P_2 are plotted on the SOAR curve for d = 0·5 as shown in Fig. 11. For P_3 the duty cycle is 70/960 or 0·073, so the V_{CE} and I_C measurements recorded for pulse P_3 are again plotted on the SOAR curve for d = 0·1 as in Fig. 12.

In all three cases the pulse conditions are acceptable since not even the d.c. SOAR limits are exceeded. Thus, the transistor will not fail through second breakdown even when the amplifier is continuously overdriven.

Heatsink calculations

The heatsinks have to be designed to keep the junction temperature below the rating of 150°C. The known thermal restraints are the standard ambient temperature of 60°C allowed for in television enclosures, and the thermal impedances associated with the BD131. The thermal impedance curves for the BD131 are shown in Fig. 13, and the contact thermal resistance $R_{th(mb-h)}$ is 1 degC/W.

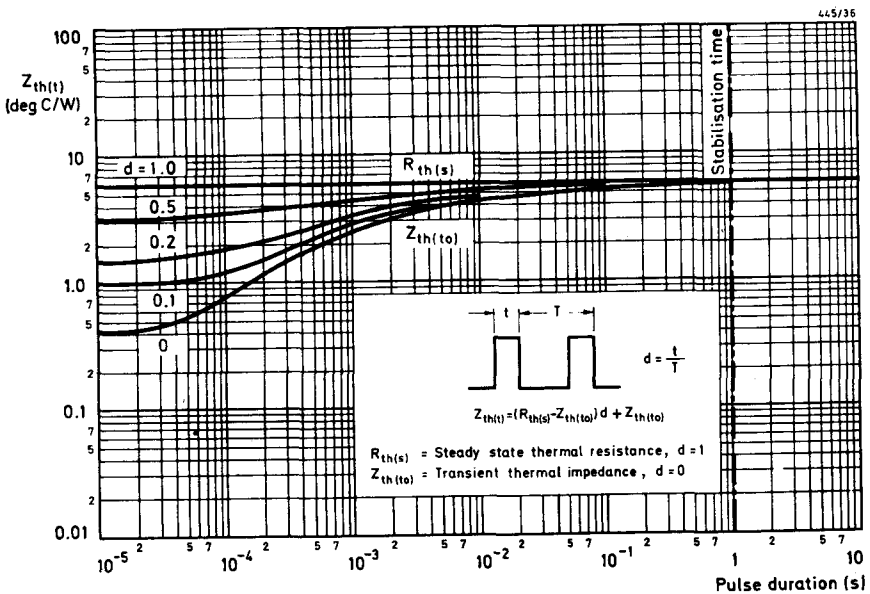


Fig. 13—Thermal impedance curves for BD131

The calculations used to determine the size of the required heatsinks involve average power values, as follows:

$$R_{th(h-a)} = \frac{T_{mb}max - T_a}{P_{av}} - R_{th(mb-h)}, \quad \ldots(1)$$

where:

$$T_{mb}max = T_j max - (T_j - T_{mb})max. \quad \ldots(2)$$

Therefore:

$$R_{th(h-a)} = \left(\frac{T_j max - (T_j - T_{mb})max - T_a}{P_{av}}\right) - R_{th(mb-h)} \quad \ldots(3)$$

Two average powers have to be considered; that during the overload condition and that during the quiescent state. Since this is a class A amplifier, 2W will be dissipated in each of the output transistors during the quiescent condition, and this will be the d.c. bias condition. Under the overload condition the average power value is calculated as follows:

average heat input per cycle

$$= [(t_{p1} \times P_1) + (t_{p2} \times P_2) + (t_{p3} \times P_3)]/T, \quad \ldots(4)$$

$$= [(82.5 \times 2.24) + (420 \times 0.15) + (70 \times 1.96)]/960 \quad = \frac{385\mu sW}{960\mu s} = 0.4W.$$

The calculation of heatsink sizes should be determined under worst-case conditions. This occurs when the quiescent state is followed by the overload conditions. Since the average overload power is less than the quiescent power the first cycle of overload will define the $(T_j - T_{mb})max$.

The maximum value of $(T_j - T_{mb})$ is to be the greater of the two values given by the equations (5) and (6) below.

$$(T_j - T_{mb})max = P_Q \times R_{th} + (P_1 - P_Q)Z_{th}t_{p1}, \quad \ldots(5)$$

$$\text{and } (T_j - T_{mb})max = P_Q \times R_{th} + (P_1 - P_Q)Z_{th}(t_{p1} + t_{p2} + t_{p3})$$

$$-(P_1 - P_2)Z_{th}(t_{p2} + t_{p3}) + (P_3 - P_2)Z_{th}t_{p3}, \quad \ldots(6)$$

where:

quiescent power $P_Q = 2W$

$P_1 = 2.24W$

$P_2 = 0.15W$

$P_3 = 1.96W$

$t_{p1} = 82.5\mu s$

$t_{p1} + t_{p2} + t_{p3} = 572.5\mu s$

$t_{p2} + t_{p3} = 490.0\mu s$

$t_{p3} = 70\mu s$

$R_{th} = 6degC/W$

$Z_{th}t_{p1} = 0.72degC/W$

$Z_{th}(t_{p1} + t_{p2} + t_{p3}) = 2.0degC/W$

$Z_{th}(t_{p2} + t_{p3}) = 1.8degC/W$

$Z_{th}t_{p3} = 0.63degC/W.$

Thus, Eq. 5 becomes:

$$(T_j - T_{mb})max = (2 \times 6) + (0.24 \times 0.72) \quad = (12 + 0.2) \quad = 12.2degC.$$

Eq. 6 becomes:

$$(T_j - T_{mb})max = (2 \times 6) + (0.24 \times 2) - (2.09 \times 1.8) + (1.81 \times 0.63),$$

$$= 12 + 0.48 - 3.76 + 1.14 \quad = 9.9degC.$$

Therefore the maximum value of $(T_j - T_{mb})$ is 12.2degC from Eq. 5 .

Thus Eq. 3 becomes:

$$R_{th(h-a)} = \left(\frac{150 - 12.2 - 60}{2}\right) - 1 \quad = 37.9degC/W.$$

Therefore the maximum value of $(T_j - T_{mb})$ is 12.2 degC from Eq. 5.

Therefore heatsinks used for the BD131 transistors in this application should each have a thermal resistance of 37degC/W or less. The foregoing calculations assume a contact thermal resistance value of 1degC/W, which is true only if a heat-sink mounting compound is used.

APPENDIX I
Transistor heatsink sizes

The heatsink size for any transistor can be found from the nomogram shown in Fig. 14 provided that the power dissipation is no greater than 100W, and that the heat is dissipated by free convection. This nomogram should not be used where forced air cooling is employed, or where heatsink material other than aluminium is desired. The nomogram is operated as follows, with reference to the simplified curves in Fig. 15.

1) Calculate the worst-case dissipation $P_{tot}max$ and hence the thermal resistance of heatsink to ambient $R_{th}(h-a)$. Thus:

$$R_{th(h-a)} = \frac{T_{mb}max - T_{amb}}{P_{tot}} - R_{th(mb-h)}$$

2) Enter the nomogram in section I of Fig. 15. Move horizontally to the left until the appropriate orientation (either horizontal or vertical) and the appropriate surface finish is reached.
3) Move vertically upwards to intersect appropriate power dissipation curve (P_{tot}) in section II.
4) Move horizontally to intersect the curve in section III for the desired thickness of sheet aluminium heatsink. If an extrusion is required, move vertically upwards

from the point of intersection on the chosen extrusion curve and read off the required length on the top horizontal scale. (The 30D and 40D are shown in outline in Fig. 16. These types belong to the family of extrusions which has been used with Mullard power devices requiring special heatsink considerations, such as thyristor stacks and power rectifiers. Similar curves for alternative extrusions could also be plotted in section III using the heatsink manufacturer's data relating $R_{th(h-a)}$ and power, and length).

5) Move vertically down from point A in section III to intersect with the appropriate curve for the transistor encapsulation style.
6) Move horizontally to the left and read off the required area of one side of flat aluminium heatsink.
7) The heatsink dimensions of height to width should not exceed the ratio 1·25:1.

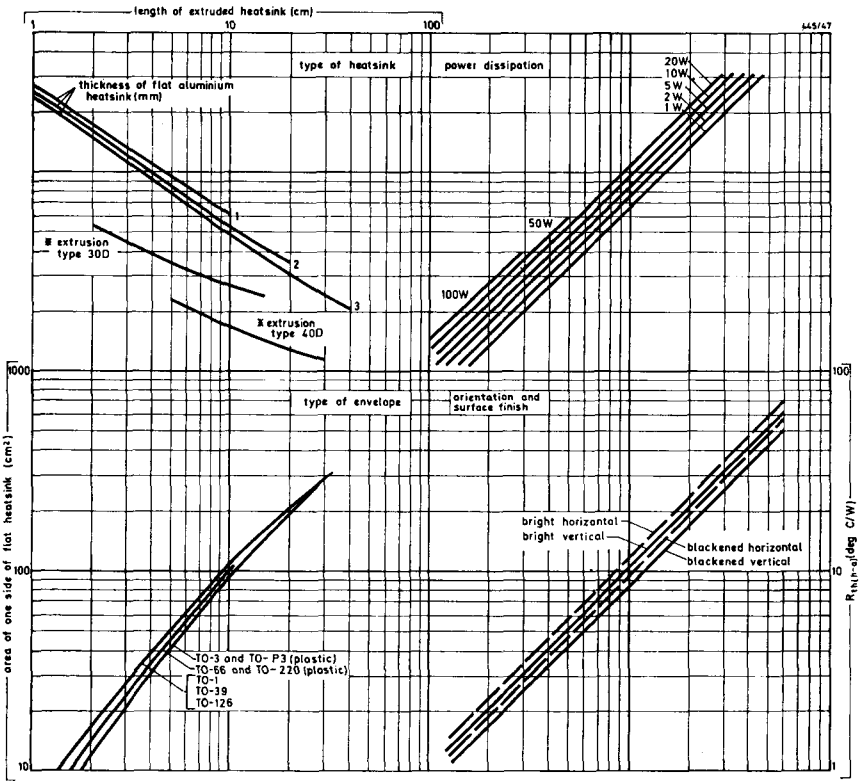


Fig. 14—Heatsink nomogram. *(For outlines of extrusions see Fig. 16.)

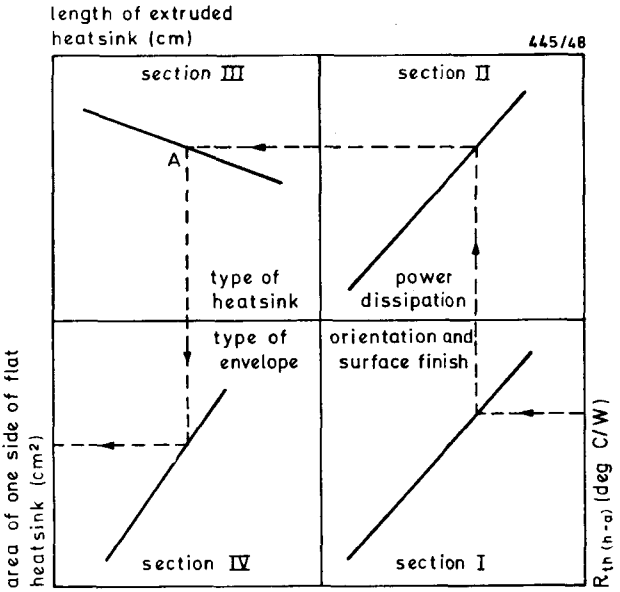


Fig. 15—Simplified nomogram

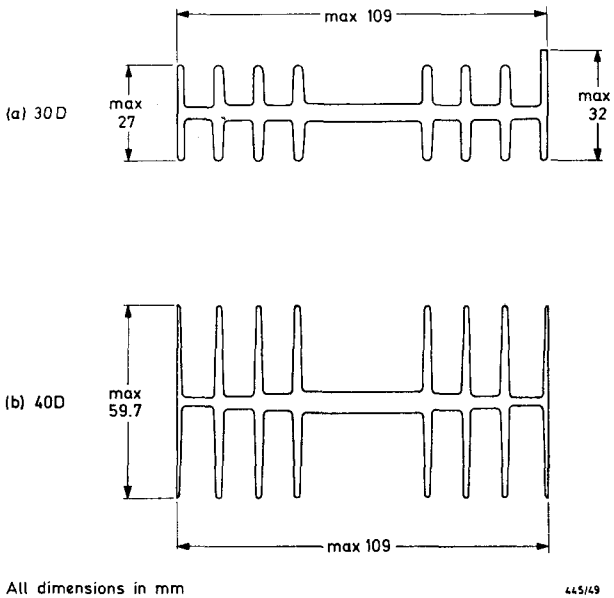


Fig.16—Outlines of extrusions: (a) 30D, (b) 40D

TRANSISTORS

B

DUAL N-CHANNEL FIELD EFFECT TRANSISTORS

BFQ10 to BFQ16

Dual n-channel silicon planar epitaxial junction field-effect transistors in TO-71 metal envelope, with electrically insulated gates and a common substrate connected to the envelope; intended for high performance low level differential amplifiers.

QUICK REFERENCE DATA

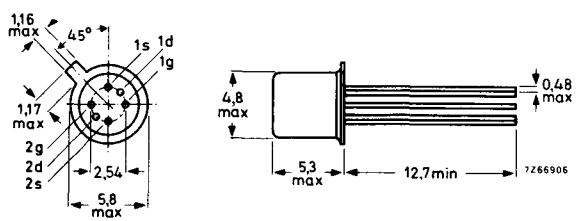
Characteristics measured at T_{amb} = 25 °C; I_D = 200 μA; V_{DG} = 15 V

			BFQ10	11	12	13	14	15	16	
Difference in gate current	$\lvert\Delta I_G\rvert$	<	10	10	10	10	10	10	10	pA
Gate-source voltage difference	$\lvert\Delta V_{GS}\rvert$	<	5	10	10	10	15	20	50	mV
Thermal drift of gate-source voltage difference	$\lvert\frac{d\,\Delta V_{GS}}{dT}\rvert$	<	5	5	10	20	20	40	50	μV/°C
Transfer conductance ratio	$\frac{g_{1fs}}{g_{2fs}}$	>	0,98	0,98	0,98	0,98	0,98	0,95	0,95	
		<	1,02	1,02	1,02	1,02	1,02	1,05	1,05	
Difference in transfer impedance	$\lvert\Delta\frac{1}{g_{fs}}\rvert$	<	6	6	12	12	12	20	30	Ω
Difference in penetration factor	$\lvert\Delta\frac{g_{os}}{g_{fs}}\rvert$	<	10	30	30	30	30	30	100	μV/V
Common mode rejection ratio	CMRR	>	100	90	90	90	90	90	80	dB

MECHANICAL DATA

Dimensions in mm

TO-71
All leads insulated
from the case



RATINGS Limiting values in accordance with the Absolute Maximum System

Voltages				
Drain-source voltage	$\pm V_{DS}$	max.	30	V
Drain-gate voltage (open source)	V_{DGO}	max.	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30	V
Voltage between gate 1 and gate 2	$\pm V_{1G-2G}$	max.	40	V
Currents				
Drain current	I_D	max.	30	mA
Gate current	I_G	max.	10	mA
Power dissipation				
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	250	mW
Temperatures				
Storage temperature	T_{stg}	−65 to +200		°C
Junction temperature	T_j	max.	200	°C
THERMAL RESISTANCE				
From junction to ambient in free air	$R_{th\ j-a}$	=	0,5	°C/mW

CHARACTERISTICS (total device) $T_{amb} = 25\ ^{o}C$ unless otherwise specified

Measured at: $I_D = 200\ \mu A$; $V_{DG} = 15\ V$ except for drain current ratio.

			BFQ10	11	12	13	14	15	16	
Drain current ratio [1]										
$V_{DG} = 15\ V$; $V_{GS} = 0$	$\frac{I_{1D\text{-}1SS}}{I_{2D\text{-}2SS}}$	>	0,97	0,95	0,95	0,95	0,92	0,90	0,80	
		<	1,03	1,05	1,05	1,05	1,08	1,10	1,20	
Difference in gate current	$\lvert\Delta I_G\rvert$	<	10	10	10	10	10	10	10	pA
Gate-source voltage difference	$\lvert\Delta V_{GS}\rvert$	<	5	10	10	10	15	20	50	mV
Thermal drift of gate-source voltage difference	$\left\lvert\frac{d\,\Delta V_{GS}}{dT}\right\rvert$	<	5	5	10	20	20	40	50	$\mu V/^{o}C$
Transfer conductance ratio	$\frac{g_{1fs}}{g_{2fs}}$	>	0,98	0,98	0,98	0,98	0,98	0,95	0,95	
		<	1,02	1,02	1,02	1,02	1,02	1,05	1,05	
Difference in transfer impedance [2]	$\left\lvert\Delta\frac{1}{g_{fs}}\right\rvert$	<	6	6	12	12	12	20	30	Ω
Difference in penetration factor [3]	$\left\lvert\Delta\frac{g_{os}}{g_{fs}}\right\rvert$	<	10	30	30	30	30	30	100	μV/V
Common mode rejection ratio [4]	CMRR	>	100	90	90	90	90	90	80	dB

1) Measured under pulse conditions.

2) The difference in transfer impedance is equal to the ratio of the change of the gate-source voltage difference to the change of drain current, at constant drain-gate voltage.

$\left(\Delta\frac{1}{g_{fs}} = \frac{d\,\Delta V_{GS}}{d\,I_D}\right.$ at $\left.V_{DG} = \text{constant}\right)$

3) The difference in penetration factor is equal to the ratio of the change of the gate-source voltage difference to the change of drain-gate voltage, at constant drain current.

$\left(\Delta\frac{g_{os}}{g_{fs}} = \frac{d\,\Delta V_{GS}}{d\,V_{DG}}\right.$ at $\left.I_D = \text{constant}\right)$

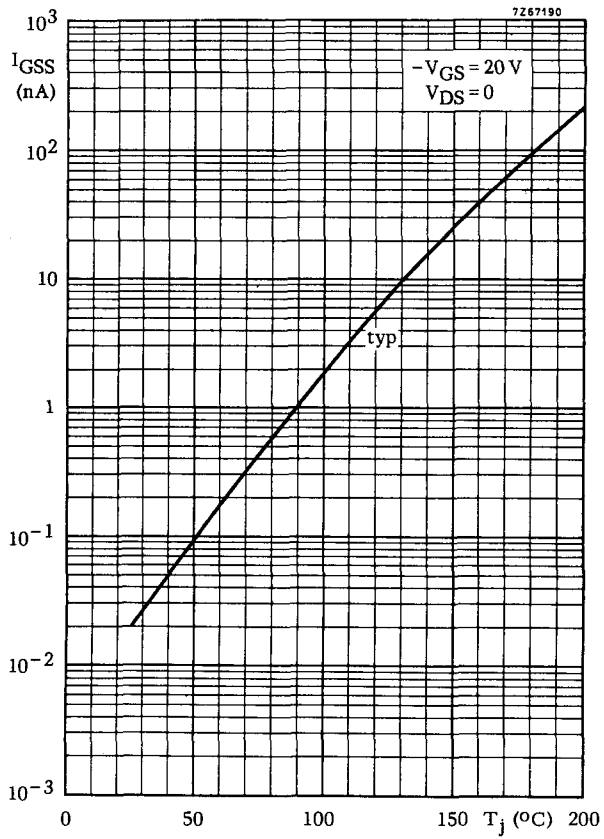
4) Common mode rejection ratio

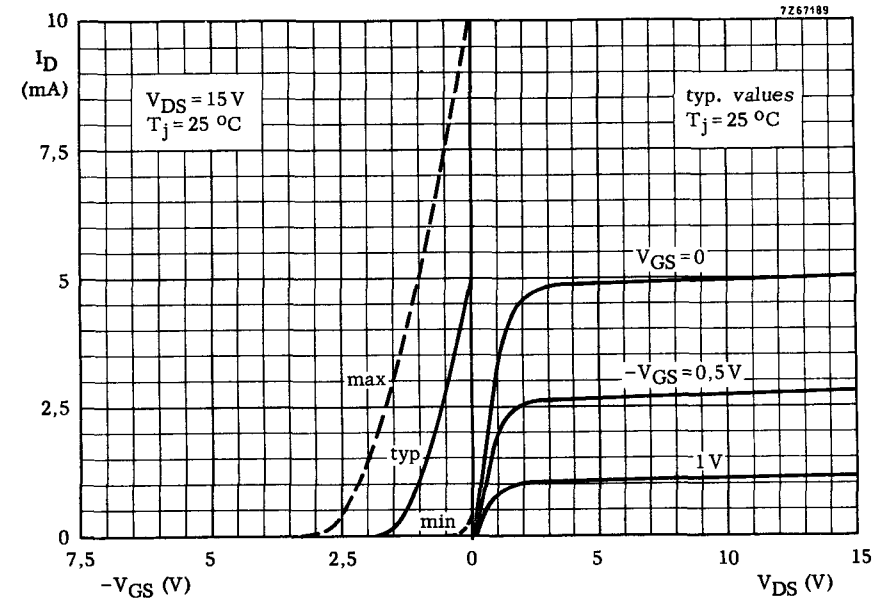
$\text{CMRR (in dB)} = -20\log\left\lvert\Delta\frac{g_{os}}{g_{fs}}\right\rvert$

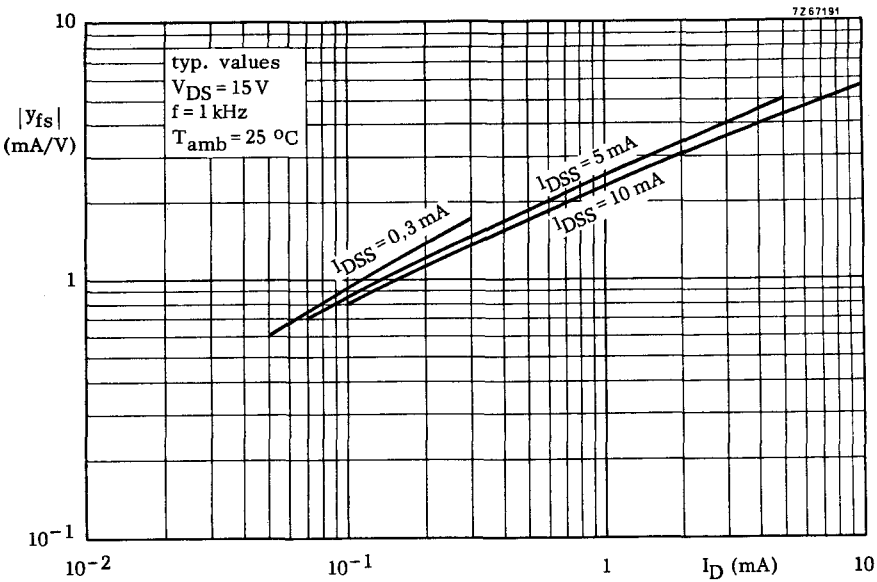
CHARACTERISTICS (Individual transistor) T_{amb} = 25 °C unless otherwise specified

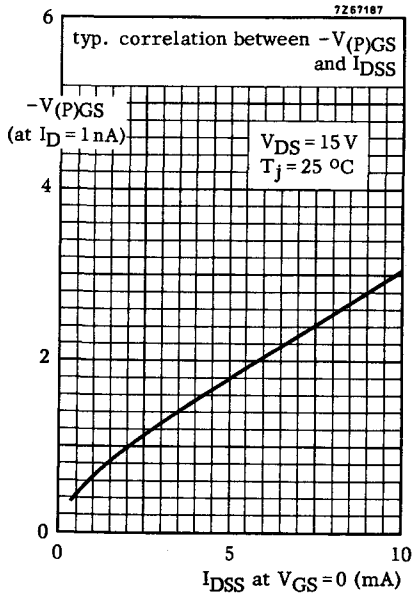
Gate cut-off current				
$-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	<	100	pA
$-V_{GS}$ = 20 V; V_{DS} = 0; T_{amb} = 125 °C	$-I_{GSS}$	<	20	nA
Gate current				
I_D = 200 µA; V_{DG} = 15 V; T_{amb} = 125 °C	I_G	<	10	nA
Drain current				
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	0,5 to 10		mA [1]
Gate-source voltage				
I_D = 200 µA; V_{DG} = 15 V	$-V_{GS}$	<	2,7	V
Gate-source cut-off voltage				
I_D = 1 nA; V_{DG} = 15 V	$-V_{(P)GS}$	0,5 to 3,5		V
Transfer conductance at f = 1 kHz				
I_D = 200 µA; V_{DG} = 15 V	g_{fs}	>	1,0	mA/V
Output conductance at f = 1 kHz				
I_D = 200 µA; V_{DG} = 15 V	g_{os}	<	5	µA/V
Input capacitance at f = 1 MHz				
I_D = 200 µA; V_{DG} = 15 V	C_{is}	<	8	pF [2]
Feedback capacitance at f = 1 MHz				
I_D = 200 µA; V_{DG} = 15 V	C_{rs}	<	1,0	pF [2]
Equivalent noise voltage				
I_D = 200 µA; V_{DS} = 15 V B = 0,6 to 100 Hz	V_n	<	0,5	µV

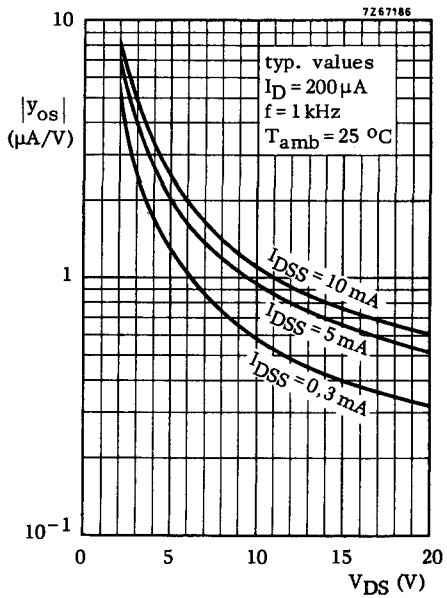
1) Measured under pulse conditions.
2) Measured with case grounded.

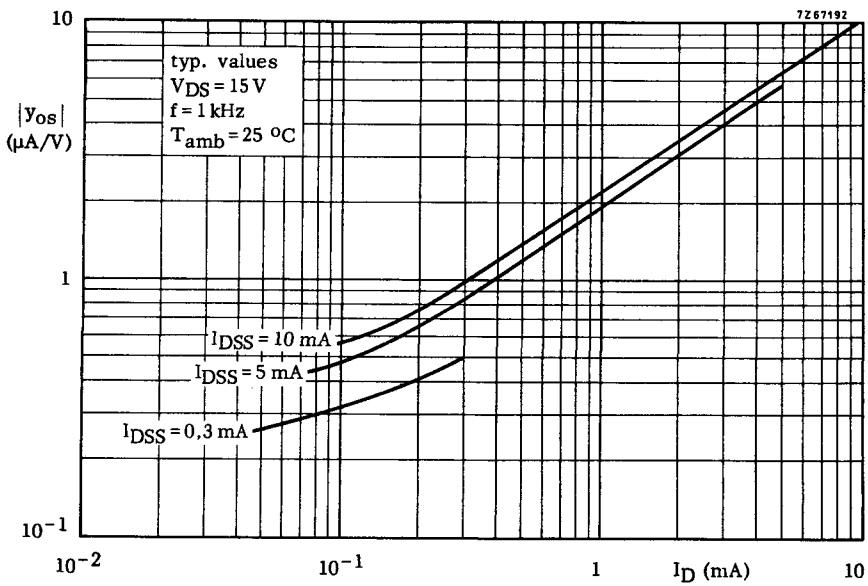

7Z67190
10^3
I_{GSS}
(nA)
10^2
10
1
10^{-1}
10^{-2}
10^{-3}
$-V_{GS} = 20\ V$
$V_{DS} = 0$
typ
0
50
100
150
T_j (°C)
200

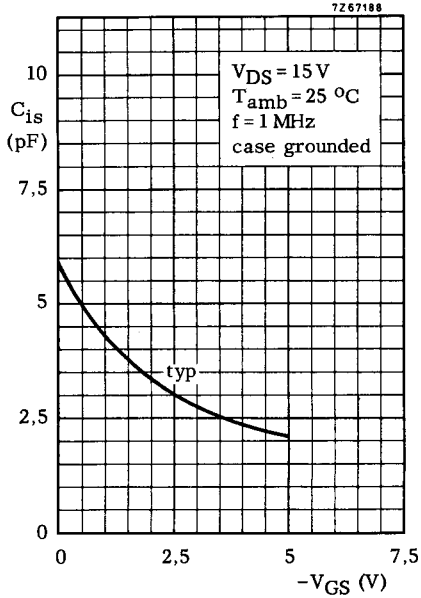

7Z67189
10
I_D (mA)
7,5
5
2,5
0
V_{DS} = 15 V
T_j = 25 °C
typ. values
T_j = 25 °C
V_{GS} = 0
$-V_{GS}$ = 0,5 V
1 V
max
typ
min
7,5
5
2,5
0
5
10
15
$-V_{GS}$ (V)
V_{DS} (V)

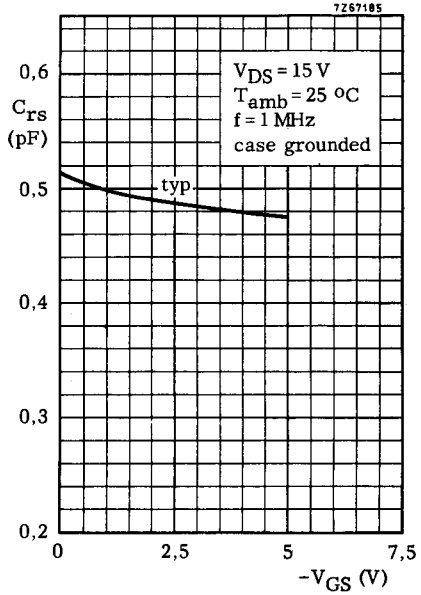

7Z67191
10
1
10^{-1}
$|y_{fs}|$ (mA/V)
typ. values
V_{DS} = 15 V
f = 1 kHz
T_{amb} = 25 °C
I_{DSS} = 0,3 mA
I_{DSS} = 5 mA
I_{DSS} = 10 mA
10^{-2}
10^{-1}
1
10
I_D (mA)

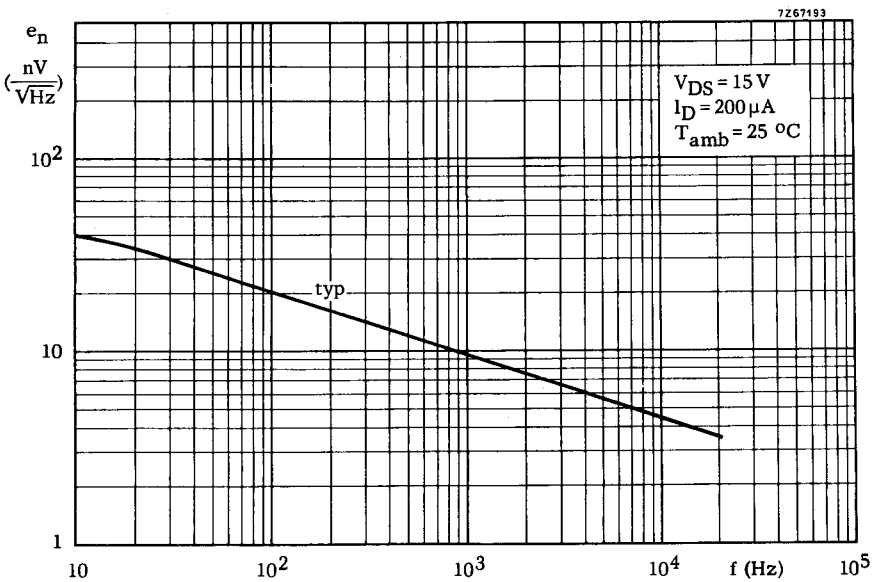

7Z67187
typ. correlation between $-V_{(P)GS}$ and I_{DSS}
$-V_{(P)GS}$ (at I_D = 1 nA)
V_{DS} = 15 V
T_j = 25 °C
6
4
2
0
0
5
10
I_{DSS} at V_{GS} = 0 (mA)


7Z67186
typ. values
I_D = 200 µA
f = 1 kHz
T_{amb} = 25 °C
$|y_{os}|$ (µA/V)
10
1
10^{-1}
I_{DSS} = 10 mA
I_{DSS} = 5 mA
I_{DSS} = 0,3 mA
0
5
10
15
20
V_{DS} (V)


7Z67192
typ. values
V_{DS} = 15 V
f = 1 kHz
T_{amb} = 25 °C
$|y_{os}|$ (µA/V)
10
1
10^{-1}
I_{DSS} = 10 mA
I_{DSS} = 5 mA
I_{DSS} = 0,3 mA
10^{-2}
10^{-1}
1
I_D (mA)
10


7Z67188
10
C_{is} (pF)
7,5
5
2,5
0
V_{DS} = 15 V
T_{amb} = 25 °C
f = 1 MHz
case grounded
typ
0
2,5
5
7,5
$-V_{GS}$ (V)


7Z67185
0,6
C_{rs} (pF)
0,5
0,4
0,3
0,2
V_{DS} = 15 V
T_{amb} = 25 °C
f = 1 MHz
case grounded
typ
0
2,5
5
7,5
$-V_{GS}$ (V)


7Z67193
e_n
$(\frac{nV}{\sqrt{Hz}})$
10^2
10
1
V_{DS} = 15 V
I_D = 200 µA
T_{amb} = 25 °C
typ
10
10^2
10^3
10^4
f (Hz)
10^5

N-CHANNEL INSULATED GATE FIELD EFFECT TRANSISTOR

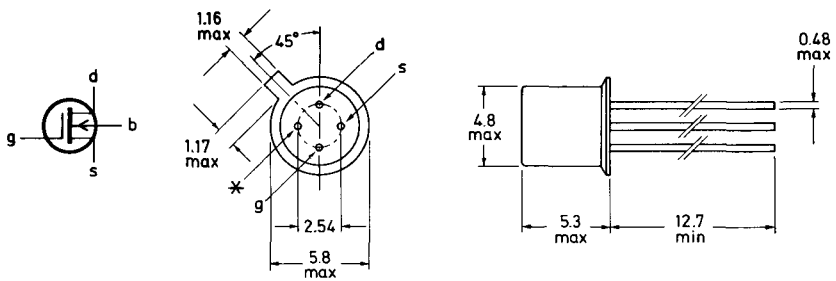
BFR29

Depletion type, insulated gate, field effect transistor in a TO-72 metal envelope with the substrate connected to the case. It is intended for linear applications in the audio as well as the i.f. and v.h.f. frequency region, and in cases where high input impedance, low gate leakage currents and low noise figures are of importance.

QUICK REFERENCE DATA		
V_{DB} max.	30	V
$\pm V_{GB}$ max.	10	V
I_{DSS} (V_{DS} = 15V, V_{GS} = 0)	10 to 40	mA
$\lvert y_{fs} \rvert$ min. (I_D = 5mA, V_{DS} = 15V, f = 1kHz)	6.0	mA/V
$-C_{rs}$ max. (I_D = 5mA, V_{DS} = 15V, f = 1MHz)	0.7	pF
N max. (I_D = 5mA, V_{DS} = 15V, f = 200MHz, G_S = 1mA/V, B_S = optimum)	5.0	dB
$V_n/\sqrt{B}$ typ. (I_D = 5mA, V_{DS} = 15V, f = 1kHz)	100	nV/$\sqrt{Hz}$

OUTLINE AND DIMENSIONS

Conforms to BS 3934 SO-12A/SB4-3
J.E.D.E.C. TO-72



* Substrate connected to envelope

All dimensions in mm

D3925

NOTE

To exclude the possibility of damage to the gate oxide layer by an electrostatic charge building up on the high resistance gate electrode, the device is fitted with a conductive rubber ring around the leads. This ring should not be removed until after the device has been mounted in the circuit.

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{DB} max.	Drain-substrate voltage	30	V
V_{SB} max.	Source-substrate voltage	30	V
$\pm V_{GB}$ max.	Gate-substrate voltage (continuous)	10	V
$\pm V_{G-N}$ max.	Repetitive peak gate voltage (gate to all other terminals) $V_{SB}=V_{DB}=0$, $f>100Hz$	15	V
I_D max.	Drain current (d.c.)	20	mA
I_{DM} max.	Peak drain current $t_r=20ms$, $d=0.1$	50	mA
P_{tot} max.	Total power dissipation $T_{amb}\leq 25^oC$	200	mW

Temperature

T_{stg}	Storage temperature	-65 to +125	^oC
T_j max.	Junction temperature	125	^oC

THERMAL CHARACTERISTIC

$R_{th(j-amb)}$	Thermal resistance, junction to ambient, in free air	0.5	degC/mW

ELECTRICAL CHARACTERISTICS ($T_j=25^oC$ unless otherwise stated)

		Min.	Typ.	Max.	
	Gate current, $V_{BS}=0$				
$-I_{GSS}$	$-V_{GS}=10V$, $V_{DS}=0$	-	-	10	pA
I_{GSS}	$V_{GS}=10V$, $V_{DS}=0$	-	-	10	pA
$-I_{GSS}$	$-V_{GS}=10V$, $V_{DS}=0$, $T_j=125^oC$	-	-	200	pA
I_{GSS}	$V_{GS}=10V$, $V_{DS}=0$, $T_j=125^oC$	-	-	200	pA
	Substrate current, $V_{GB}=0$				
$-I_{BDO}$	$-V_{BD}=30V$, $I_S=0$	-	-	10	μA
$-I_{BSO}$	$-V_{BS}=30V$, $I_D=0$	-	-	10	μA
I_{DSS}	Drain current $V_{DS}=15V$, $V_{GS}=0$	10	-	40	mA
$-V_{GS}$	Gate-source voltage $I_D=100nA$, $V_{DS}=15V$	0.5	-	3.5	V

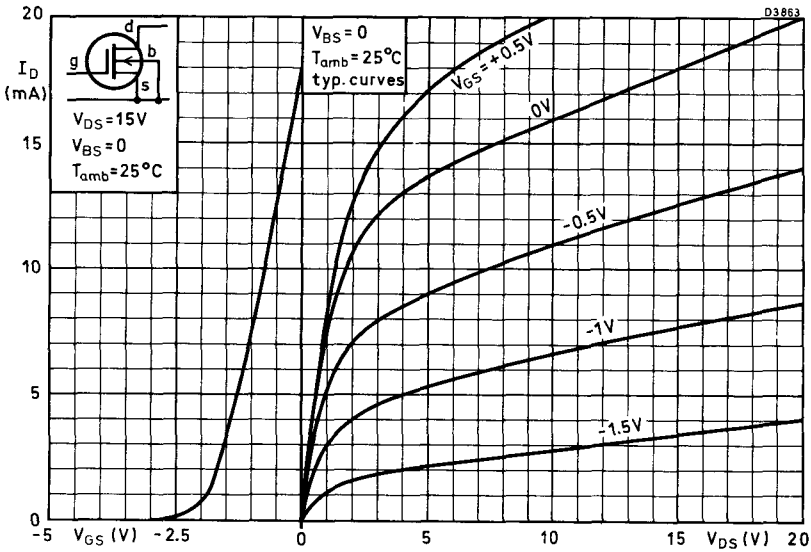
ELECTRICAL CHARACTERISTICS (contd.)

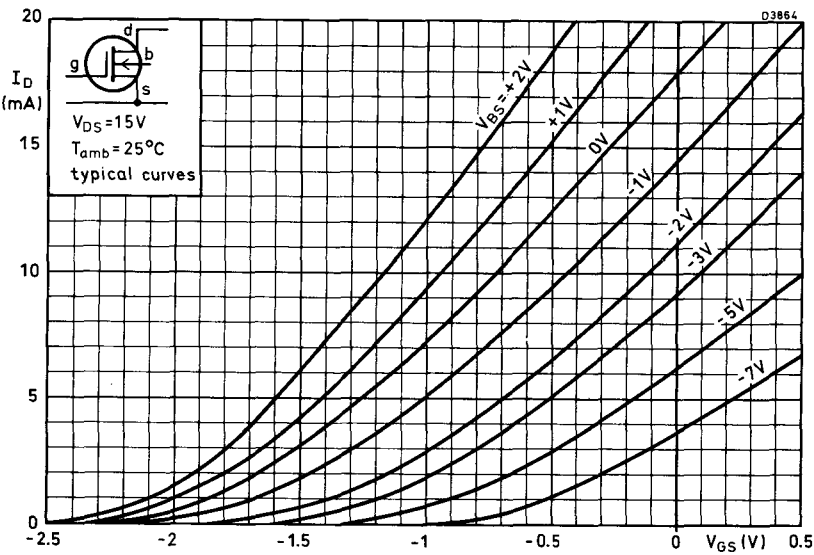
		Min.	Typ.	Max.	
$-V_{(P)GS}$	Gate-source cut-off voltage $I_D = 100nA$, $V_{DS} = 15V$	-	-	4.0	V
N	Noise figure at f = 200MHz $I_D = 5mA$, $V_{DS} = 15V$, $T_{amb} = 25^oC$ $G_S = 1mA/V$, B_S = optimum	-	-	5.0	dB
$V_n/\sqrt{B}$	Equivalent noise voltage, $T_{amb} = 25^oC$				
	$I_D = 5mA$, $V_{DS} = 15V$, f = 120Hz	-	300	-	$nV/\sqrt{Hz}$
	f = 1kHz	-	100	-	$nV/\sqrt{Hz}$
	f = 10kHz	-	35	-	$nV/\sqrt{Hz}$

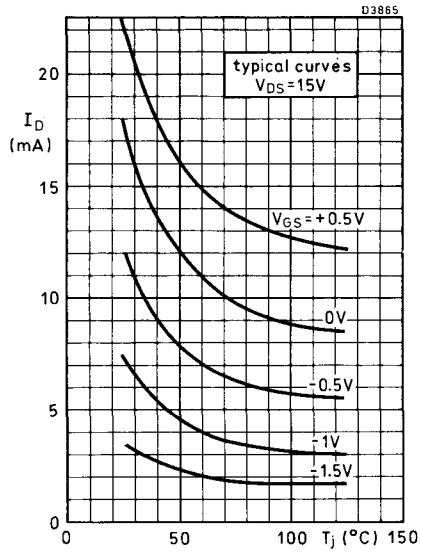
y-parameters

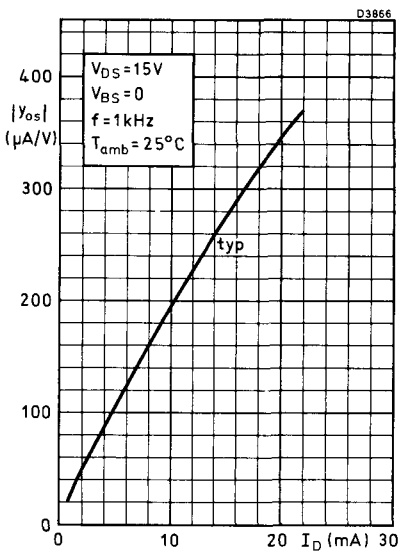
$I_D = 5mA$, $V_{DS} = 15V$, $T_{amb} = 25^oC$

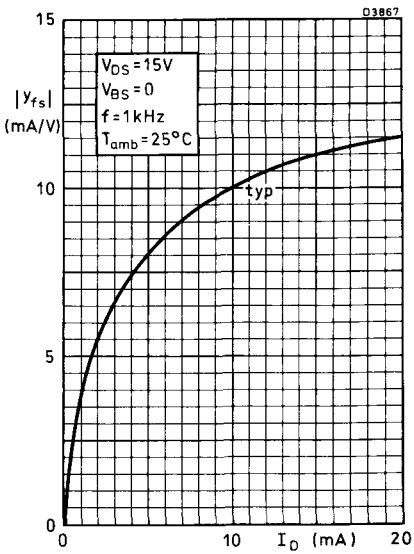
$\|y_{fs}\|$	Transfer admittance at f = 1kHz	6.0	-	-	mA/V
$\|y_{os}\|$	Output admittance at f = 1kHz	-	-	0.4	mA/V
C_{is}	Input capacitance at f = 1MHz	-	-	5.0	pF
$-C_{rs}$	Feedback capacitance at f = 1MHz	-	-	0.7	pF
C_{os}	Output capacitance at f = 1MHz	-	-	3.0	pF

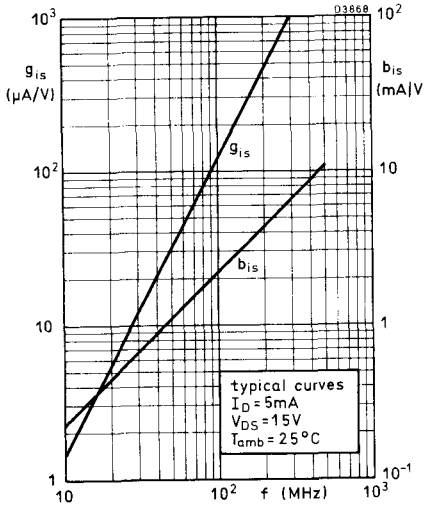

D3863
I_D (mA)
V_{DS}=15V
V_{BS}=0
T_{amb}=25°C
V_{BS}=0
T_{amb}=25°C
typ. curves
V_{GS}=+0.5V
0V
-0.5V
-1V
-1.5V
V_{GS} (V)
V_{DS} (V)

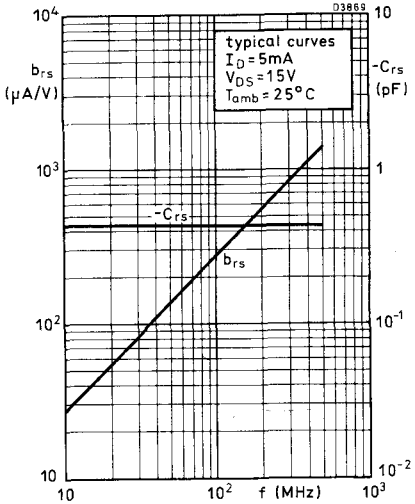

D3864
I_D (mA)
V_{DS}=15V
T_{amb}=25°C
typical curves
V_{BS}=+2V
+1V
0V
-1V
-2V
-3V
-5V
-7V
V_{GS} (V)

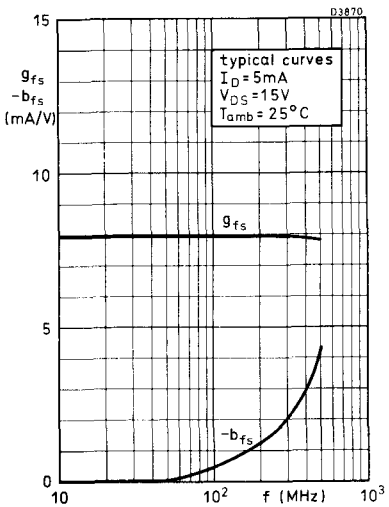

D3865
typical curves
V_{DS}=15V
I_D (mA)
20
15
10
5
0
V_{GS}=+0.5V
0V
-0.5V
-1V
-1.5V
0
50
100
T_j (°C)
150

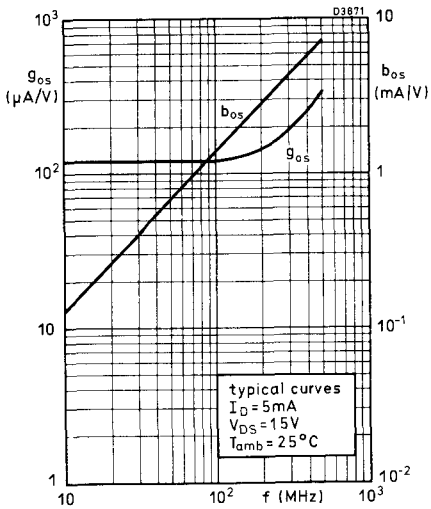

D3866
V_{DS}=15V
V_{BS}=0
f=1kHz
T_{amb}=25°C
$|Y_{os}|$ (μA/V)
400
300
200
100
0
typ
0
10
20
I_D (mA)
30

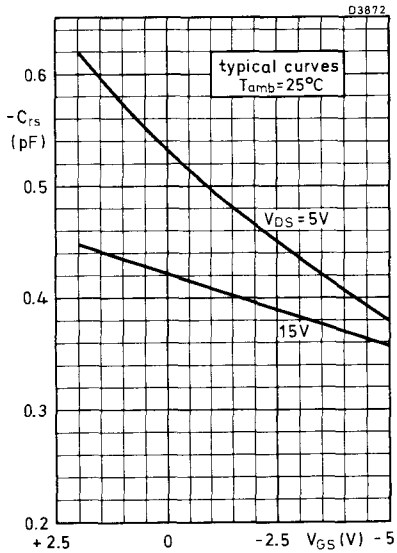

D3867
V_{DS}=15V
V_{BS}=0
f=1kHz
T_{amb}=25°C
$|Y_{fs}|$ (mA/V)
15
10
5
0
typ
0
10
I_D (mA)
20

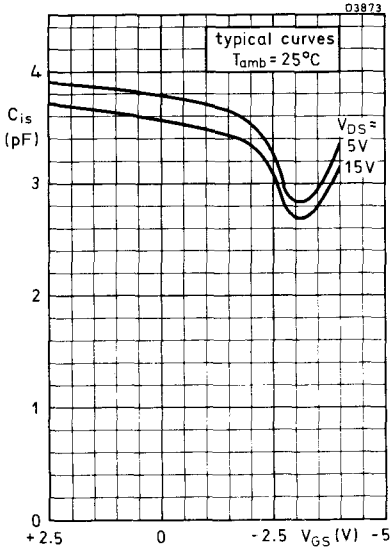

D3868
g_{is} (μA/V)
b_{is} (mA/V)
g_{is}
b_{is}
typical curves
I_D = 5mA
V_{DS} = 15V
T_{amb} = 25°C
f (MHz)


D3869
b_{rs} (μA/V)
$-C_{rs}$ (pF)
typical curves
I_D = 5mA
V_{DS} = 15V
T_{amb} = 25°C
$-C_{rs}$
b_{rs}
f (MHz)


D3870
g_{fs} $-b_{fs}$ (mA/V)
typical curves
I_D = 5mA
V_{DS} = 15V
T_{amb} = 25°C
g_{fs}
$-b_{fs}$
f (MHz)


D3871
g_{os} (μA/V)
b_{os} (mA/V)
b_{os}
g_{os}
typical curves
I_D = 5mA
V_{DS} = 15V
T_{amb} = 25°C
f (MHz)


D3872
typical curves
Tamb = 25°C
-Crs (pF)
0.6
0.5
0.4
0.3
0.2
VDS = 5V
15V
+2.5
0
-2.5
VGS (V)
-5


D3873
typical curves
Tamb = 25°C
Cis (pF)
4
3
2
1
0
VDS = 5V
15V
+2.5
0
-2.5
VGS (V)
-5

μ min. N-CHANNEL SILICON FIELD EFFECT TRANSISTORS

BFR30
BFR31

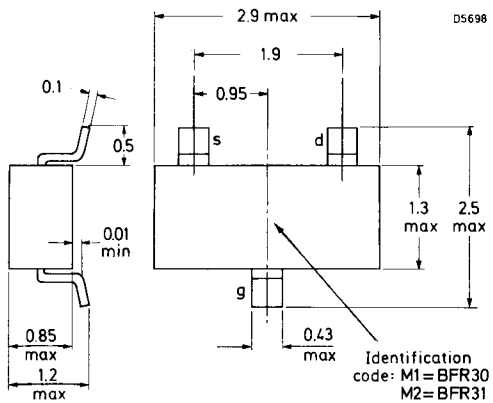
N-channel silicon planar epitaxial junction field effect transistors in microminiature encapsulation. They are intended for low-level general purpose amplifiers in thick and thin film circuits.

QUICK REFERENCE DATA

$\pm V_{DS}$	max.			25	V
$-V_{GSO}$	max.			25	V
P_{tot}	max. ($T_{amb} \leq 25^{o}C$)			200	mW
			BFR30	BFR31	
I_{DSS} (V_{DS} = 10V, V_{GS} = 0)		min.	4.0	1.0	mA
		max.	10	5.0	mA
$\|y_{fs}\|$ (I_D = 1mA, V_{DS} = 10V, f = 1kHz)		min.	1.0	1.5	mA/V
		max.	4.0	4.5	mA/V

Unless otherwise stated data are applicable to both types

OUTLINE AND DIMENSIONS



All dimensions in millimetres
Plan view from above

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

$\pm V_{DS}$	max.	Drain-source voltage	25	V
V_{DGO}	max.	Drain-gate voltage (open source)	25	V
$-V_{GSO}$	max.	Gate-source voltage (open drain)	25	V
I_D	max.	Drain current	10	mA
I_G	max.	Gate current	5.0	mA
P_{tot}	max.	Power dissipation ($T_{amb} \leq 25^oC$) mounted on a ceramic substrate of $7 \times 5 \times 0.5$mm	200	mW

Temperature

T_{stg}		Storage temperature	-65 to +150	^oC
T_j	max.	Junction temperature	150	^oC

THERMAL CHARACTERISTICS

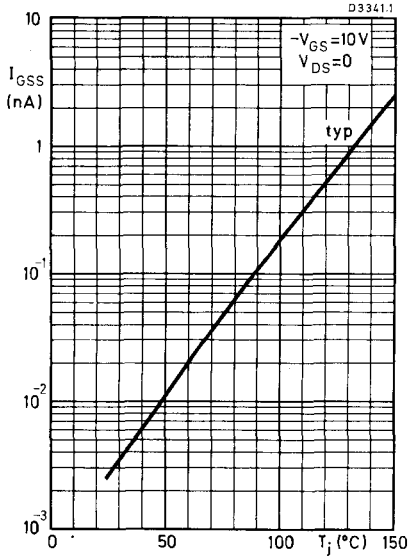
$R_{th(j-amb)}$	Thermal resistance between junction and ambient, the device mounted on a ceramic substrate of $7 \times 5 \times 0.5$mm	0.62	$^oC/mW$

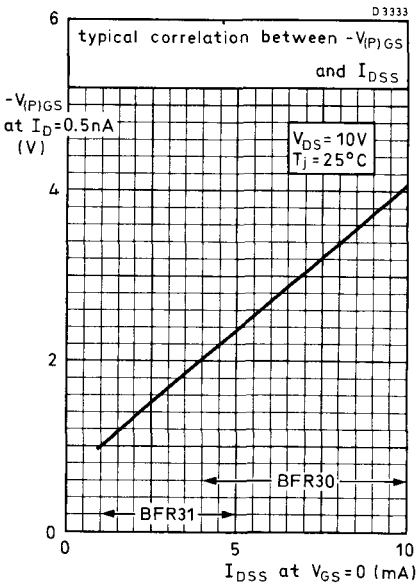
ELECTRICAL CHARACTERISTICS ($T_j = 25^oC$ unless otherwise stated)

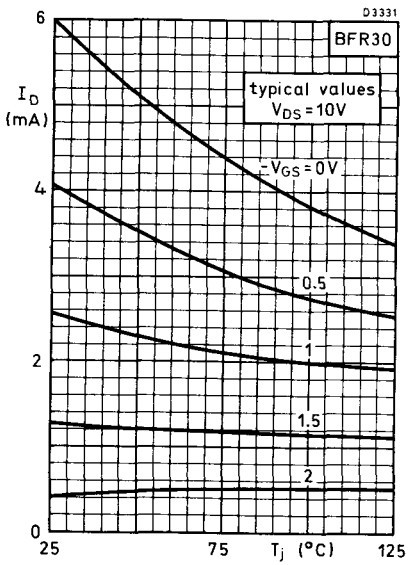
			Min.	Max.	
$-I_{GSS}$	Gate cut-off current $-V_{GS} = 10V$, $V_{DS} = 0$		-	0.2	nA
I_{DSS}	Drain current $V_{DS} = 10V$, $V_{GS} = 0$	BFR30	4.0	10	mA
		BFR31	1.0	5.0	mA
$-V_{GS}$	Gate-source voltage $I_D = 1mA$, $V_{DS} = 10V$	BFR30	0.7	3.0	V
		BFR31	0	1.3	V
	$I_D = 50\mu A$, $V_{DS} = 10V$	BFR30	-	4.0	V
		BFR31	-	2.0	V
$-V_{(P)GS}$	Gate-source cut-off voltage $I_D = 0.5nA$, $V_{DS} = 10V$	BFR30	-	5.0	V
		BFR31	-	2.5	V

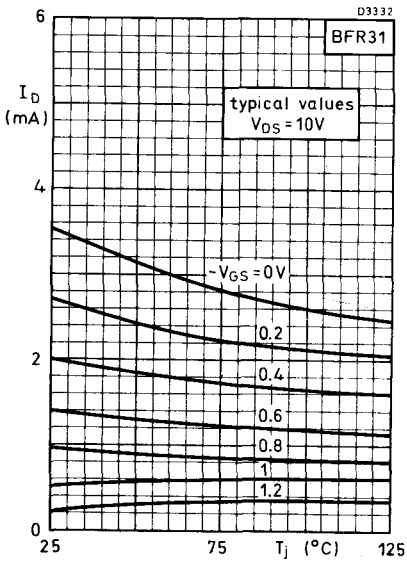
ELECTRICAL CHARACTERISTICS (contd.)

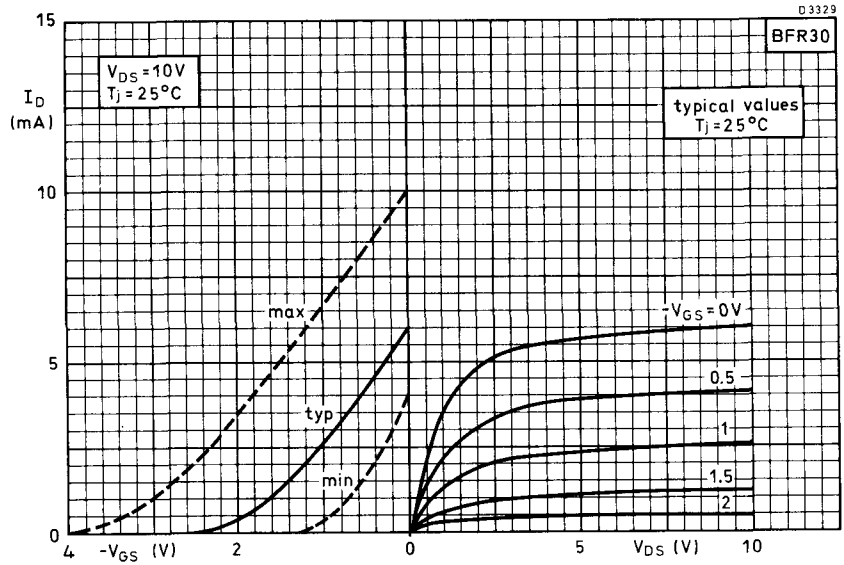
			Min.	Max.	
y-parameters, $T_{amb} = 25^{o}C$					
$\lvert y_{fs} \rvert$	Transfer admittance at f = 1kHz				
	I_D = 1mA, V_{DS} = 10V	BFR30	1.0	4.0	mA/V
		BFR31	1.5	4.5	mA/V
	I_D = 200μA, V_{DS} = 10V	BFR30	0.5	-	mA/V
		BFR31	0.75	-	mA/V
$\lvert y_{os} \rvert$	Output admittance at f = 1kHz				
	I_D = 1mA, V_{DS} = 10V	BFR30	-	40	μA/V
		BFR31	-	25	μA/V
	I_D = 200μA, V_{DS} = 10V	BFR30	-	20	μA/V
		BFR31	-	15	μA/V
C_{is}	Input capacitance at f = 1MHz				
	I_D = 1mA, V_{DS} = 10V		-	4.0	pF
	I_D = 200μA, V_{DS} = 10V		-	4.0	pF
C_{rs}	Feedback capacitance at f = 1MHz,				
	I_D = 1mA, V_{DS} = 10V, $T_{amb} = 25^{o}C$		-	1.5	pF
	I_D = 200μA, V_{DS} = 10V, $T_{amb} = 25^{o}C$		-	1.5	pF
V_n	Equivalent noise voltage				
	I_D = 200μA, V_{DS} = 10V				
	B = 0.6 to 100Hz		-	0.5	μV

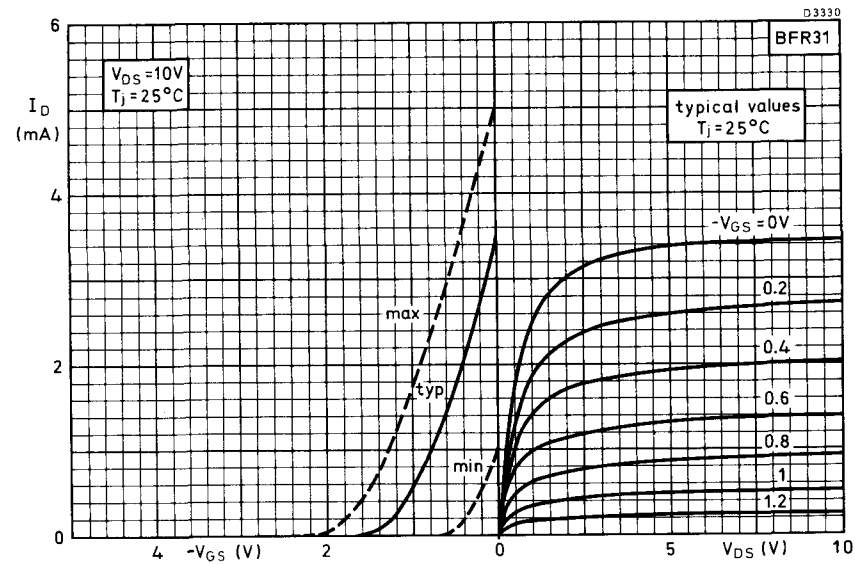

D3341.1
10
I_{GSS} (nA)
1
10^{-1}
10^{-2}
10^{-3}
$-V_{GS}$=10V
V_{DS}=0
typ
0
50
100
T_j (°C)
150

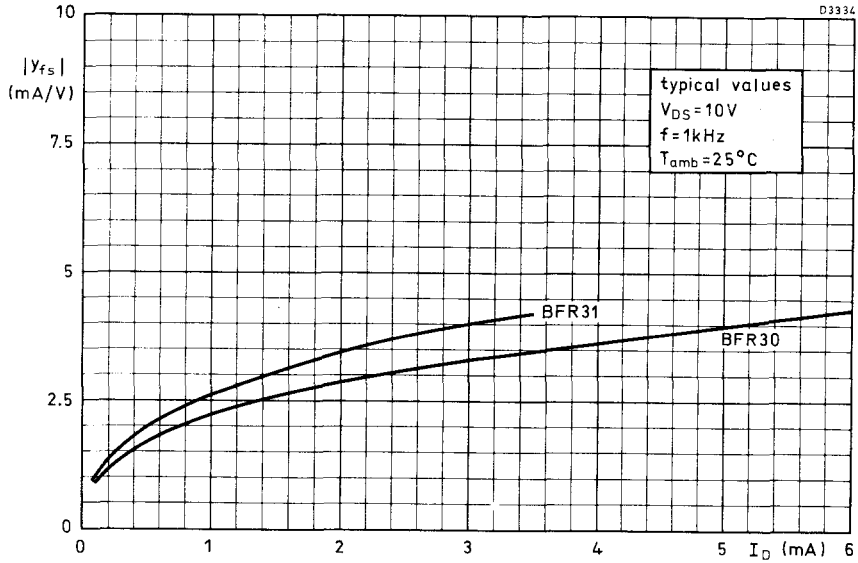

D3333
typical correlation between $-V_{(P)GS}$ and I_{DSS}
$-V_{(P)GS}$ at I_D=0.5nA (V)
V_{DS}= 10V
T_j = 25°C
BFR30
BFR31
0
2
4
6
0
5
10
I_{DSS} at V_{GS}=0 (mA)

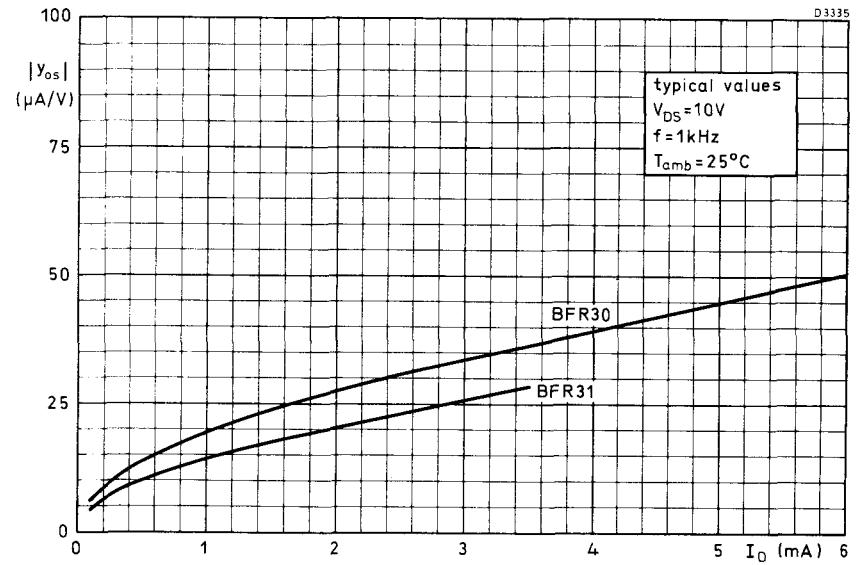

D3331
BFR30
typical values
V_{DS}=10V
I_D (mA)
$-V_{GS}$=0V
0.5
1
1.5
2
0
2
4
6
25
75
T_j (°C)
125

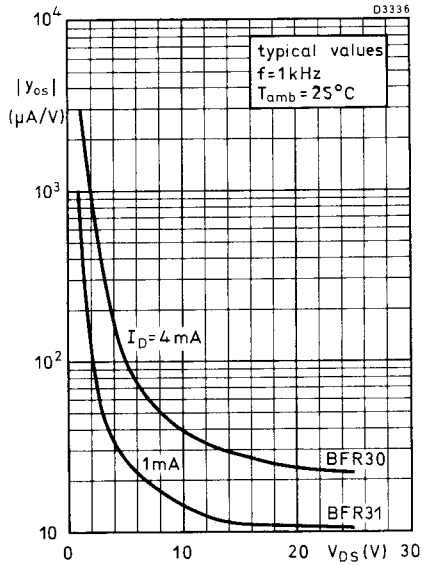

D3332
BFR31
typical values
V_{DS}=10V
I_D (mA)
$-V_{GS}$=0V
0.2
0.4
0.6
0.8
1
1.2
0
2
4
6
25
75
T_j (°C)
125

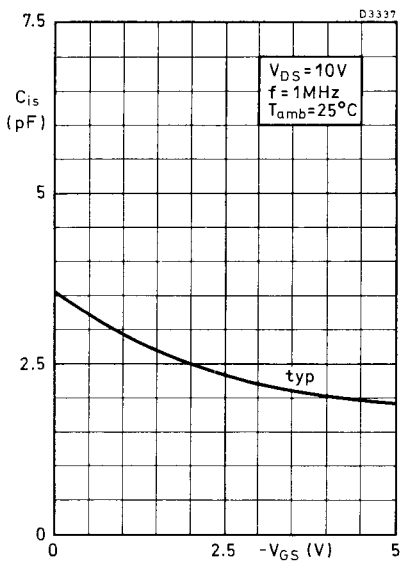

D3329
BFR30
V_{DS} = 10V
T_j = 25°C
typical values
T_j = 25°C
I_D (mA)
15
10
5
0
max
typ
min
$-V_{GS}$ = 0V
0.5
1
1.5
2
4
$-V_{GS}$ (V)
2
0
5
V_{DS} (V)
10

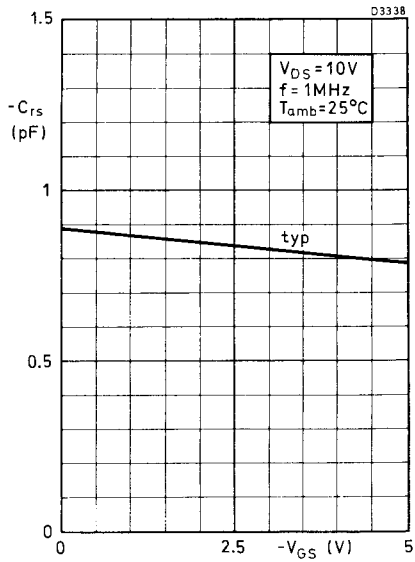

D3330
BFR31
V_{DS} = 10V
T_j = 25°C
typical values
T_j = 25°C
I_D (mA)
6
4
2
0
max
typ
min
$-V_{GS}$ = 0V
0.2
0.4
0.6
0.8
1
1.2
4
$-V_{GS}$ (V)
2
0
5
V_{DS} (V)
10

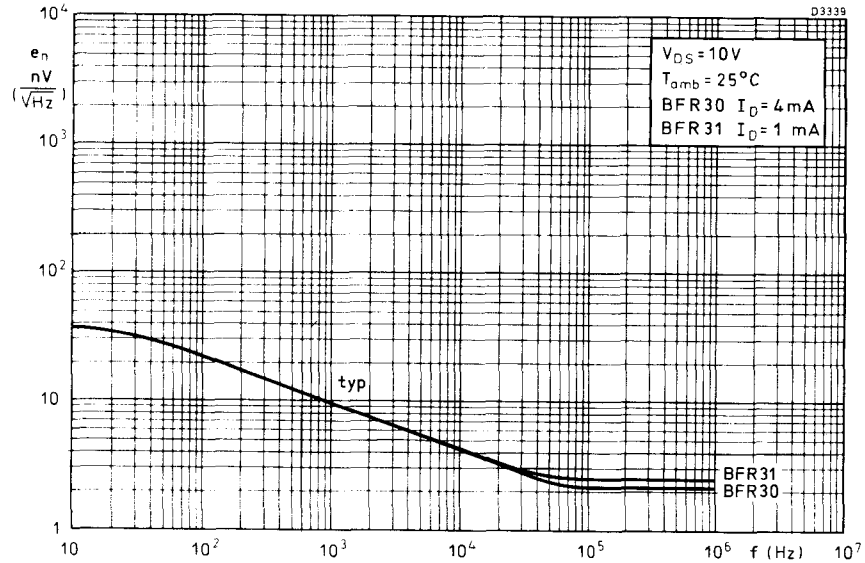

D3334
$|y_{fs}|$ (mA/V)
typical values
V_{DS} = 10V
f = 1kHz
T_{amb} = 25°C
BFR31
BFR30
10
7.5
5
2.5
0
0
1
2
3
4
5
I_D (mA)
6

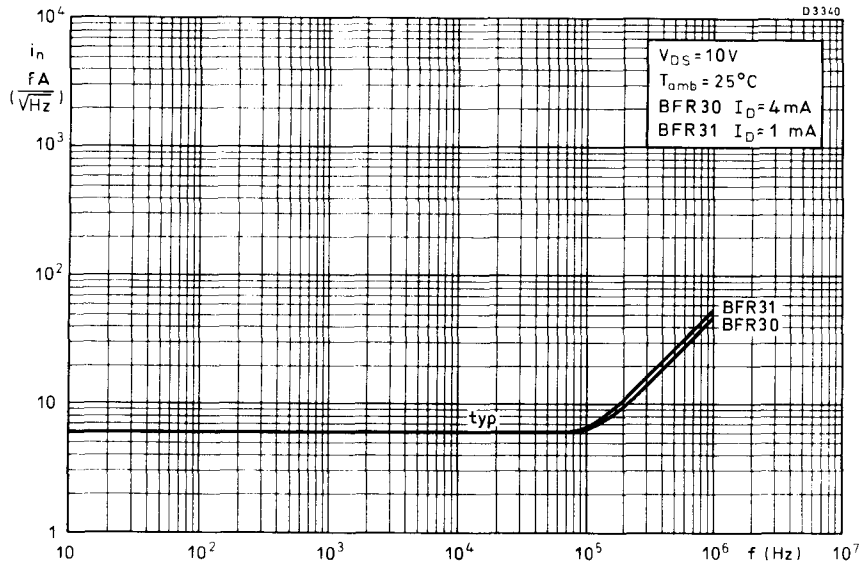

D3335
$|y_{os}|$ (μA/V)
typical values
V_{DS} = 10V
f = 1kHz
T_{amb} = 25°C
BFR30
BFR31
100
75
50
25
0
0
1
2
3
4
5
I_D (mA)
6


D3336
typical values
f=1kHz
Tamb=25°C
|yos|
(μA/V)
10⁴
10³
10²
10
ID=4mA
1mA
BFR30
BFR31
0
10
20
VDS(V)
30


D3337
VDS=10V
f=1MHz
Tamb=25°C
Cis
(pF)
7.5
5
2.5
0
typ
0
2.5
-VGS (V)
5


D3338
VDS=10V
f=1MHz
Tamb=25°C
-Crs
(pF)
1.5
1
0.5
0
typ
0
2.5
-VGS (V)
5


D3339
e_n
nV
$(\frac{}{\sqrt{Hz}})$
10^4
10^3
10^2
10
1
V_{DS} = 10V
T_{amb} = 25°C
BFR30 I_D = 4mA
BFR31 I_D = 1 mA
typ
BFR31
BFR30
10
10^2
10^3
10^4
10^5
10^6
f (Hz)
10^7


D3340
i_n
fA
$(\frac{}{\sqrt{Hz}})$
10^4
10^3
10^2
10
1
V_{DS} = 10V
T_{amb} = 25°C
BFR30 I_D = 4mA
BFR31 I_D = 1 mA
BFR31
BFR30
typ
10
10^2
10^3
10^4
10^5
10^6
f (Hz)
10^7

N-P-N SILICON PLANAR EPITAXIAL TRANSISTORS

BFR63
BFR64

N-P-N multi-emitter silicon transistors in capstan envelopes. The transistors have extremely good intermodulation properties and high power gain.

The devices are intended for:

(a) Final and driver stages of channel and band aerial amplifiers with high output power for band I, II, III and IV/V (40 to 860MHz).

(b) Final and driver stages of wideband amplifiers (40 to 230MHz).

(c) Final stages of the wideband vertical amplifier in high speed oscilloscopes.

(d) Frequency multiplier and oscillator circuits.

QUICK REFERENCE DATA

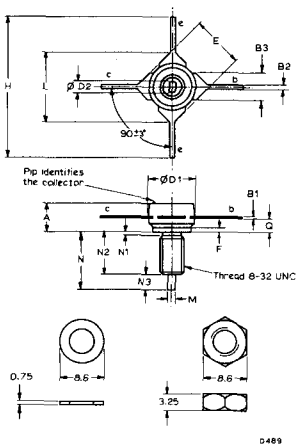
V_{CBOM} max. (peak value)	40		V
V_{CEO} max.	25		V
I_{CM} max.	500		mA
P_{tot} max. ($T_{mb} \leq 60^{o}C$, $f \geq 1MHz$)	3.5		W
T_j max.	150		^{o}C
	BFR63	BFR64	
f_T min. ($f = 500MHz$, $I_C = 75mA$, $V_{CE} = 20V$)	1000	1200	MHz
P_o typ. ($f = 200MHz$, $I_C = 70mA$, $V_{CE} = 20V$, $d_{im} = -30dB$)	150	150	mW
G_p typ. ($f = 200MHz$, $I_C = 70mA$, $V_{CE} = 20V$)	16	16	dB

Unless otherwise stated data is applicable to both types

OUTLINE AND DIMENSIONS

For details see page 2

OUTLINE AND DIMENSIONS



	Millimetres	
	Min.	Max.
A	5.25	5.75
B1	0.107	0.147
B2	0.7	1.1
B3	5.60	5.85
ØD1	9.0	9.6
ØD2	2.7	2.9
E	10.5	10.7
F	1.0	1.5
H	25.0	29.0
L	14 nom.	
M	1.4	1.6
N	11.2	12.0
N1	-	1.6
N2	7.5	8.5
N3	2.93	3.68
Q	2.85	3.00

Diameter of hole in heatsink: max 4.17mm

Torque on nut

min. 7.5kg cm (0.75N m)

max. 8.5kg cm (0.85N m)

When locking is required, an adhesive instead of a lock washer is preferred.

N-P-N SILICON PLANAR EPITAXIAL TRANSISTORS

BFR63
BFR64

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{CBOM} max. (peak value, $I_C = 100\mu A$)	40	V
V_{CERM} max. (peak value, $R_{BE} = 10\Omega$, $I_C = 10mA$)	40	V
V_{CEO} max. ($I_C = 10mA$)	25	V
V_{EBO} max. ($I_E = 100\mu A$)	3.5	V
I_C max.	200	mA
I_{CM} max. (peak value, f > 1.0MHz)	500	mA
P_{tot} max. ($T_{mb} \leq 60^oC$, f ≥ 1.0MHz	3.5	W

Temperature

T_{stg}	-40 to +150	^oC
T_j max.	150	^oC

THERMAL CHARACTERISTIC

$R_{th(j-mb)}$	25	degC/W
$R_{th(mb-h)}$	0.5	degC/W

ELECTRICAL CHARACTERISTICS ($T_j = 25^oC$ unless otherwise stated)

		Min.	Typ.	Max.	
I_{CBO}	Collector cut-off current $I_E = 0$, $V_{CB} = 20V$	-	-	10	μA
$V_{CE(sat)}$	Collector-emitter saturation voltage $I_C = 100mA$, $I_B = 10mA$	-	-	0.75	V
h_{FE}	Static forward current transfer ratio $I_C = 50mA$, $V_{CE} = 5V$	25	-	-	
	$I_C = 150mA$, $V_{CE} = 5V$	25	-	-	
C_{Tc}	Collector capacitance $I_E = I_e = 0$, $V_{CB} = 20V$, f = 1.0MHz	-	-	4.5	pF
$-C_{re}$	Feedback capacitance $I_C = 10mA$, $V_{CE} = 20V$, f = 1.0MHz, $T_{mb} = 25^oC$	-	1.7	-	pF
N	Noise figure $I_C = 40mA$, $V_{CE} = 20V$, f = 200MHz, $R_S = 75\Omega$, $T_{mb} = 25^oC$	-	6.0	-	dB

ELECTRICAL CHARACTERISTICS (contd.)

			Min.	Typ.	Max.	
f_T	Transition frequency at f = 500MHz					
	I_C = 15mA, V_{CE} = 20V	BFR64	-	1000	-	MHz
	I_C = 75mA, V_{CE} = 20V	BFR63	1000	-	-	MHz
		BFR64	1200	-	-	MHz
	I_C = 150mA, V_{CE} = 20V	BFR63	-	1100	-	MHz
		BFR64	-	1200	-	MHz
P_o	*Output power at f = 200MHz, T_{mb} = 25°C					
	I_C = 70mA, V_{CE} = 20V, v.s.w.r. at output < 2					
	f_p = 202MHz, f_q = 205MHz, d_{im} = -30dB					
	measured at $f_{(2q-p)}$ = 208MHz (channel 9)					
		BFR63	-	150	-	mW
		BFR64	130	150	-	mW
P_o	**Output power at f = 800MHz, T_{mb} = 25°C					
	I_C = 70mA, V_{CE} = 20V, v.s.w.r. at output < 2					
	f_p = 798MHz, f_q = 802MHz, d_{im} = -30dB					
	measured at $f_{(2q-p)}$ = 806MHz (channel 62)					
		BFR64	70	90	-	mW
G_p	Power gain (not neutralised)					
	I_C = 70mA, V_{CE} = 20V, T_{mb} = 25°C,					
	f = 200MHz	BFR63	-	16	-	dB
		BFR64	15	16	-	dB
	f = 800MHz	BFR64	-	6.5	-	dB

*See test circuit etc. on Page 5

**See test circuit etc. on Page 6

CAUTION

This device incorporates Beryllium Oxide, the dust of which is toxic. The device is entirely safe provided that it is not dismantled.

Care should be taken to ensure that all those who may handle, use or dispose of this device are aware of its nature and of the necessary safety precautions. In particular, it should never be thrown out with general industrial or domestic waste.

DISPOSAL SERVICE

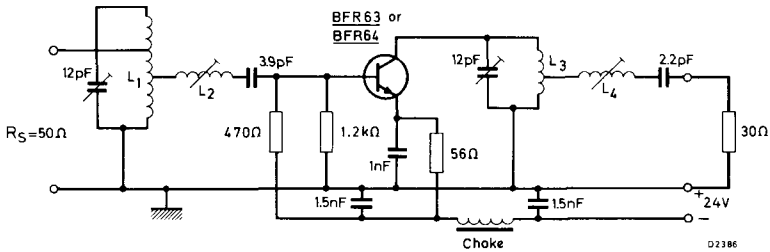
Devices requiring disposal may be returned to the Mullard Service Dept. They must be separately and securely packed and clearly identified. If any are damaged or broken they MUST NOT be sent through the post. In this case, advice is available from the Service Department, Mullard Limited, New Road, Mitcham, Surrey.

ELECTRICAL CHARACTERISTICS (contd.)

Intermodulation characteristics

1. Output power at f = 200MHz, $T_{mb} = 25^{o}C$
   $I_C = 70mA$, $V_{CE} = 20V$, v.s.w.r. at output < 2,
   $f_p = 202MHz$, $f_q = 205MHz$, $d_{im} = -30dB$,
   measured at $f_{(2q-p)} = 208MHz$ (channel 9)

   Test circuit



L_1 = 3 turns of 1.4mm silver plated copper wire, winding pitch 2.7mm, int. dia. 8mm, taps 1.5 and 0.5 turns from earth.
L_2 = 5.5 turns of 1.4mm silver plated copper wire, winding pitch 2.2mm, int. dia. 8mm.
L_3 = 3 turns of 1.4mm silver plated copper wire, winding pitch 3.3mm, int. dia. 8mm.
L_4 = 5.5 turns of 1.4mm silver plated copper wire, winding pitch 2.2mm, int. dia. 11mm.

Basis of adjustment

Intermodulation distortion at $d_{im} = -30dB$ is caused by clipping in h.f. output current and voltage.
The maximum undistorted output power is attained when

(a) Clipping in current and voltage is simultaneous; this occurs if

$$R_{load} = (V_{CE} - V_{cek})/I_C$$

Where V_{cek} is the high frequency knee voltage

Basic of adjustment (contd.)

(b) The h.f. collector current is as low as possible; this occurs if

$$-C_{load} = +C_{oe}$$

Where C_{oe} is the output capacitance of the transistor with short-circuited input. Experimentally obtained values of R_{load} and C_{load}, for maximum output power at an intermodulation factor of -30dB, are:

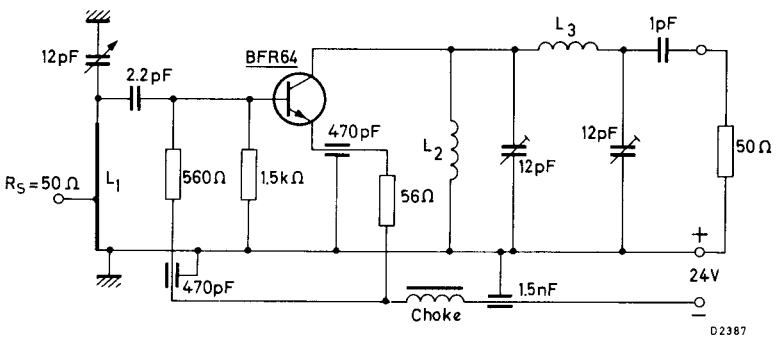
$$R_{load} = 220\Omega,\ C_{load} = -4pF$$

Procedure

1. Remove the transistor and connect a dummy load, consisting of a 220Ω resistor in parallel with a 4pF capacitor, between the collector and the emitter connections of the output circuit.
2. Tune and match the output circuit for zero reflection at 205MHz (i.e. v.s.w.r.=1).
3. Replace the dummy load by the transistor. Tune and match the input circuit for maximum power gain and good bandpass curve. The v.s.w.r. of the output will then be ≤ 2 over most of the channel. Corrections can be made by tuning L_2, this will not disturb the bandpass curve.

2. Output power at f = 800MHz, $T_{mb} = 25^{o}C$
$I_C = 70mA$, $V_{CE} = 20V$, v.s.w.r. at output < 2,
$f_p = 798MHz$, $f_q = 802MHz$, $d_{im} = -30dB$,
measured at $f_{(2q-p)} = 806MHz$ (channel 62)

Test circuit



L_1 = 25 × 7 × 0.85mm silver plated copper strip, input tap at 5mm from earth.
L_2 = 13 turns of 0.6mm enamelled copper wire, int. dia. 8mm.
L_3 = 1.5 turns of 1.3mm copper wire, int. dia. 8mm.

ELECTRICAL CHARACTERISTICS (contd.)

Basis of adjustment

At 800MHz a dummy load cannot be used to adjust for optimum collector load, because at these frequencies the impedance transformations of the dummy load are too high.

A small signal with a frequency of the midchannel 802MHz is fed to the input. The signal is increased until clipping occurs, that is until the output power no longer increases linearly with increasing input signal. Care should be taken not to allow the voltage swing to exceed the V_{CER} value as this may result in the destruction of the transistor by second breakdown.

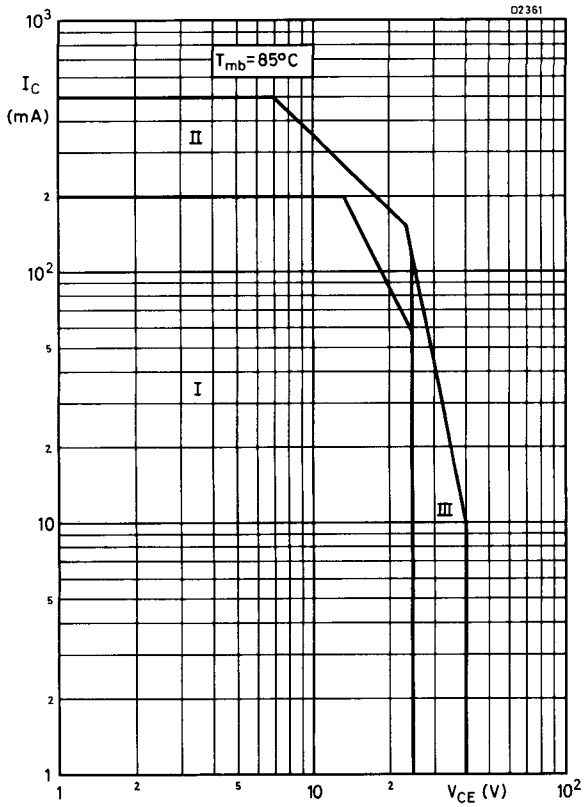
The output circuit is then tuned to eliminate clipping.

The output P_o is given by

$$P_o = I_C(V_{CE} - V_{cek})/2 = 480mW$$

where V_{cek} is the high frequency knee voltage

Keeping the input signal as small as possible at $P_o = 480mW$, the output circuit is adjusted for minimum intermodulation. The input circuit is then adjusted for maximum gain and good bandpass curve. The v.s.w.r. is found to be ≤ 2 over the whole channel.

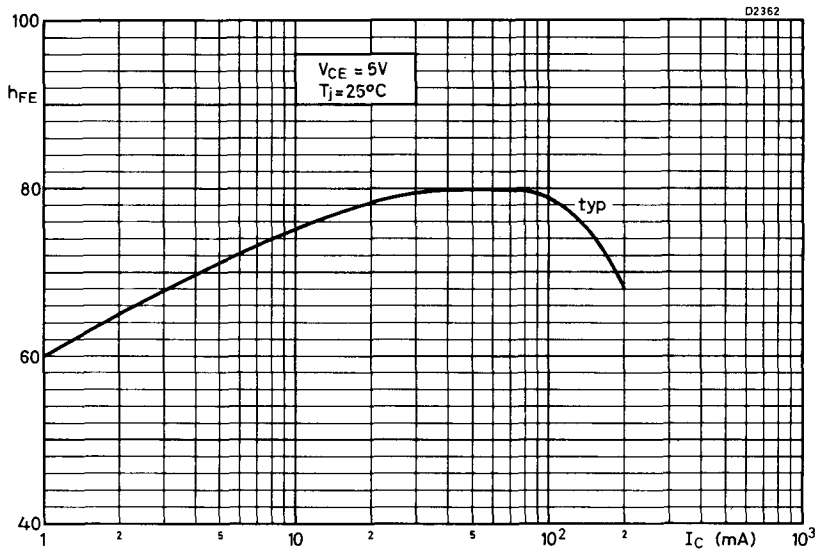


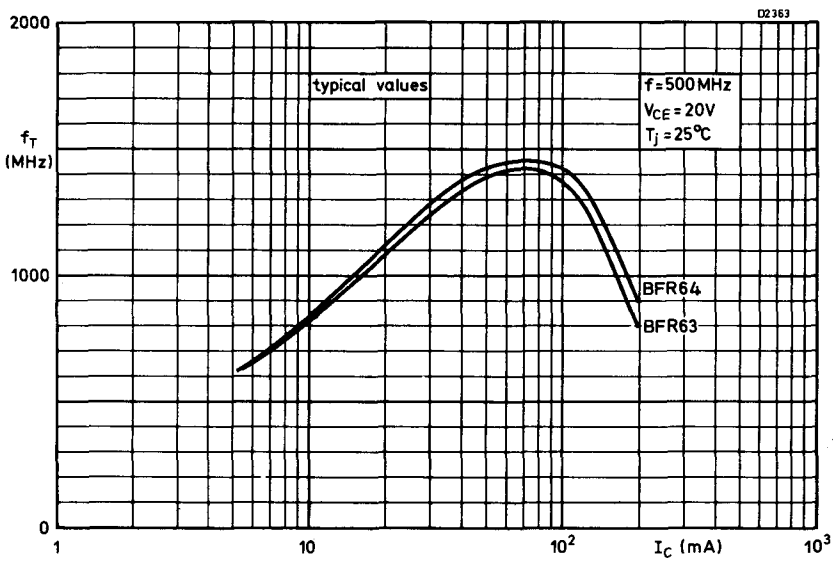
Safe Operating Areas with the transistor forward biased

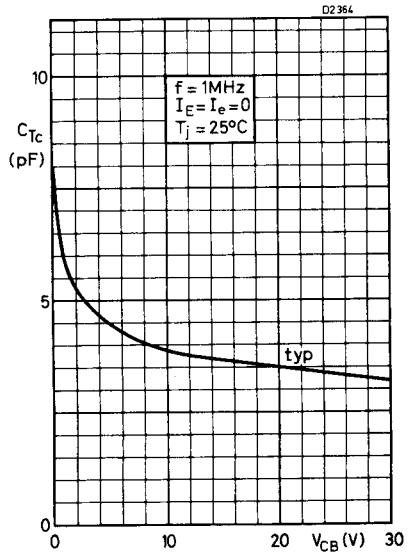
I Region of permissible d.c. operation

II Permissible extension for repetitive pulsed operation; f > 1MHz

III Repetitive pulsed operation in this region is allowed, provided $R_{BE} < 10\Omega$ and f > 1MHz


D2362
100
h_{FE}
80
60
40
V_{CE} = 5V
T_j = 25°C
typ
1
2
5
10
2
5
10^2
2
I_C (mA)
10^3


D2363
2000
f_T
(MHz)
1000
0
typical values
f = 500 MHz
V_{CE} = 20V
T_j = 25°C
BFR64
BFR63
1
10
10^2
I_C (mA)
10^3


D2364
f = 1MHz
$I_E = I_e = 0$
$T_j = 25°C$
C_{Tc} (pF)
10
5
0
typ
0
10
20
V_{CB} (V)
30

N-P-N SILICON PLANAR EPITAXIAL U.H.F. TRANSISTOR

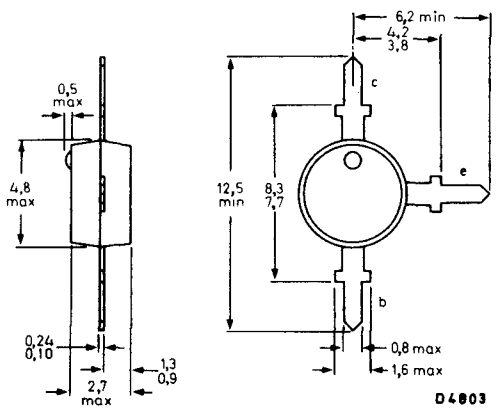
BFR90

Silicon planar epitaxial n-p-n transistor in a plastic T-package. It is primarily intended for use in u.h.f. and microwave amplifiers such as aerial amplifiers, radar systems, oscilloscopes, spectrum analysers etc. The transistor features very low intermodulation distortion, high power gain and excellent wideband properties combined with very high transition frequency and a low noise figure.

QUICK REFERENCE DATA

V_{CBO} max.		20	V
V_{CEO} max.		15	V
I_C max.		25	mA
P_{tot} max.	($T_{amb} \leq 60^oC$)	180	mW
T_j max.		150	^oC
f_T typ.	($I_C = 14mA$, $V_{CE} = 10V$, $f = 500MHz$)	5.0	GHz
$-C_{re}$ typ.	($I_C = 2mA$, $V_{CE} = 10V$, $f = 1MHz$)	0.4	pF
N typ.	($I_C = 2mA$, $V_{CE} = 10V$, $f = 500MHz$)	2.4	dB
G_{UM} typ.	($I_C = 14mA$, $V_{CE} = 10V$, $f = 500MHz$)	19.5	dB
d_{im} typ.	($I_C = 14mA$, $V_{CE} = 10V$, $R_L = 75\Omega$ $V_o = 150mV$, $f_{(p+q-r)} = 493.25MHz$)	-60	dB

OUTLINE AND DIMENSIONS



All dimensions in mm

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{CBO} max.	20	V
V_{CEO} max.	15	V
V_{EBO} max.	2.0	V
I_C max.	25	mA
P_{tot} max. ($T_{amb} \leq 60^oC$)	180	mW

Temperature

T_{stg}	-65 to +150	^oC
T_j max.	150	^oC

THERMAL CHARACTERISTIC

$R_{th(j-amb)}$	in free air, mounted on a glass-fibre print of 40 × 25 × 1mm (see fig. 1)	0.5	$^oC/mW$

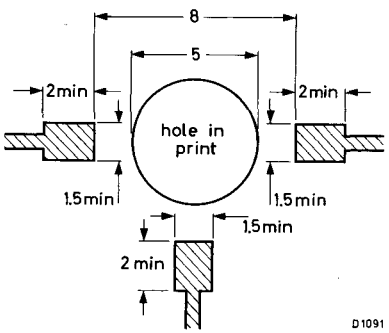


Fig. 1

Requirements for a glass-fibre print

ELECTRICAL CHARACTERISTICS ($T_j = 25^oC$ unless otherwise stated)

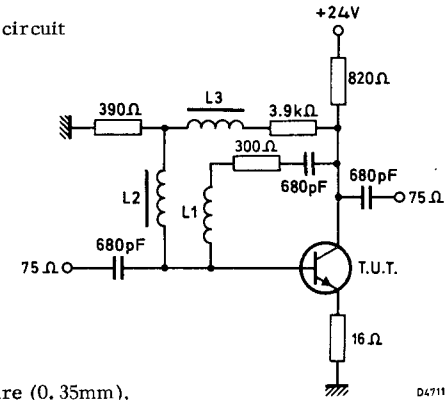
		Min.	Typ.	Max.	
I_{CBO}	Collector cut-off current $I_E = 0$, $V_{CB} = 10V$	-	-	50	nA
h_{FE}	*Static forward current transfer ratio $I_C = 14mA$, $V_{CE} = 10V$	25	50	-	
f_T	*Transition frequency $I_C = 14mA$, $V_{CE} = 10V$, $f = 500MHz$	-	5.0	-	GHz
C_{Tc}	Collector capacitance $I_E = I_e = 0$, $V_{CB} = 10V$, $f = 1.0MHz$	-	0.5	-	pF
C_{Te}	Emitter capacitance $I_C = I_c = 0$, $V_{EB} = 0.5V$, $f = 1.0MHz$	-	0.8	-	pF
$-C_{re}$	Feedback capacitance at $T_{amb} = 25^oC$ $I_C = 2.0mA$, $V_{CE} = 10V$, $f = 1.0MHz$	-	0.4	-	pF
N	Noise figure at optimum source impedance and $T_{amb} = 25^oC$ $I_C = 2.0mA$, $V_{CE} = 10V$, $f = 500MHz$	-	2.4	-	dB
G_{UM}	Maximum unilateralized stage gain at $T_{amb} = 25^oC$ Calculated from s-parameters: $G_{UM} = 10 \log \frac{\lvert s_{fe} \rvert^2}{(1 - \lvert s_{ie} \rvert^2)(1 - \lvert s_{oe} \rvert^2)}$ $I_C = 14mA$, $V_{CE} = 10V$, $f = 500MHz$	-	19.5	-	dB

*Measured under pulsed conditions.

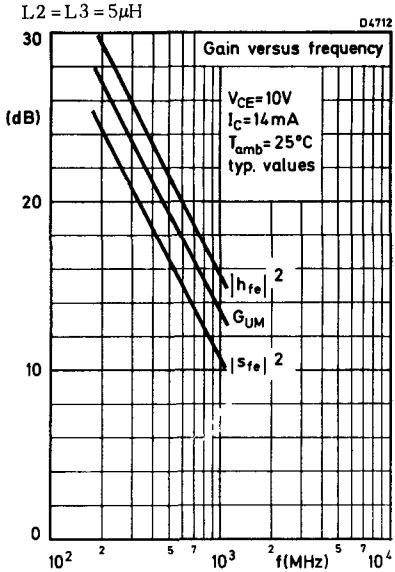
ELECTRICAL CHARACTERISTICS (contd.)

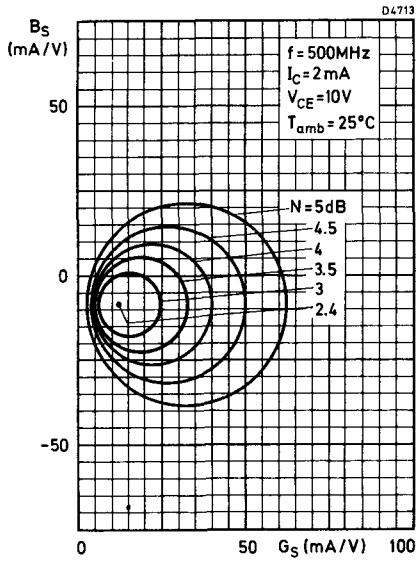
		Min.	Typ.	Max.	
d_{im}	Intermodulation distortion at $T_{amb} = 25^{\circ}C$ $I_C = 14mA$, $V_{CE} = 10V$, $R_L = 75\Omega$, V.S.W.R < 2 $V_p = V_o = 150mV$ at $f_p = 495.25MHz$ $V_q = V_o$ - 6dB at $f_q = 503.25MHz$ $V_r = V_o$ - 6dB at $f_r = 505.25MHz$ measured at $f_{(p+q-r)} = 493.25MHz$	-	-60	-	dB

Intermodulation test circuit

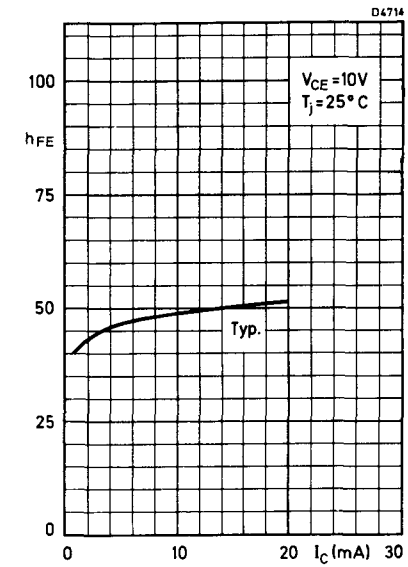


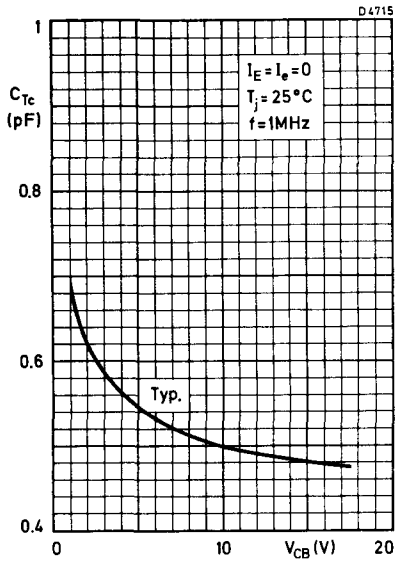
L1 = 4 turns of Cu wire (0.35mm), winding pitch 1mm, int. dia. 4mm
L2 = L3 = 5μH

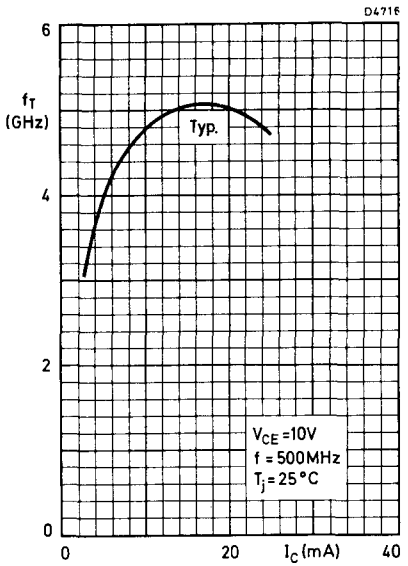


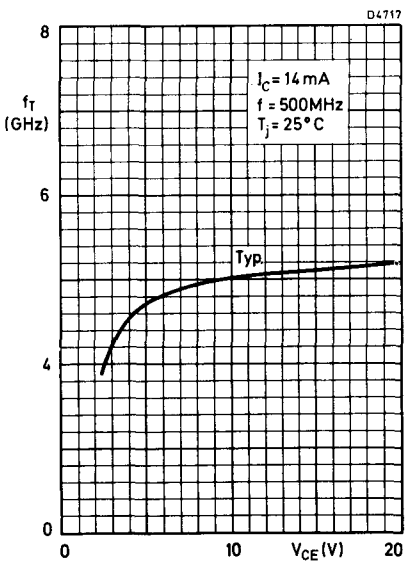


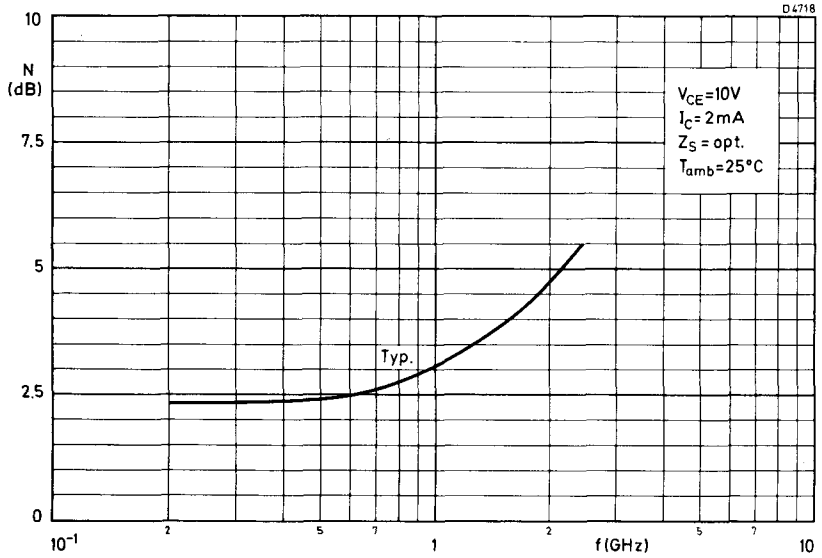
Constant noise figure circles

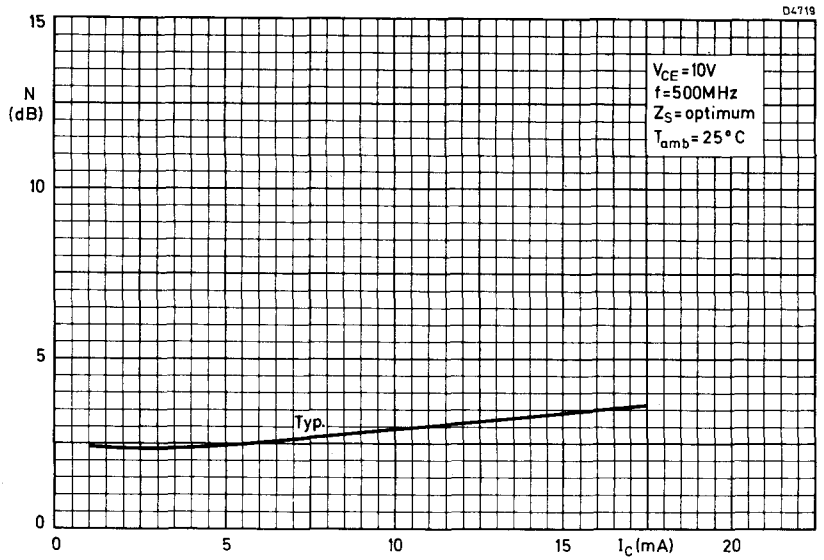

D4714
100
h_{FE}
75
50
25
0
V_{CE} = 10V
T_j = 25°C
Typ.
0
10
20
I_C (mA)
30


D4715
1
C_{Tc}
(pF)
0.8
0.6
0.4
$I_E = I_e = 0$
T_j = 25°C
f = 1MHz
Typ.
0
10
V_{CB} (V)
20

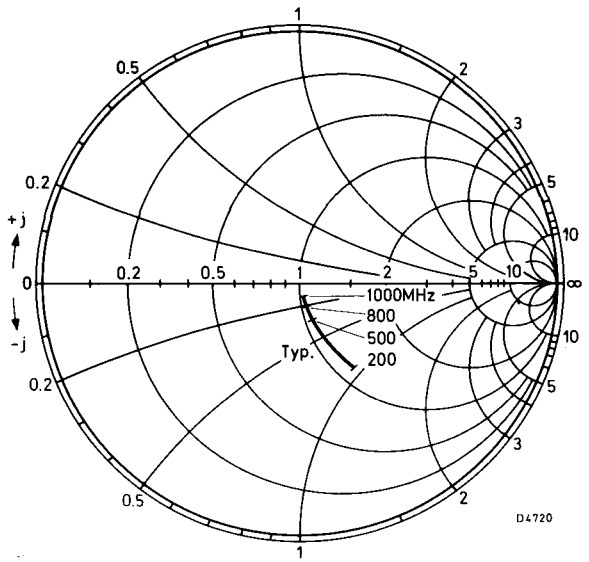

D4716
6
f_T
(GHz)
4
2
0
Typ.
V_{CE} = 10V
f = 500MHz
T_j = 25°C
0
20
I_C (mA)
40


D4717
8
f_T
(GHz)
6
4
0
I_C = 14 mA
f = 500MHz
T_j = 25°C
Typ.
0
10
V_{CE} (V)
20


D4718
10
N
(dB)
7.5
5
2.5
0
V_{CE}=10V
I_C=2mA
Z_S=opt.
T_{amb}=25°C
Typ.
10^{-1}
2
5
7
1
2
5
7
10
f(GHz)

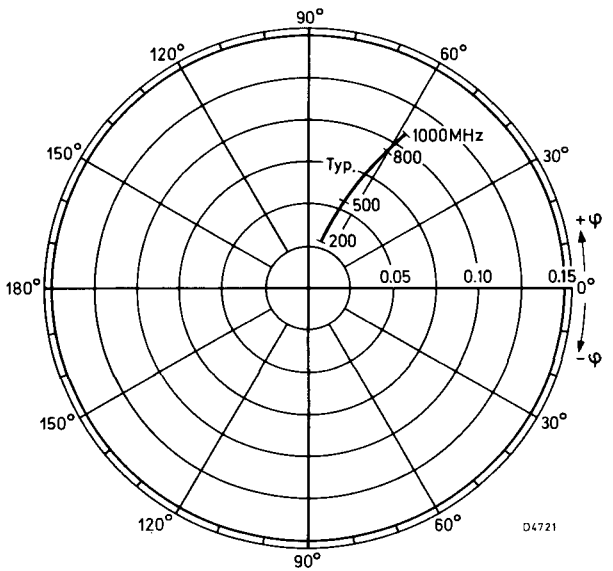

D4719
15
N
(dB)
10
5
0
V_{CE}=10V
f=500MHz
Z_S=optimum
T_{amb}=25°C
Typ.
0
5
10
15
I_C(mA)
20

$V_{CE} = 10V$
$I_C = 14mA$
$T_{amb} = 25^oC$



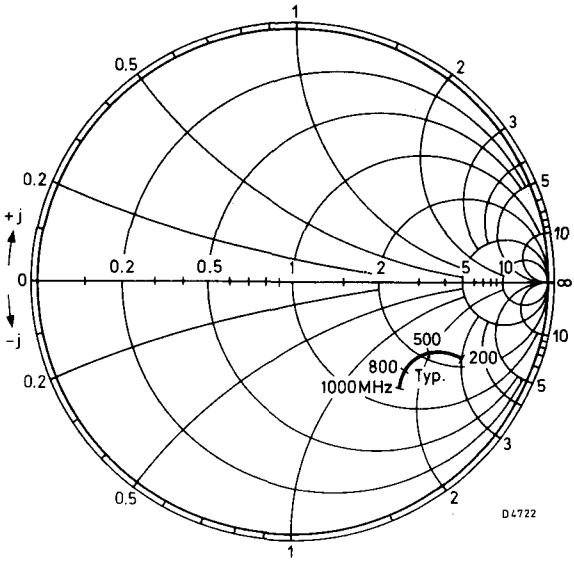
Input impedance derived from input reflection coefficient s_{ie} coordinates in ohm × 50

$V_{CE} = 10V$
$I_C = 14mA$
$T_{amb} = 25^oC$



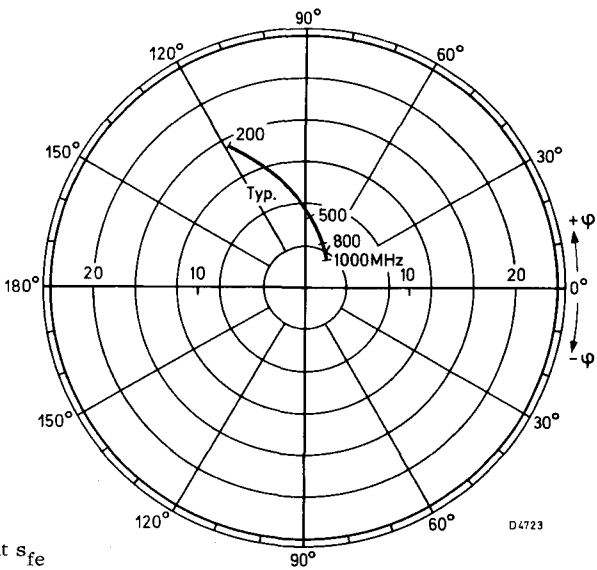
Feedback coefficient s_{re}

$V_{CE} = 10V$
$I_C = 14mA$
$T_{amb} = 25^oC$



Output impedance derived from output reflection coefficient s_{oe} coordinates in ohm × 50

$V_{CE} = 10V$
$I_C = 14mA$
$T_{amb} = 25^oC$



Forward transfer coefficient s_{fe}

N-P-N SILICON PLANAR EPITAXIAL U.H.F. TRANSISTOR

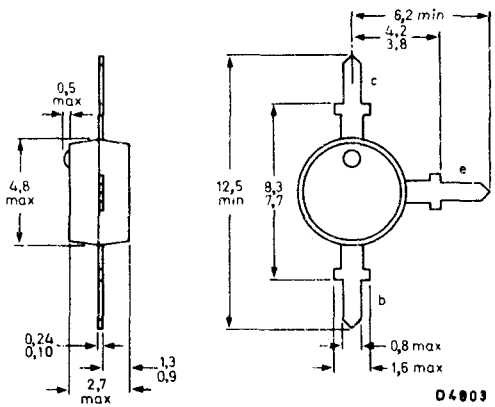
BFR91

Silicon planar epitaxial n-p-n transistor in a plastic T-package. It is primarily intended for use in u.h.f. and microwave amplifiers such as aerial amplifiers, radar systems, oscilloscopes, spectrum analysers etc. The transistor features very low intermodulation distortion, high power gain and excellent wideband properties combined with very high transition frequency and a low noise figure.

QUICK REFERENCE DATA

V_{CBO} max.		15	V
V_{CEO} max.		12	V
I_C max.		35	mA
P_{tot} max.	($T_{amb} \leq 60^oC$)	180	mW
T_j max.		150	^oC
f_T typ.	(I_C = 30mA, V_{CE} = 5V, f = 500MHz)	5.0	GHz
C_{re} typ.	(I_C = 2mA, V_{CE} = 5V, f = 1MHz)	0.8	pF
N typ.	(I_C = 2mA, V_{CE} = 5V, f = 500MHz)	1.9	dB
G_{UM} typ.	(I_C = 30mA, V_{CE} = 5V) f = 500MHz	16.5	dB
d_{im} typ.	(I_C = 30mA, V_{CE} = 5V, R_L = 75Ω V_o = 300mV, $f_{(p+q-r)}$ = 493.25MHz	-60	dB

OUTLINE AND DIMENSIONS



All dimensions in mm

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{CBO} max.	15	V
V_{CEO} max.	12	V
V_{EBO} max.	2.0	V
I_C max.	35	mA
P_{tot} max. ($T_{amb} \leq 60^oC$)	180	mW

Temperature

T_{stg}	-65 to +150	^oC
T_j max.	150	^oC

THERMAL CHARACTERISTIC

$R_{th(j-amb)}$ in free air, mounted on a glass-fibre print of 40 × 25 × 1mm (see fig. 1)	0.5	$^oC/mW$

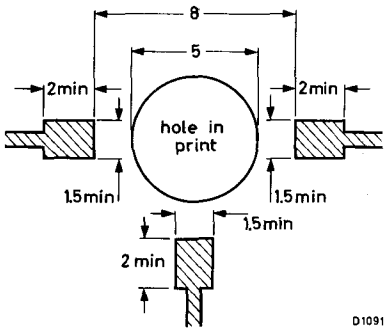


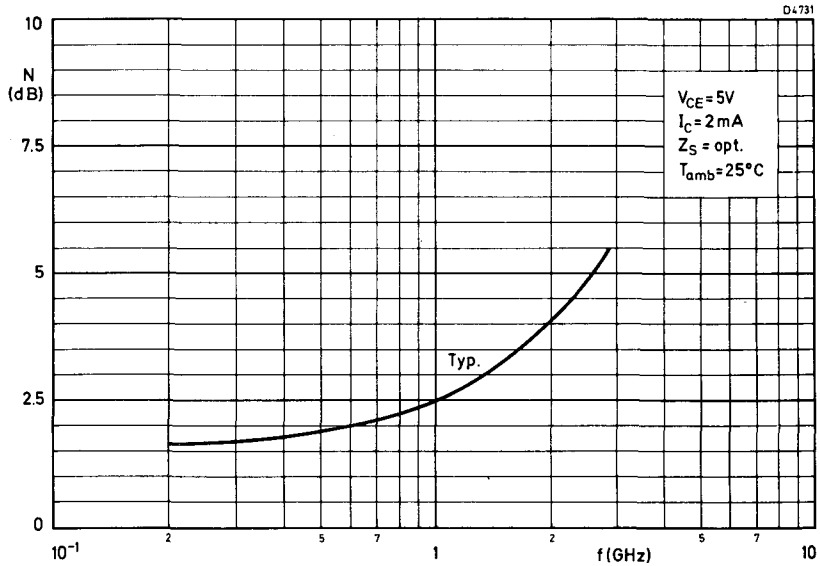
Fig. 1

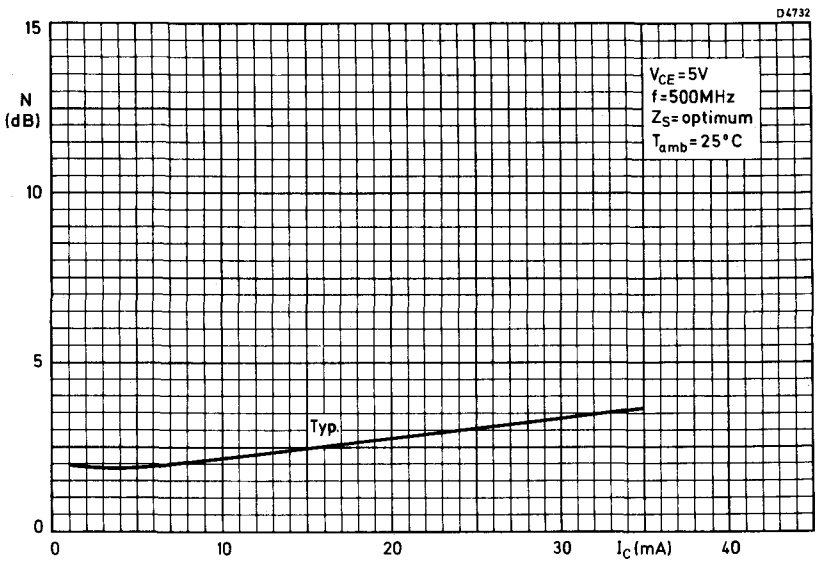
Requirements for a glass-fibre print

ELECTRICAL CHARACTERISTICS ($T_j = 25^oC$ unless otherwise stated)

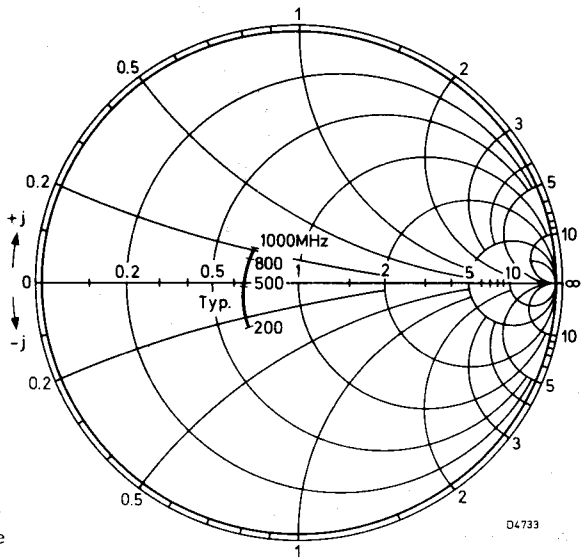
		Min.	Typ.	Max.	
I_{CBO}	Collector cut-off current $I_E = 0$, $V_{CB} = 5.0V$	-	-	50	nA
h_{FE}	*Static forward current transfer ratio $I_C = 30mA$, $V_{CE} = 5.0V$	25	50	-	
f_T	*Transition frequency $I_C = 30mA$, $V_{CE} = 5.0V$, $f = 500MHz$	-	5.0	-	GHz
C_{Tc}	Collector capacitance $I_E = I_e = 0$, $V_{CB} = 10V$, $f = 1.0MHz$	-	0.7	-	pF
C_{Te}	Emitter capacitance $I_C = I_c = 0$, $V_{EB} = 0.5V$, $f = 1.0MHz$	-	1.8	-	pF
C_{re}	Feedback capacitance at $T_{amb} = 25^oC$ $I_C = 2.0mA$, $V_{CE} = 5.0V$, $f = 1.0MHz$	-	0.8	-	pF
N	Noise figure at optimum source impedance and $T_{amb} = 25^oC$ $I_C = 2.0mA$, $V_{CE} = 5.0V$, $f = 500MHz$	-	1.9	-	dB
G_{UM}	Maximum unilateralized stage gain at $T_{amb} = 25^oC$ Calculated from s-parameters: $G_{UM} = 10 \log \frac{\lvert s_{fe} \rvert^2}{(1 - \lvert s_{ie} \rvert^2)(1 - \lvert s_{oe} \rvert^2)}$ $I_C = 30mA$, $V_{CE} = 5.0V$, $f = 500MHz$	-	16.5	-	dB

*Measured under pulsed conditions.


D4731
10
N
(dB)
7.5
5
2.5
0
V_{CE}=5V
I_C=2mA
Z_S = opt.
T_{amb}=25°C
Typ.
10^{-1}
2
5
7
1
2
5
7
10
f(GHz)

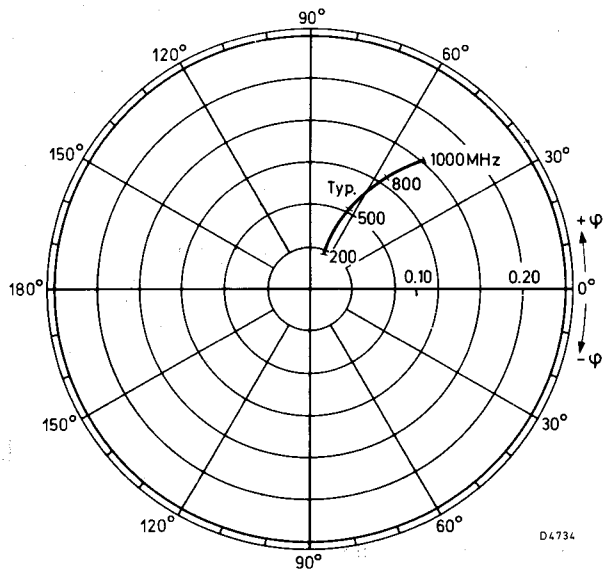

D4732
15
N
(dB)
10
5
0
V_{CE}=5V
f=500MHz
Z_S=optimum
T_{amb}=25°C
Typ.
0
10
20
30
I_C(mA)
40

$V_{CE} = 5V$
$I_C = 30mA$
$T_{amb} = 25^oC$



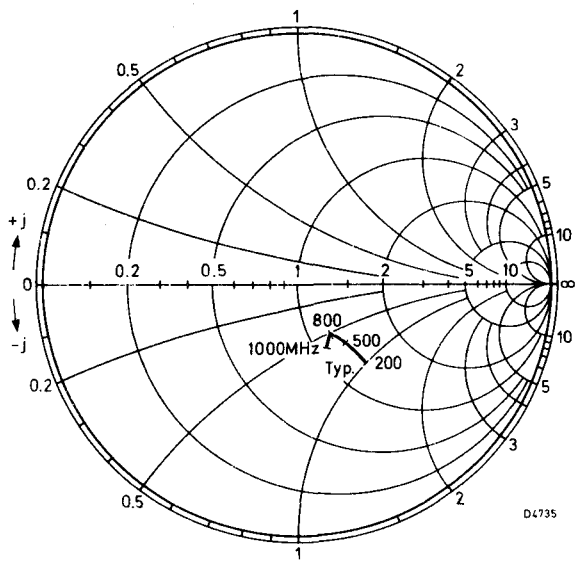
Input impedance derived from input reflection coefficient s_{ie} coordinates in ohm × 50

$V_{CE} = 5V$
$I_C = 30mA$
$T_{amb} = 25^oC$



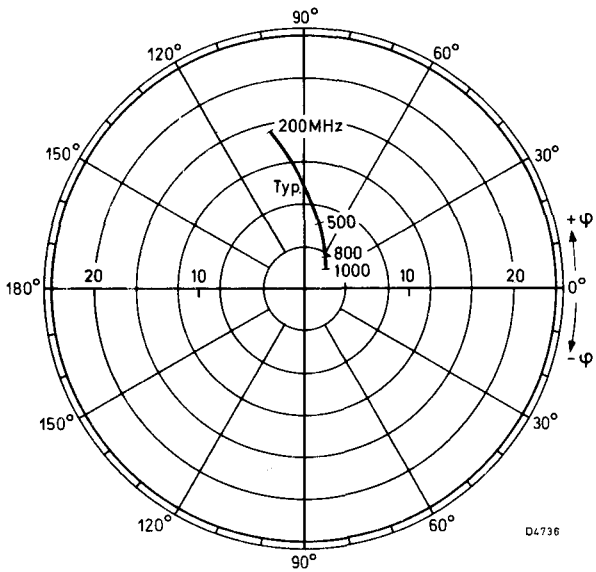
Feedback coefficient s_{re}

$V_{CE} = 5V$
$I_C = 30mA$
$T_{amb} = 25^oC$



Output impedance derived from output reflection coefficient s_{oe} coordinates in ohm × 50

$V_{CE} = 5V$
$I_C = 30mA$
$T_{amb} = 25^oC$



Forward transfer coefficient s_{fe}

μ min. N-P-N SILICON PLANAR EPITAXIAL U.H.F. TRANSISTOR

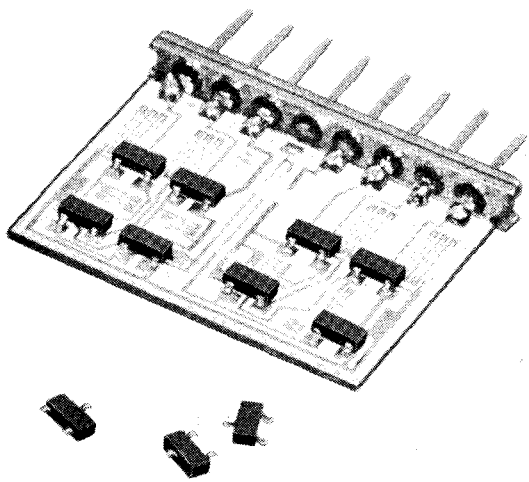
BFR92

Silicon n-p-n planar epitaxial transistor in a micro-miniature plastic envelope. It is primarily intended for use in u.h.f. and microwave amplifiers in thick and thin film circuits, such as in aerial amplifiers, radar systems, oscilloscopes, spectrum analysers, etc.

QUICK REFERENCE DATA

V_{CBO}	max.		20	V
V_{CEO}	max.		15	V
I_C	max.		25	mA
P_{tot}	max.	($T_{amb} \leq 60^oC$)	180	mW
T_j	max.		150	^oC
f_T	typ.	(I_C = 14mA, V_{CE} = 10V, f = 500MHz)	5.0	GHz
$-C_{re}$	typ.	(I_C = 2mA, V_{CE} = 10V, f = 1MHz)	0.7	pF
N	typ.	(I_C = 2mA, V_{CE} = 10V, f = 500MHz)	2.4	dB
G_{UM}	typ.	(I_C = 14mA, V_{CE} = 10V, f = 500MHz)	18	dB
d_{im}	typ.	(I_C = 14mA, V_{CE} = 10V, R_L = 75Ω, V_o = 150mV, f(p+q-r) = 493.25MHz, see also page 4)	-60	dB

OUTLINE AND DIMENSIONS - For details see page 2

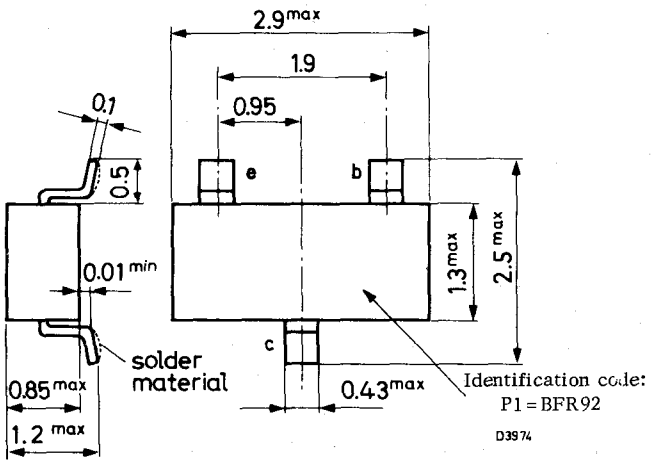


$2\frac{1}{2}$ × actual size

OUTLINE AND DIMENSIONS

All dimensions in millimetres

Plan view from above



RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{CBO} max.	20	V
V_{CEO} max.	15	V
V_{EBO} max.	2.0	V
I_C max.	25	mA
P_{tot} max., $T_{amb} \leq 60^oC$, mounted on a ceramic substrate of 15 × 10 × 0.5mm	180	mW

Temperature

T_{stg}	-65 to +150	^oC
T_j max.	150	^oC

THERMAL CHARACTERISTIC

$R_{th(j-amb)}$	Thermal resistance between junction and ambient, the device mounted on a ceramic substrate of 15 × 10 × 0.5mm	0.50	$^oC/mW$

ELECTRICAL CHARACTERISTICS ($T_j = 25^oC$ unless otherwise stated)

		Min.	Typ.	Max.	
I_{CBO}	Collector cut-off current $I_E = 0$, $V_{CB} = 10V$	-	-	50	nA
h_{FE}	*Static forward current transfer ratio $I_C = 14mA$, $V_{CE} = 10V$	25	50	-	
f_T	*Transition frequency $I_C = 14mA$, $V_{CE} = 10V$, $f = 500MHz$	-	5.0	-	GHz
C_{Tc}	Collector capacitance $I_E = I_e = 0$, $V_{CB} = 10V$, $f = 1.0MHz$	-	0.75	-	pF
C_{Te}	Emitter capacitance $I_C = I_c = 0$, $V_{EB} = 0.5V$, $f = 1.0MHz$	-	0.8	-	pF
$-C_{re}$	Feedback capacitance, $T_{amb} = 25^oC$ $I_C = 2.0mA$, $V_{CE} = 10V$, $f = 1.0MHz$	-	0.7	-	pF
N	†Noise figure at optimum source impedance, $T_{amb} = 25^oC$ $I_C = 2.0mA$, $V_{CE} = 10V$, $f = 500MHz$	-	2.4	-	dB
G_{UM}	Max. unilateralized stage gain at $T_{amb} = 25^oC$, calculated from s-parameters: $G_{UM} = 10 \log \frac{\lvert s_{fe} \rvert^2}{(1 - \lvert s_{ie} \rvert^2)(1 - \lvert s_{oe} \rvert^2)}$ $I_C = 14mA$, $V_{CE} = 10V$, $f = 500MHz$	-	18	-	dB

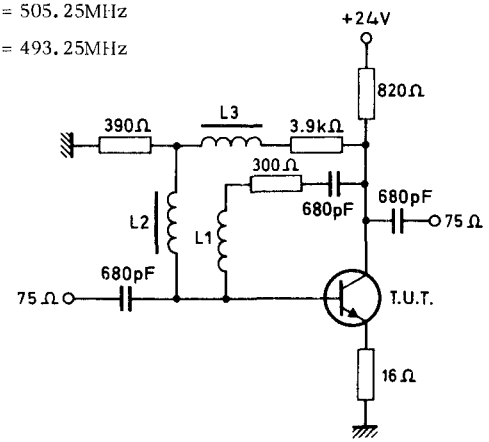
*Measured under pulsed conditions.
†Crystal mounted in a BFR90 envelope.

ELECTRICAL CHARACTERISTICS (Cont' d)

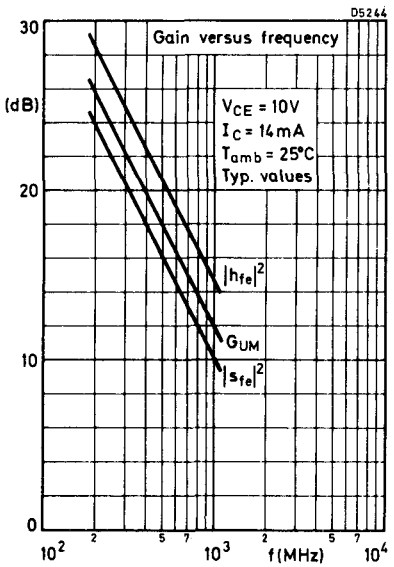
		Min.	Typ.	Max.	
d_{im}	Intermodulation distortion at $T_{amb} = 25^{o}C$ $I_C = 14mA$, $V_{CE} = 10V$, $R_L = 75\Omega$, V.S.W.R. $\prec 2$	-	-60	-	dB

$V_p = V_o = 150mV$ at $f_p = 495.25MHz$
$V_q = V_o$ -6dB at $f_q = 503.25MHz$
$V_r = V_o$ -6dB at $f_r = 505.25MHz$
Measured at $f_{(p+q-r)} = 493.25MHz$

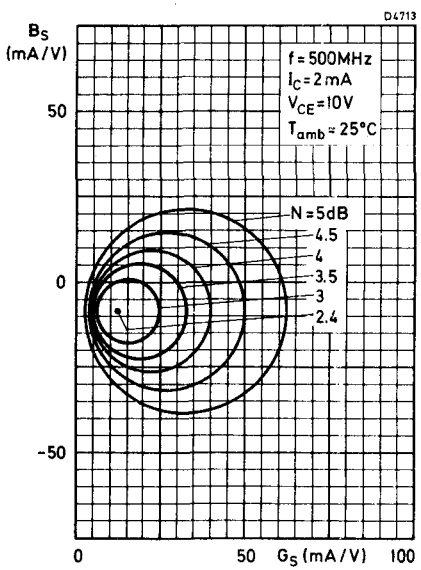
Intermodulation test circuit:

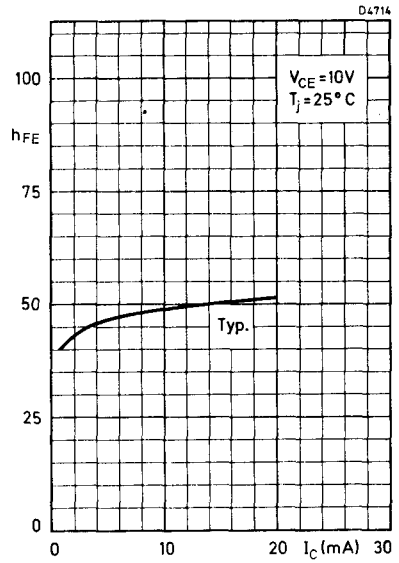


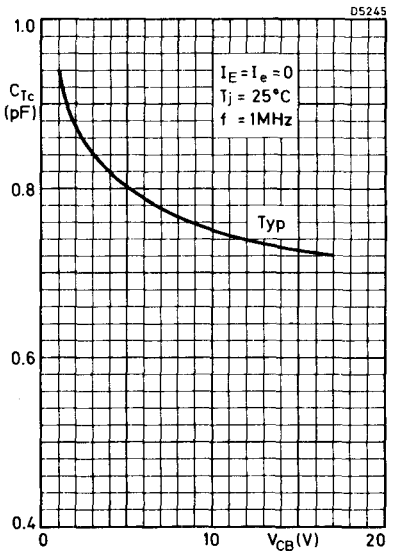
L1 = 4 turns of Cu wire (0.35mm), winding pitch 1mm, int. dia. 4mm
L2 = L3 = 5μH

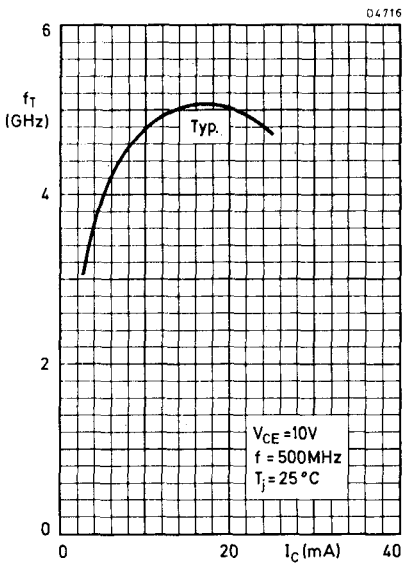


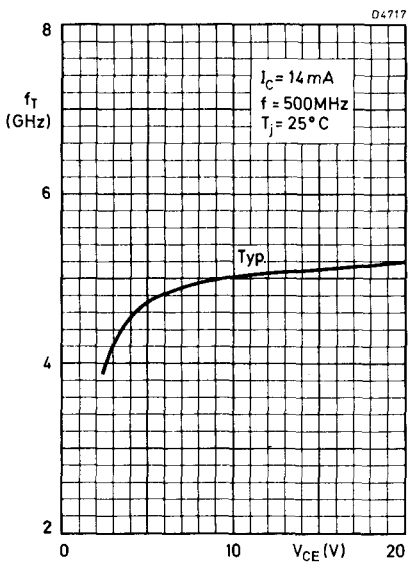
Circles of constant noise figure

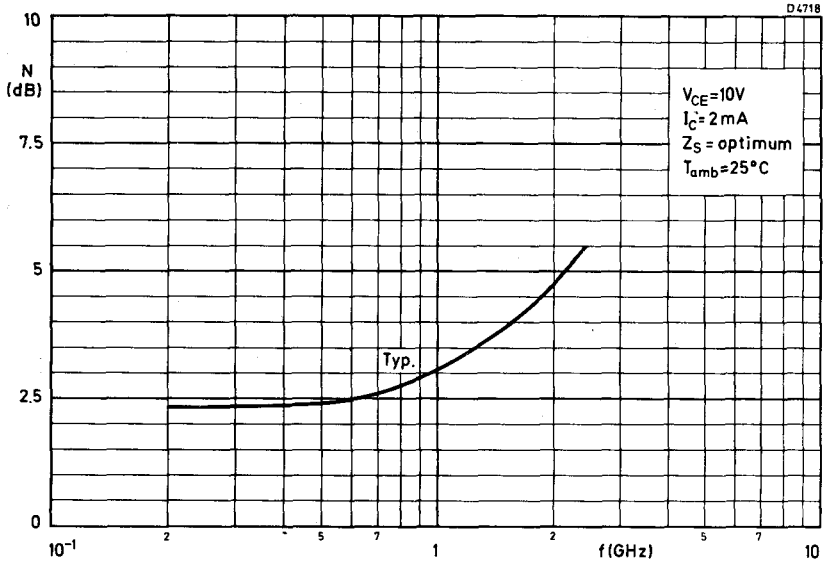


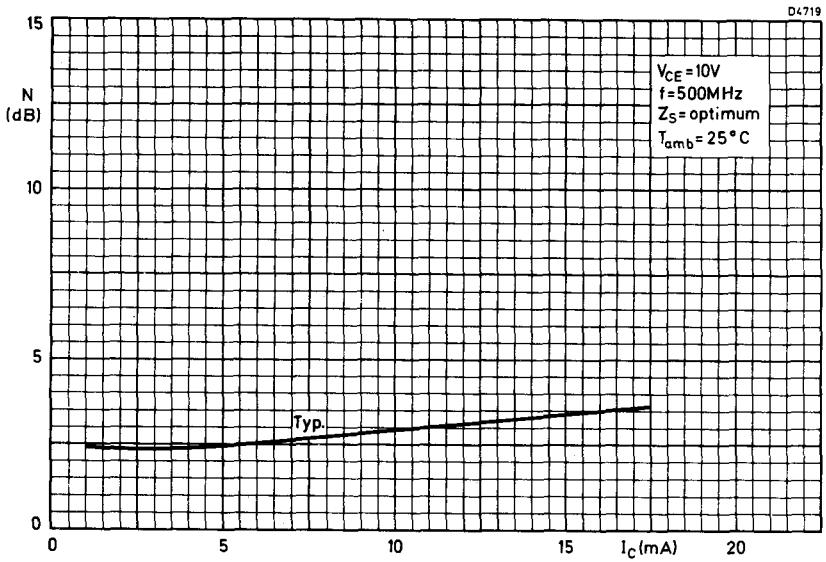

D4714
100
h_{FE}
75
50
25
0
0
10
20
I_C (mA)
30
V_{CE} = 10V
T_j = 25° C
Typ.


D5245
1.0
C_{Tc} (pF)
0.8
0.6
0.4
0
10
V_{CB} (V)
20
$I_E = I_e = 0$
T_j = 25°C
f = 1MHz
Typ

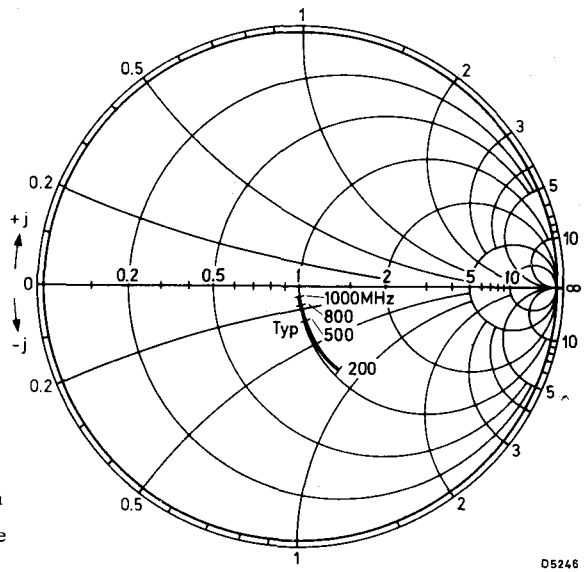

D4716
6
f_T (GHz)
4
2
0
0
20
I_C (mA)
40
Typ.
V_{CE} = 10V
f = 500MHz
T_j = 25 °C


D4717
8
f_T (GHz)
6
4
2
0
10
V_{CE} (V)
20
I_C = 14 mA
f = 500MHz
T_j = 25°C
Typ.


D4718
10
N
(dB)
7.5
5
2.5
0
V_{CE}=10V
I_C= 2 mA
Z_S = optimum
T_{amb}=25°C
Typ.
10^{-1}
2
5
7
1
2
5
7
10
f(GHz)

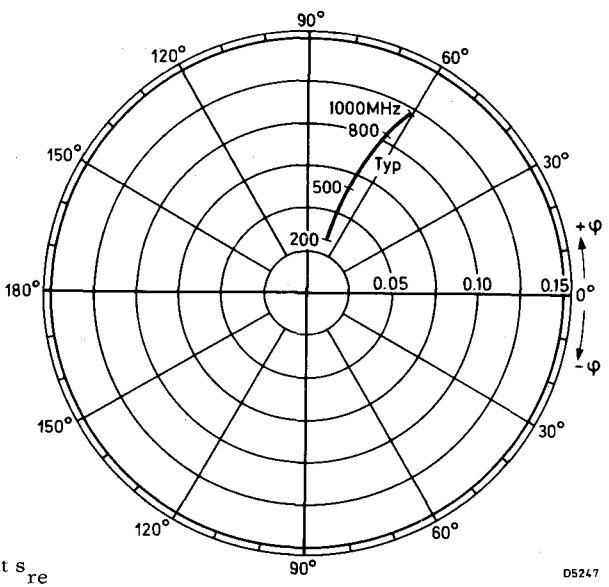

D4719
15
N
(dB)
10
5
0
V_{CE} = 10V
f = 500MHz
Z_S = optimum
T_{amb} = 25 °C
Typ.
0
5
10
15
I_C(mA)
20

V_{CE} = 10V
I_C = 14mA
T_{amb} = 25°C



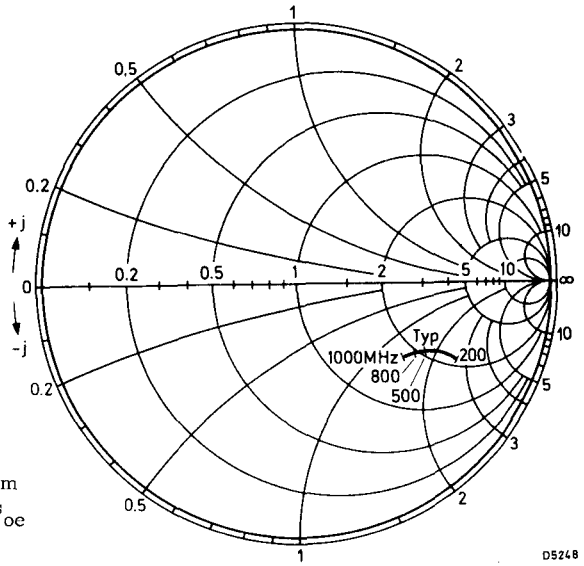
Input impedance derived from input reflection coefficient s_{ie} coordinates in ohm × 50

V_{CE} = 10V
I_C = 14mA
T_{amb} = 25°C



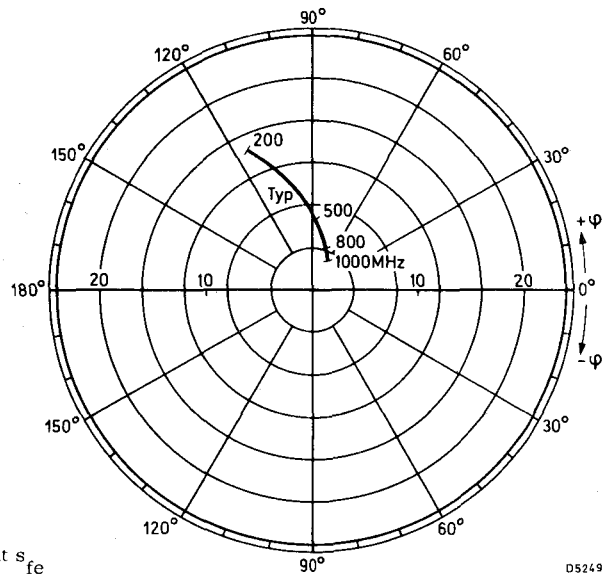
Reverse transfer coefficient s_{re}

V_{CE} = 10V
I_C = 14mA
T_{amb} = 25°C



Output impedance derived from output reflection coefficient s_{oe} coordinates in ohm × 50

V_{CE} = 10V
I_C = 14mA
T_{amb} = 25°C



Forward transfer coefficient s_{fe}

μmin. N-P-N SILICON PLANAR EPITAXIAL U.H.F. TRANSISTOR

BFR93

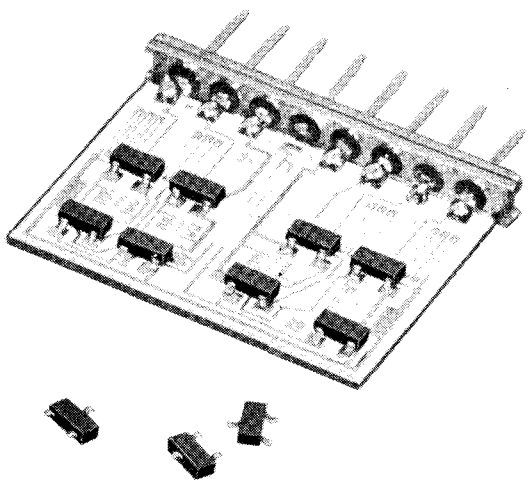
Silicon n-p-n planar epitaxial transistor in a micro-miniature plastic envelope. It is primarily intended for use in u.h.f. and microwave amplifiers in thick and thin film circuits, such as in aerial amplifiers, radar systems, oscilloscopes, spectrum analyers, etc.

QUICK REFERENCE DATA

V_{CBO}	max.		15	V
V_{CEO}	max.		12	V
I_C	max.		35	mA
P_{tot}	max.	($T_{amb} \leq 60^oC$)	180	mW
T_j	max.		150	^oC
f_T	typ.	(I_C = 30mA, V_{CE} = 5V, f = 500MHz)	5.0	GHz
$-C_{re}$	typ.	(I_C = 2mA, V_{CE} = 5V, f = 1MHz)	0.8	pF
N	typ.	(I_C = 2mA, V_{CE} = 5V, f = 500MHz)	1.9	dB
G_{UM}	typ.	(I_C = 30mA, V_{CE} = 5V, f = 500MHz)	16.5	dB
d_{im}	typ.	(I_C = 30mA, V_{CE} = 5V, R_L = 75Ω, V_o = 300mV $f_{(p+q-r)}$ = 493.25MHz, see also page 4)	-60	dB

OUTLINE AND DIMENSIONS

For details see page 2

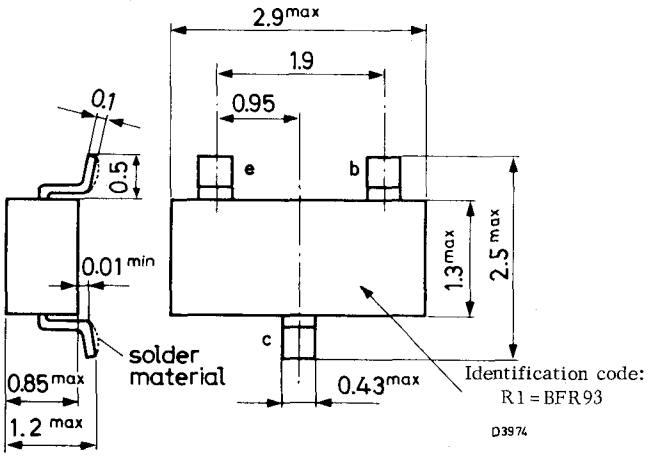


$2\frac{1}{2}$ × actual size

OUTLINE AND DIMENSIONS

All dimensions in millimetres

Plan view from above



RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{CBO} max.	15	V
V_{CEO} max.	12	V
V_{EBO} max.	2.0	V
I_C max.	35	mA
P_{tot} max., $T_{amb} \leq 60^oC$, mounted on a ceramic substrate of 15 × 10 × 0.5mm	180	mW

Temperature

T_{stg}	-65 to +150	^oC
T_j max.	150	^oC

THERMAL CHARACTERISTIC

$R_{th(j-amb)}$	Thermal resistance between junction and ambient, the device mounted on a ceramic substrate of 15 × 10 × 0.5mm	0.50	$^oC/mW$

μ min. N-P-N SILICON PLANAR EPITAXIAL U.H.F. TRANSISTOR

BFR93

ELECTRICAL CHARACTERISTICS ($T_j = 25^oC$ unless otherwise stated)

		Min.	Typ.	Max.	
I_{CBO}	Collector cut-off current $I_E = 0$, $V_{CB} = 10V$	-	-	50	nA
h_{FE}	*Static forward current transfer ratio $I_C = 30mA$, $V_{CE} = 5V$	25	50	-	
f_T	*Transition frequency $I_C = 30mA$, $V_{CE} = 5V$, $f = 500MHz$	-	5.0	-	GHz
C_{Tc}	Collector capacitance $I_E = I_e = 0$, $V_{CB} = 10V$, $f = 1.0MHz$	-	0.7	-	pF
C_{Te}	Emitter capacitance $I_C = I_c = 0$, $V_{EB} = 0.5V$, $f = 1.0MHz$	-	1.8	-	pF
$-C_{re}$	Feedback capacitance, $T_{amb} = 25^oC$ $I_C = 2.0mA$, $V_{CE} = 5V$, $f = 1.0MHz$	-	0.8	-	pF
N	†Noise figure at optimum source impedance, $T_{amb} = 25^oC$ $I_C = 2.0mA$, $V_{CE} = 5V$, $f = 500MHz$	-	1.9	-	dB
G_{UM}	Max. unilateralized stage gain at $T_{amb} = 25^oC$, calculated from s-parameters: $G_{UM} = 10 \log \frac{\lvert s_{fe} \rvert^2}{(1 - \lvert s_{ie} \rvert^2)(1 - \lvert s_{oe} \rvert^2)}$ $I_C = 30mA$, $V_{CE} = 5V$, $f = 500MHz$	-	16.5	-	dB

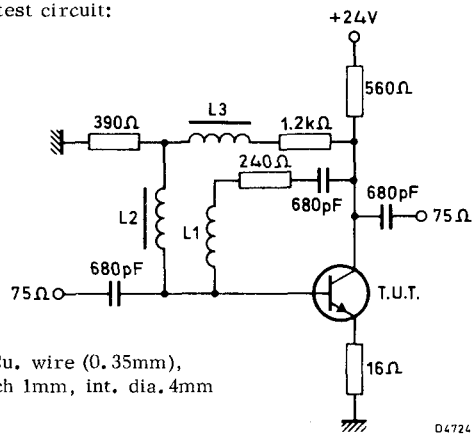
*Measured under pulsed conditions

†Crystal mounted in a BFR91 envelope

ELECTRICAL CHARACTERISTICS (Cont'd)

		Min.	Typ.	Max.	
d_{im}	†Intermodulation distortion at $T_{amb} = 25^{o}C$				
	I_C = 30mA, V_{CE} = 5V, R_L = 75Ω, V.S.W.R. ≤ 2	-	-60	-	dB
	$V_p = V_o$ = 300mV at f_p = 495.25MHz				
	$V_q = V_o$ -6dB at f_q = 503.25MHz				
	$V_r = V_o$ -6dB at f_r = 505.25MHz				
	Measured at $f_{(p+q-r)}$ = 493.25MHz				

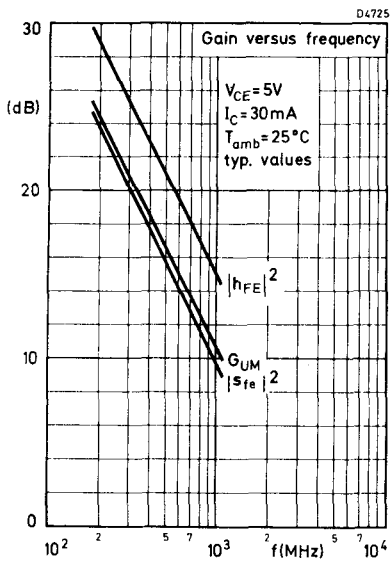
Intermodulation test circuit:



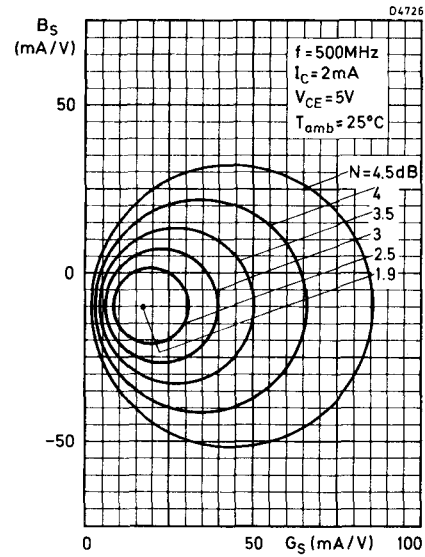
L1 = 4 turns of Cu. wire (0.35mm), winding pitch 1mm, int. dia. 4mm

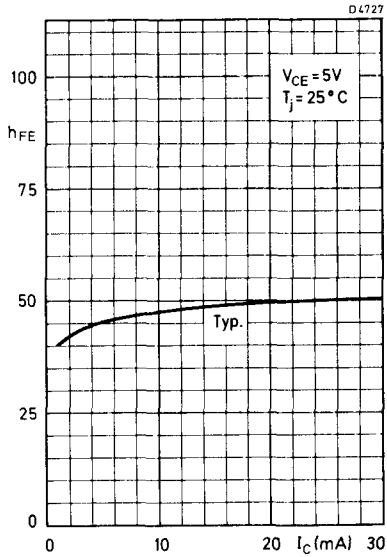
L2 = L3 = 5μH

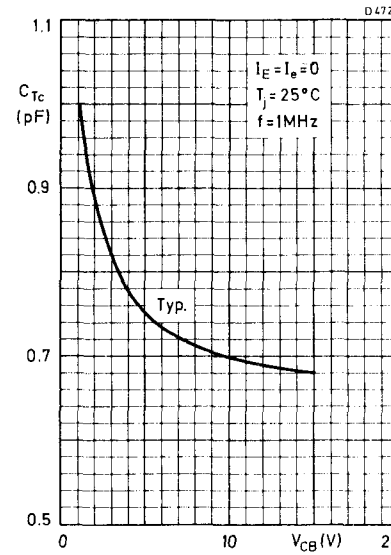
†Crystal mounted in a BFR91 envelope

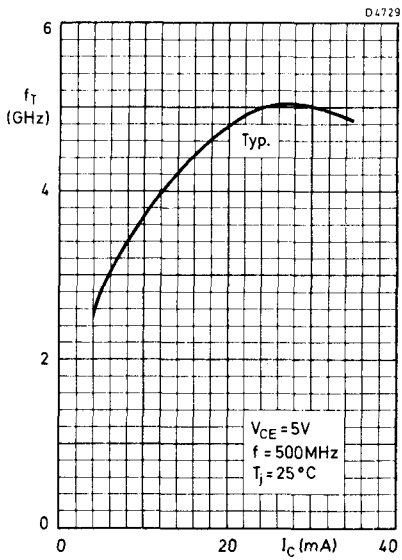


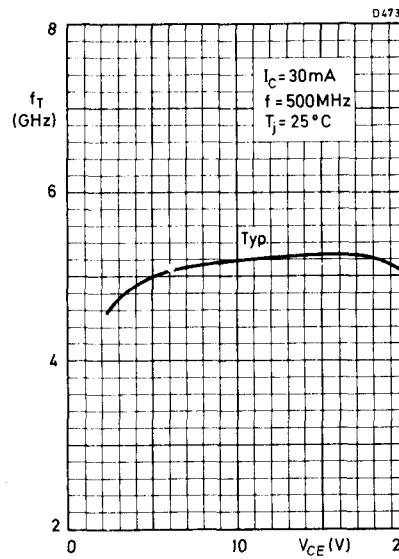
Circles of constant noise figure

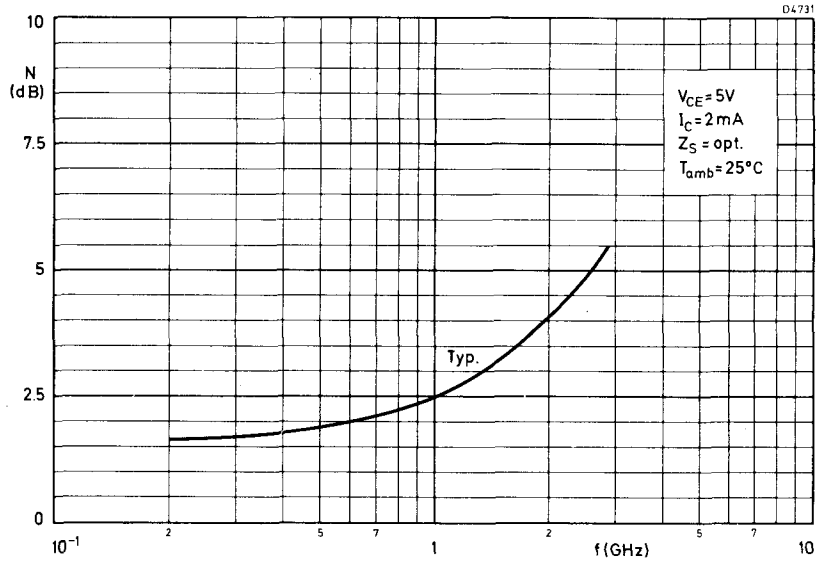


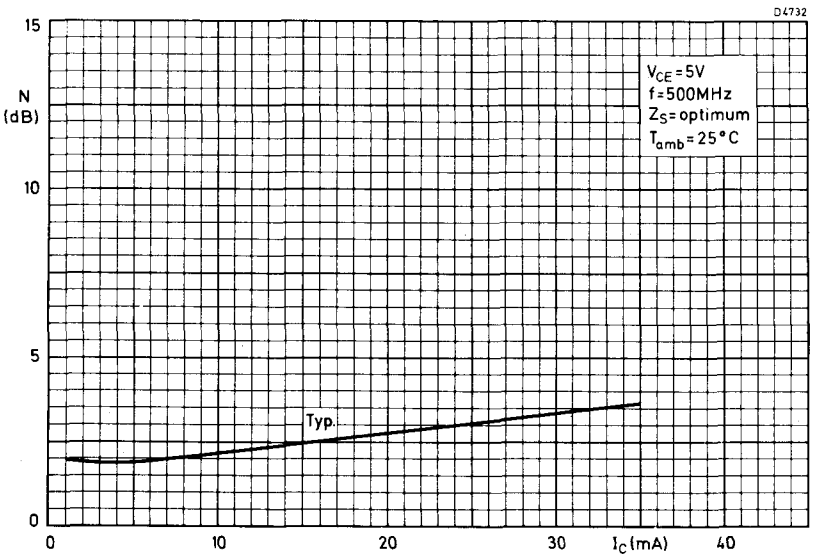

D4727
100
75
50
25
0
h_{FE}
V_{CE} = 5V
T_j = 25 °C
Typ.
0
10
20
I_C (mA)
30


D4728
1.1
0.9
0.7
0.5
C_{Tc} (pF)
$I_E = I_e = 0$
T_j = 25 °C
f = 1MHz
Typ.
0
10
V_{CB} (V)
20

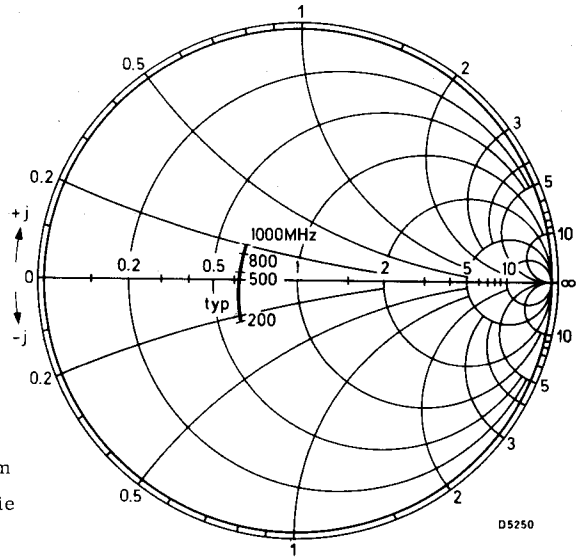

D4729
6
4
2
0
f_T (GHz)
Typ.
V_{CE} = 5V
f = 500MHz
T_j = 25 °C
0
20
I_C (mA)
40


D4730
8
6
4
2
f_T (GHz)
I_C = 30mA
f = 500MHz
T_j = 25 °C
Typ.
0
10
V_{CE} (V)
20


D4731
10
N
(dB)
7.5
5
2.5
0
V_{CE}=5V
I_C=2mA
Z_S=opt.
T_{amb}=25°C
Typ.
10^{-1}
2
5
7
1
2
5
7
10
f(GHz)

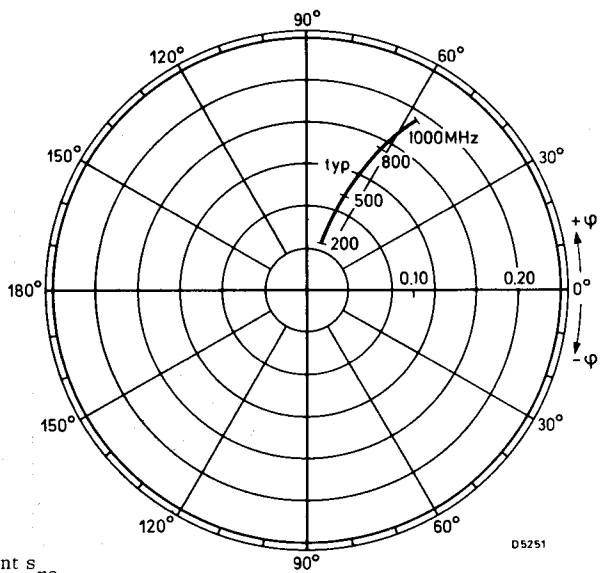

D4732
15
N
(dB)
10
5
0
V_{CE}=5V
f=500MHz
Z_S=optimum
T_{amb}=25°C
Typ.
0
10
20
30
I_C(mA)
40

V_{CE} = 5V
I_C = 30mA
T_{amb} = 25°C



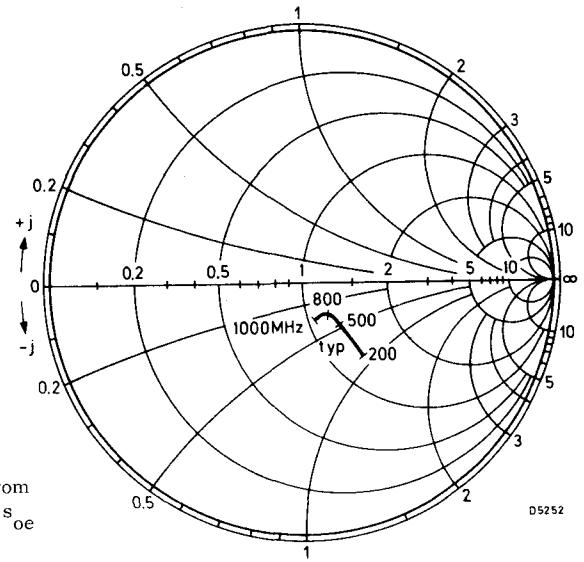
Input impedance derived from input reflection coefficient s_{ie} coordinates in ohm × 50

V_{CE} = 5V
I_C = 30mA
T_{amb} = 25°C



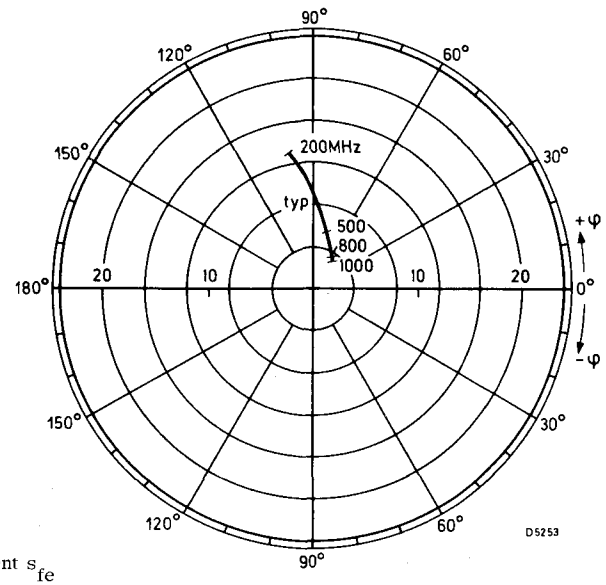
Reverse transfer coefficient s_{re}

V_{CE} = 5V
I_C = 30mA
T_{amb} = 25°C



Output impedance derived from output reflection coefficient s_{oe} coordinates in ohm × 50

V_{CE} = 5V
I_C = 30mA
T_{amb} = 25°C



Forward transfer coefficient s_{fe}

μ min. N-P-N SILICON PLANAR EPITAXIAL TRANSISTOR

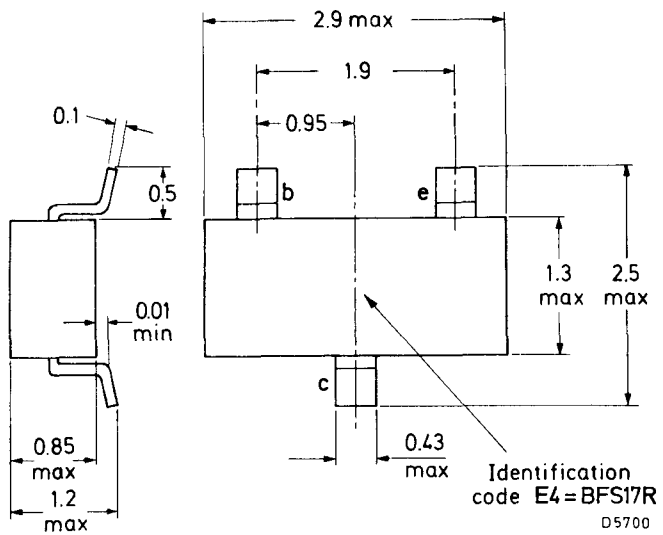
BFS17R

Silicon n-p-n planar epitaxial transistor in a subminiature plastic envelope, intended for a wide range of v.h.f. and u.h.f. applications in thin and thick films.

QUICK REFERENCE DATA

V_{CBOM}	max.	25	V
V_{CEO}	max.	15	V
I_{CM}	max.	50	mA
P_{tot}	max., $T_{amb} \leq 25^{o}C$	200	mW
T_j	max.	150	^{o}C
h_{FE}	at I_C = 2mA, V_{CE} = 1V	20-150	
f_T	typ., I_C = 25mA, V_{CE} = 5V, f = 500MHz	1.3	GHz
N	typ., I_C = 2mA, V_{CE} = 5V, R_S = 50Ω, f = 500MHz	4.5	dB

OUTLINE AND DIMENSIONS



All dimensions in millimetres
Plan view from above

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{CBOM}	max. (peak value)	25	V
V_{CEO}	max. (I_C = 10mA)	15	V
V_{EBO}	max.	2.5	V
I_C	max. (d.c.)	25	mA
I_{CM}	max. (peak value)	50	mA
P_{tot}	max. $T_{amb} \leq 25^oC$, mounted on a ceramic substrate of 7 × 5 × 0.5mm	200	mW

Temperature

T_{stg}		-65 to +150	^oC
T_j	max.	150	^oC

THERMAL CHARACTERISTICS

$R_{th(j\text{-}amb)}$	Thermal resistance between junction and ambient, the device mounted on a ceramic substrate of 7×5×0.5mm	0.62	$^oC/mW$

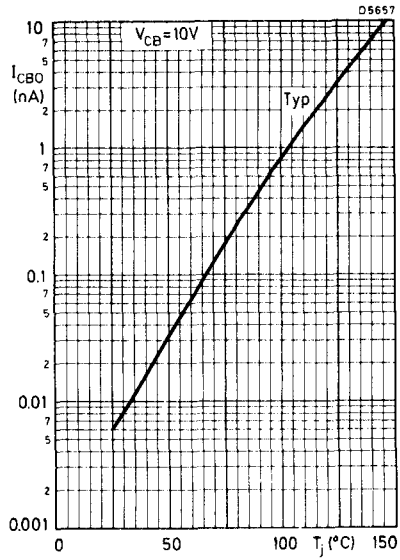
μ min. N-P-N SILICON PLANAR EPITAXIAL TRANSISTOR

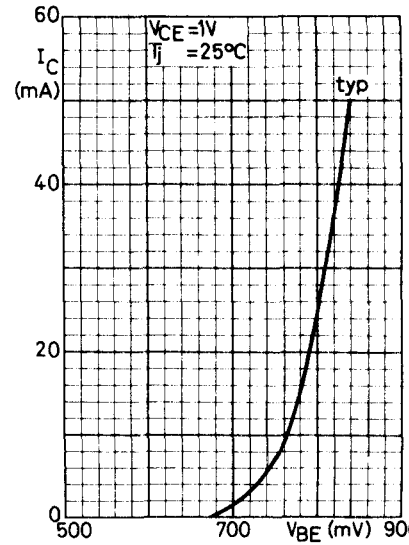
BFS17R

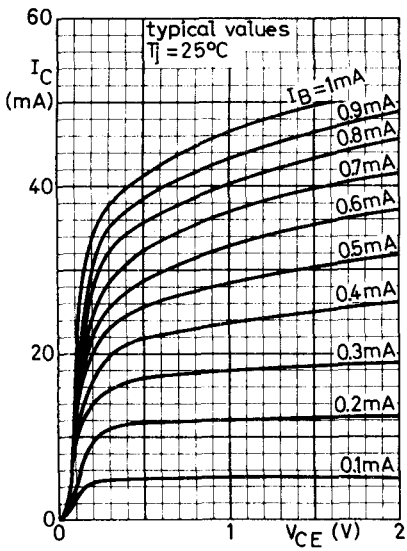
ELECTRICAL CHARACTERISTICS ($T_j = 25^oC$ unless otherwise stated)

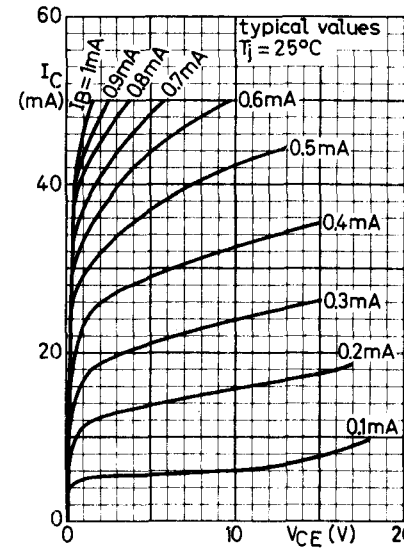
		Min.	Typ.	Max.	
I_{CBO}	Collector cut-off current				
	$I_E = 0$, $V_{CB} = 10V$	-	-	10	nA
	$I_E = 0$, $V_{CB} = 10V$, $T_j = 100^oC$	-	-	10	μA
h_{FE}	Static forward current transfer ratio				
	$I_C = 2.0mA$, $V_{CE} = 1.0V$	20	-	150	
	$I_C = 25mA$, $V_{CE} = 1.0V$	20	-	-	
f_T	Transition frequency				
	$I_C = 2.0mA$, $V_{CE} = 5.0V$, $f = 500MHz$	-	1.0	-	GHz
	$I_C = 25mA$, $V_{CE} = 5.0V$, $f = 500MHz$	-	1.3	-	GHz
$-C_{re}$	Feedback capacitance				
	$I_C = 2.0mA$, $V_{CE} = 5.0V$, $f = 1.0MHz$	-	0.65	-	pF
C_{Tc}	Collector capacitance				
	$I_E = I_e = 0$, $V_{CB} = 10V$, $f = 1.0MHz$	-	-	1.5	pF
C_{Te}	Emitter capacitance				
	$I_C = I_c = 0$, $V_{EB} = 0.5V$, $f = 1.0MHz$	-	-	2.0	pF
*N	Noise figure				
	$I_C = 2.0mA$, $V_{CE} = 5.0V$,				
	$R_S = 50\Omega$, $f = 500MHz$	-	4.5	-	dB
d_{im}	Intermodulation distortion				
	$I_C = 10mA$, $V_{CE} = 6.0V$, $R_L = 37.5\Omega$,				
	$T_{amb} = 25^oC$				
	$V_o = 100mV$ at $f_p = 183MHz$				
	$V_o = 100mV$ at $f_q = 200MHz$				
	measured at $f_{(2q-p)} = 217MHz$	-	-45	-	dB

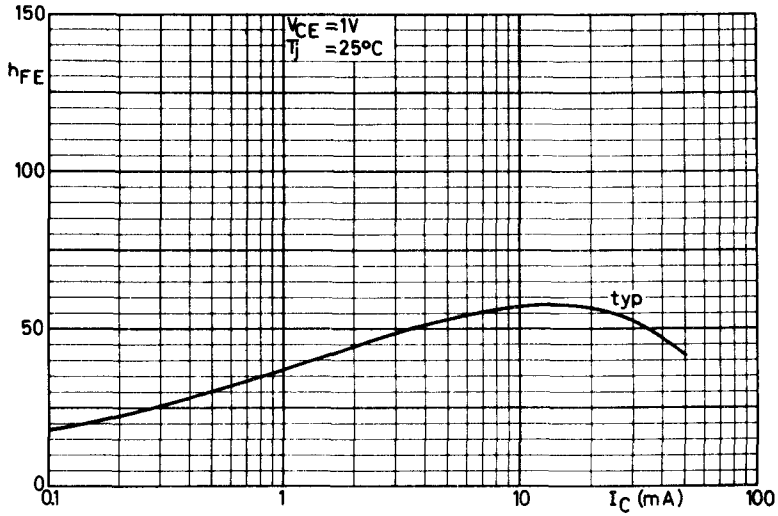
*Crystal mounted in a BFY90 envelope

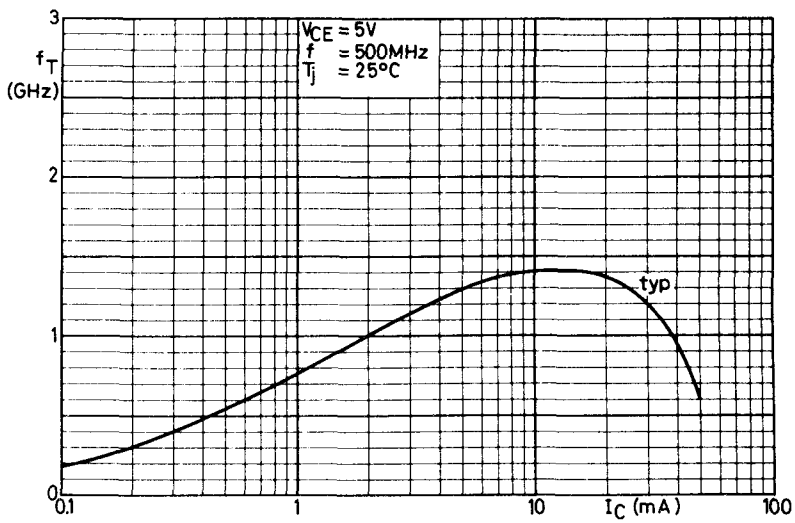

D5667
V_{CB}=10V
Typ
I_{CBO} (nA)
10
7
5
2
1
7
5
2
0.1
7
5
2
0.01
7
5
2
0.001
0
50
100
T_j (°C)
150

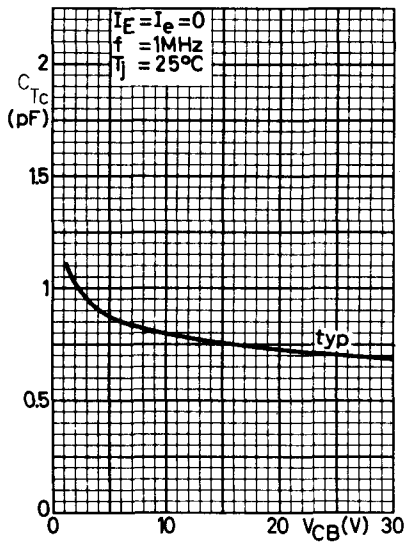

V_{CE}=1V
T_j =25°C
typ
I_C (mA)
60
40
20
0
500
700
V_{BE} (mV)
900

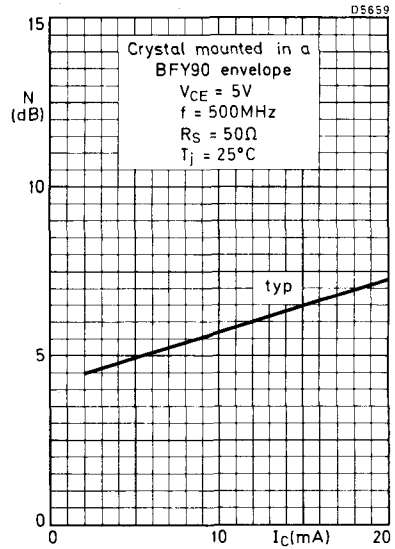

typical values
T_j =25°C
I_B=1mA
0.9mA
0.8mA
0.7mA
0.6mA
0.5mA
0.4mA
0.3mA
0.2mA
0.1mA
I_C (mA)
60
40
20
0
0
1
V_{CE} (V)
2

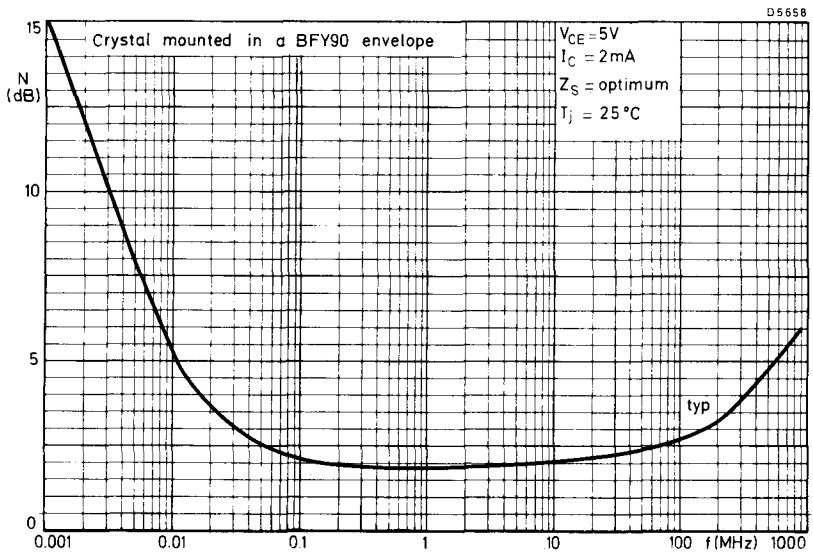

typical values
T_j = 25°C
I_B = 1mA
0.9mA
0.8mA
0.7mA
0.6mA
0.5mA
0.4mA
0.3mA
0.2mA
0.1mA
I_C (mA)
60
40
20
0
0
10
V_{CE} (V)
20


150
h_{FE}
100
50
0
0.1
1
10
100
I_C (mA)
V_{CE} = 1V
T_j = 25°C
typ


3
f_T
(GHz)
2
1
0
0.1
1
10
100
I_C (mA)
V_{CE} = 5V
f = 500MHz
T_j = 25°C
typ


$I_E = I_e = 0$
f = 1MHz
T_j = 25°C
C_{TC} (pF)
2
1.5
1
0.5
0
0
10
20
V_{CB}(V)
30
typ


D5659
Crystal mounted in a BFY90 envelope
V_{CE} = 5V
f = 500MHz
R_S = 50Ω
T_j = 25°C
N (dB)
15
10
5
0
0
10
I_C(mA)
20
typ


D5658
Crystal mounted in a BFY90 envelope
V_{CE} = 5V
I_C = 2mA
Z_S = optimum
T_j = 25°C
N (dB)
15
10
5
0
0.001
0.01
0.1
1
10
100
f(MHz)
1000
typ

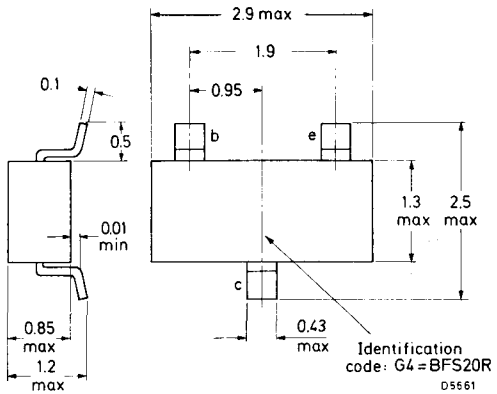
μ min. N-P-N SILICON PLANAR EPITAXIAL TRANSISTOR

BFS20R

Silicon n-p-n planar epitaxial transistor in a microminiature plastic envelope, intended for i.f. and v.h.f. applications in thin and thick films. The device features a very low feedback capacitance.

QUICK REFERENCE DATA			
V_{CBO}	max.	30	V
V_{CEO}	max.	20	V
I_C	max.	25	mA
P_{tot}	max. $T_{amb} \leq 25^oC$	200	mW
T_j	max.	150	^oC
h_{FE}	min., I_C = 7mA, V_{CE} = 10V	40	
f_T	typ., I_C = 5mA, V_{CE} = 5V, f = 100MHz	450	MHz
$-C_{re}$	max., I_C = 1mA, V_{CE} = 10V, f = 1MHz	0.4	pF

OUTLINE AND DIMENSIONS



All dimensions in millimetres

Plan view from above

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{CBO}	max.		30	V
V_{CEO}	max.	(I_C = 2.0mA)	20	V
V_{EBO}	max.		4.0	V
I_C	max.		25	mA
I_{CM}	max.		25	mA
P_{tot}	max.	$T_{amb} \leq 25^oC$, mounted on a ceramic substrate of 7 × 5 × 0.5mm	200	mW

Temperature

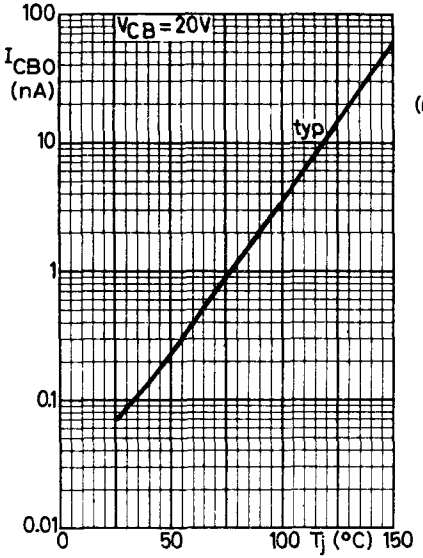
T_{stg}		-65 to +150	^oC
T_j	max.	150	^oC

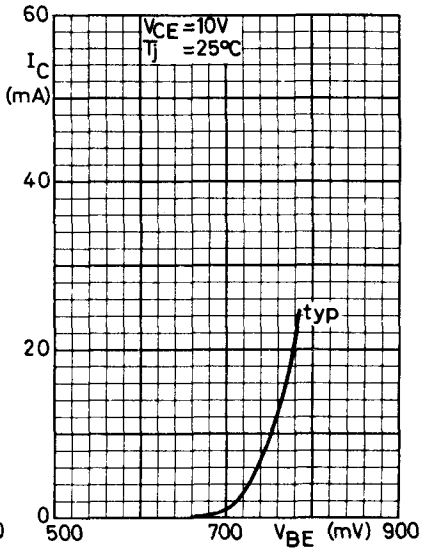
THERMAL CHARACTERISTICS

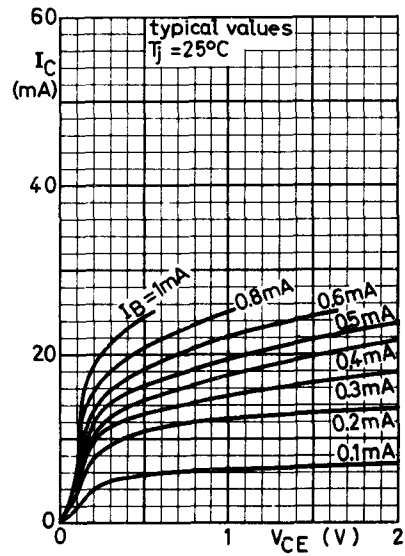
$R_{th(j-amb)}$	Thermal resistance between junction and ambient, the device mounted on a ceramic substrate of 7 × 5 × 0.5mm	0.62	$^oC/mW$

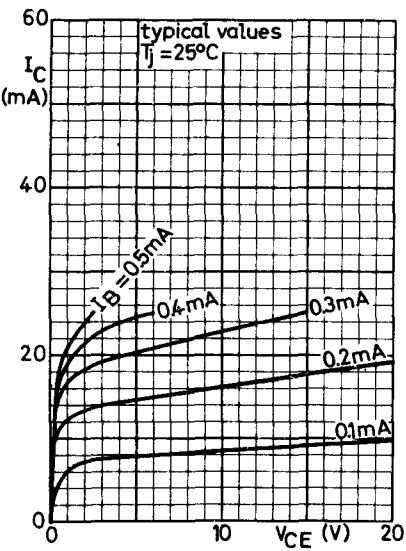
ELECTRICAL CHARACTERISTICS ($T_j = 25^oC$ unless otherwise stated)

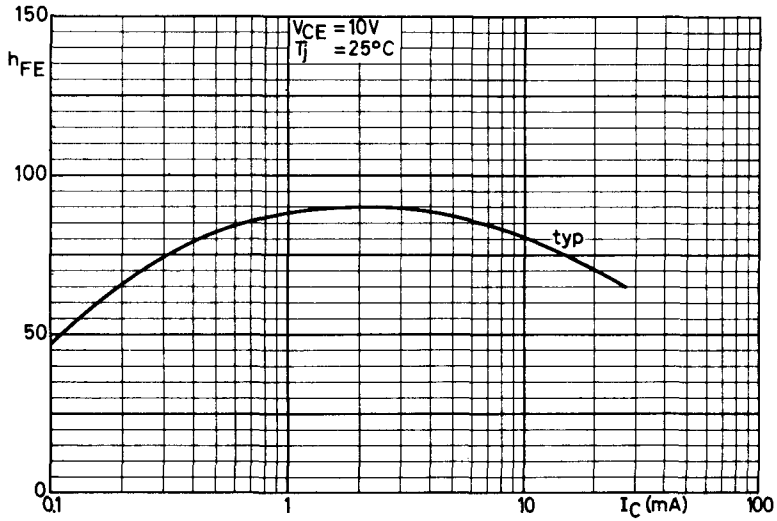
		Min.	Typ.	Max.	
I_{CBO}	Collector cut-off current				
	I_E = 0, V_{CB} = 20V	-	-	100	nA
	I_E = 0, V_{CB} = 20V, $T_j = 100^oC$	-	-	10	μA
V_{BE}	Base-emitter voltage				
	I_C = 7.0mA, V_{CE} = 10V	-	740	900	mV
h_{FE}	Static forward current transfer ratio				
	I_C = 7.0mA, V_{CE} = 10V	40	85	-	
f_T	Transition frequency				
	I_C = 5.0mA, V_{CE} = 10V, f = 100MHz	275	450	-	MHz
$-C_{re}$	Feedback capacitance				
	I_C = 1.0mA, V_{CE} = 10V, f = 1.0MHz	-	0.35	0.40	pF
C_{Tc}	Collector capacitance				
	$I_E = I_e$ = 0, V_{CB} = 10V, f = 1.0MHz	-	0.8	-	pF

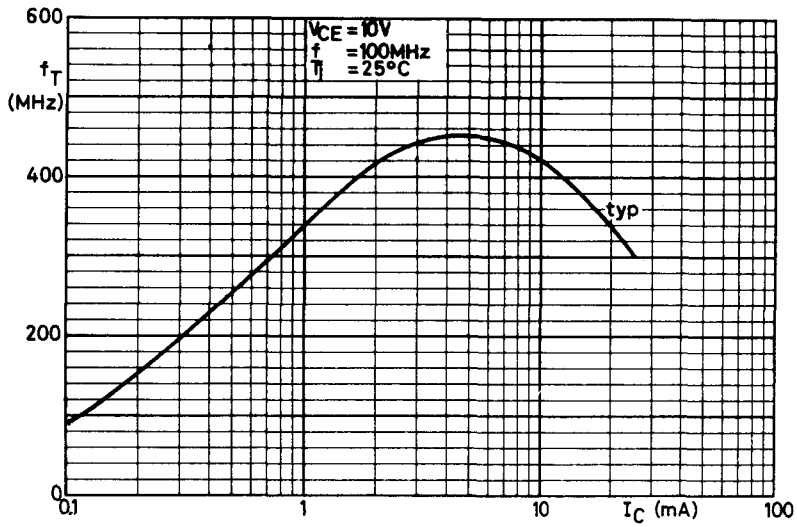

100
I_{CBO} (nA)
10
1
0.1
0.01
V_{CB} = 20V
typ
0
50
100 T_j (°C) 150

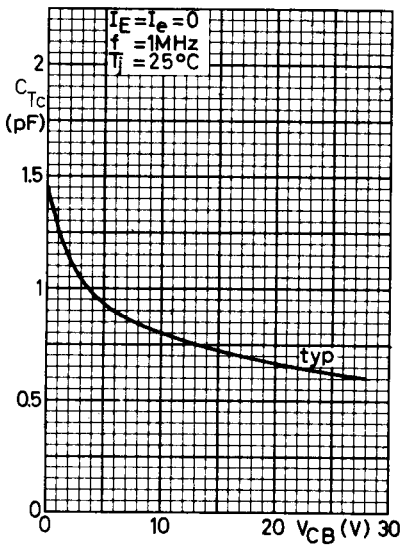

60
I_C (mA)
40
20
0
V_{CE} = 10V
T_j = 25°C
typ
500
700
V_{BE} (mV) 900


60
I_C (mA)
40
20
0
typical values
T_j = 25°C
I_B = 1mA
0.8mA
0.6mA
0.5mA
0.4mA
0.3mA
0.2mA
0.1mA
0
1
V_{CE} (V)
2


60
I_C (mA)
40
20
0
typical values
T_j = 25°C
I_B = 0.5mA
0.4mA
0.3mA
0.2mA
0.1mA
0
10
V_{CE} (V)
20


150
h_{FE}
100
50
0
0.1
1
10
I_C (mA)
100
V_{CE} = 10V
T_j = 25°C
typ


600
f_T
(MHz)
400
200
0
0.1
1
10
I_C (mA)
100
V_{CE} = 10V
f = 100MHz
T_j = 25°C
typ


$I_E = I_e = 0$
f = 1MHz
T_j = 25°C
C_{Tc} (pF)
2
1.5
1
0.5
0
typ
0
10
20
V_{CB} (V)
30

MATCHED N-CHANNEL FIELD-EFFECT TRANSISTORS

BFS21A
BFS21

Two matched N-channel silicon epitaxial planar junction-gate field-effect transistors in TO-72 metal envelopes, mounted together in an S-clip.
This device is intended for low level differential amplifiers, sample and hold circuits, chopper circuits, etc. in instrumentation and control.

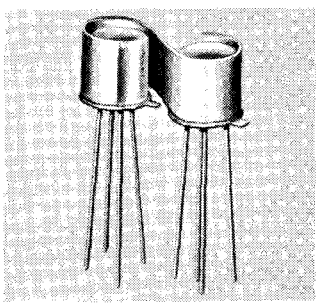
QUICK REFERENCE DATA

		BFS21	BFS21A	
I_G	Gate cut-off leakage current $T_{amb}=25^oC$, $V_{DG}=15V$, $I_D=0.5mA$	<0.5	<0.5	nA
$\lvert \Delta V_{GS} \rvert$	Differential gate-source voltage $T_{amb}=25^oC$, $V_{DG}=15V$, $I_D=0.5mA$	<20	<10	mV
$\left\lvert \frac{d\,\Delta V_{GS}}{dT} \right\rvert$	Thermal drift of differential gate-source voltage $T_{amb}=25^oC$, $V_{DG}=15V$, $I_D=0.5mA$	<75	<40	μV/degC
$\left\lvert \Delta \frac{g_{os}}{g_{fs}} \right\rvert$	Difference of penetration factors $T_{amb}=25^oC$, $V_{DG}=15V$, $I_D=0.5mA$	<1.0	<0.5	$\times 10^{-3}$
$\left\lvert \Delta \frac{1}{g_{fs}} \right\rvert$	Difference of transfer impedances $T_{amb}=25^oC$, $V_{DG}=15V$, $I_D=0.5mA$	<15	<7.5	Ω
C M R R	Common mode rejection ratio	>60	>66	dB

OUTLINE AND DIMENSIONS

Two devices conforming to J.E.D.E.C. TO-72 mounted in an S clip

For details see page 5



RATINGS (of the total device)

Limiting values of operation according to the absolute maximum system

Electrical

$V_{max.}$	Voltage between any two terminals	30	V
I_D max.	Drain current	4.0	mA
I_G max.	Gate current	0.5	mA
P_{tot} max.	Total power dissipation ($T_{clip} < 100^oC$)	30	mW

Temperature

T_{amb}	Operating ambient temperature	-20 to +100	^oC

ELECTRICAL CHARACTERISTICS (total device, $T_{amb} = 25^oC$ unless otherwise stated)

		BFS21	BFS21A	
$\frac{I_{DSS1}}{I_{DSS2}}$	Drain current ratio $V_{DG} = 15V$, $V_{GS} = 0$, $T_j = 25^oC$	>0.95 <1.05	>0.95 <1.05	
$\lvert V_{GS1} - V_{GS2} \rvert$	Differential gate-source voltage $I_D = 500\mu A$, $V_{DG} = 15V$	<20	<10	mV
	$I_D = 100\mu A$, $V_{DG} = 15V$	<20	<10	mV
$\frac{\Delta \lvert V_{G1S1} - V_{G2S2} \rvert}{\Delta T_{amb}}$	Thermal drift of differential gate-source voltage $I_D = 500\mu A$, $V_{DG} = 15V$	<75	<40	$\mu V/degC$
	$I_D = 100\mu A$, $V_{DG} = 15V$	<75	<40	$\mu V/degC$
$\Delta \lvert V_{G1S1} - V_{G2S2} \rvert$	*Differential gate-source voltage change with ambient temperature $T_{amb} = 25$ to 100^oC			
	$I_D = 500\mu A$, $V_{DG} = 15V$	<6	<3	mV
	$I_D = 100\mu A$, $V_{DG} = 15V$	<6	<3	mV
$\lvert \Delta \frac{g_{os}}{g_{fs}} \rvert$	Difference of penetration factors (see note 1) $I_D = 500\mu A$, $V_{DG} = 15V$	<1	<0.5	10^{-3}
	$I_D = 100\mu A$, $V_{DG} = 15V$	<1	<0.5	10^{-3}
$\lvert \Delta \frac{1}{g_{fs}} \rvert$	Difference of transfer impedances (see note 2) $I_D = 500\mu A$, $V_{DG} = 15V$	<15	<7.5	Ω
	$I_D = 100\mu A$, $V_{DG} = 15V$	<75	<37.5	Ω
C M R R	Common mode rejection ratio (see note 3) $I_D = 500\mu A$, $V_{DG} = 15V$	>60	>66	dB
	$I_D = 100\mu A$, $V_{DG} = 15V$	>60	>66	dB

*Differential gate-source voltage change with ambient temperature $= \lvert V_{G1S1} - V_{G2S2} \rvert T_{amb2} - \lvert V_{G1S1} - V_{G2S2} \rvert T_{amb1}$

ELECTRICAL CHARACTERISTICS (contd.)

NOTES

1. The difference between the penetration factors is equal to the ratio of the change of the differential gate-source voltage (ΔV_{GS}) to the change of drain-gate voltage (V_{DG}) with the drain current (I_D) constant.

   i.e.

$$\Delta \frac{g_{os}}{g_{fs}} = \frac{d\,\Delta V_{GS}}{d\,V_{DG}} \qquad \text{at } I_D = \text{constant}$$

2. The difference between the transfer impedances is equal to the ratio of the change of the differential gate-source voltage (ΔV_{GS}) to the change of drain current (I_D), with the drain-gate voltage (V_{DG}) constant.

   i.e.

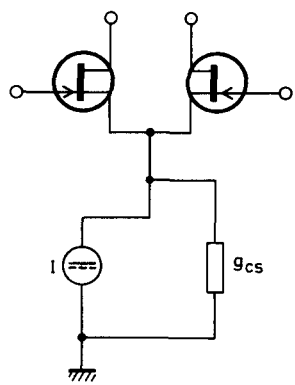
$$\Delta \frac{1}{g_{fs}} = \frac{d\,\Delta V_{GS}}{d\,I_D} \qquad \text{at } V_{DG} = \text{constant}$$

3. The common mode rejection ratio

$$\frac{1}{C\,M\,R\,R} = \Delta \frac{g_{os}}{g_{fs}} + \frac{1}{2}\, g_{cs} \,.\, \Delta \frac{1}{g_{fs}}$$

   where g_{os} in this formula is the output conductance of the summing current source.

   The guaranteed values of C M R R apply at $g_{cs} = 0.1\mu$mho.



RATINGS (of the individual field-effect transistor)

Limiting values of operation according to the absolute maximum system.

Electrical

$\pm V_{DS}$ max.	Drain-source voltage	30	V
V_{DGO} max.	Drain-gate voltage (open source)	30	V
$-V_{GSO}$ max.	Gate-source voltage (open drain)	30	V
I_D max.	Drain current	20	mA
I_G max.	Gate current	10	mA
P_{tot} max.	Power dissipation ($T_{amb} < 25^oC$)	300	mW

Temperature

T_{stg}	Storage temperature	-65 to +200	^oC
T_j max.	Junction temperature	+200	^oC

THERMAL CHARACTERISTIC

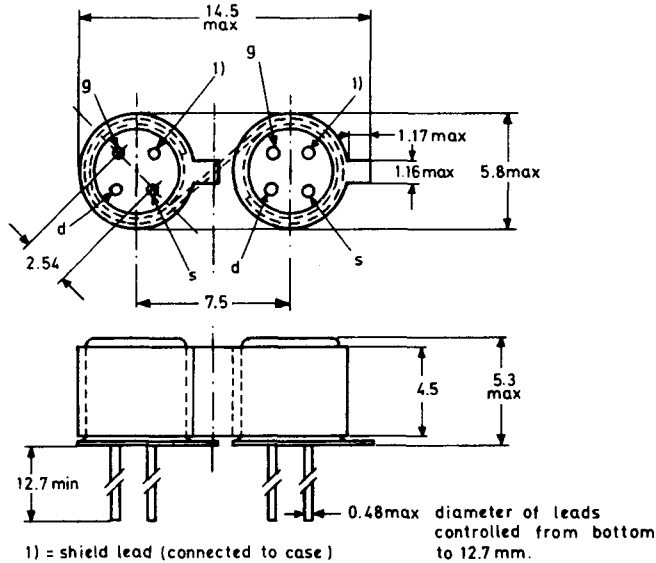
$R_{th(j-amb)}$	for individual transistor without S-clip in free air	0.59	degC/mW

ELECTRICAL CHARACTERISTICS (of the individual field-effect transistor)

$T_{amb} = 25^oC$ unless otherwise stated

I_G	Gate cut-off leakage current		
	$I_D = 500\mu A$, $V_{DG} = 15V$	< 0.5	nA
	$I_D = 500\mu A$, $V_{DG} = 15V$, $T_{amb} = 100^oC$	< 25	nA
I_{DSS}	Drain current		
	$V_{DG} = 15V$, $V_{GS} = 0$, $T_j = 25^oC$	> 1.0	mA
$-V_{(P)GS}$	Gate-source cut-off voltage		
	$I_D = 0.5nA$, $V_{DG} = 15V$	< 6.0	V
g_{fs}	Transfer conductance		
	$I_D = 500\mu A$, $V_{DG} = 15V$, $f = 1kHz$	> 1.0	mmho
g_{os}	Output conductance		
	$I_D = 500\mu A$, $V_{DG} = 15V$, $f = 1kHz$	< 15	μmho
C_{is}	Input capacitance		
	$I_D = 500\mu A$, $V_{DG} = 15V$, $f = 1MHz$	< 5.0	pF
C_{rs}	Feedback capacitance		
	$I_D = 500\mu A$, $V_{DG} = 15V$, $f = 1MHz$	< 0.75	pF
$\frac{V_n}{\sqrt{B}}$	Equivalent noise voltage (B = 5Hz)		
	$I_D = 500\mu A$, $V_{DG} = 15V$, $f = 10Hz$	< 200	$nV/\sqrt{Hz}$
	$V_{DG} = 15V$, $V_{GS} = 0$, $f = 10Hz$	< 75	$nV/\sqrt{Hz}$

OUTLINE AND DIMENSIONS



All dimensions in mm

D1222

SOLDERING AND WIRING RECOMMENDATIONS

1. Devices may be soldered directly into a circuit with a soldering iron at a maximum iron temperature of 245°C for a time of up to 10 seconds at least 1.5mm from the seal. At an iron temperature of 245°C to 400°C the maximum soldering time is 5 seconds at least 5mm from the seal.

2. These devices may be dip-soldered at a solder temperature of 245°C for a maximum soldering time of 5 seconds. The case temperature during dip-soldering must not at any time exceed the maximum storage temperature. These recommendations apply to a device mounted flush on a board having punched-through holes, or spaced at least 1.5mm above a board having plated-through holes.

3. Care should be taken not to bend the leads nearer than 1.5mm from the seal.

4. If devices are stored at temperatures above 100°C before incorporation into equipment, some deterioration of the external surface is likely to occur which may make soldering into the circuit difficult. Under these circumstances the leads should be retinned using a suitable activated flux.

SILICON N-CHANNEL DUAL-INSULATED-GATE FIELD-EFFECT TRANSISTOR

BFS28

The BFS28 is a silicon n-channel, depletion-type dual-insulated-gate M.O.S. field effect transistor. It is intended for a wide range of applications in communications, instrumentation and control.

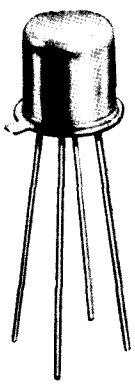
QUICK REFERENCE DATA

V_{DS} max.	Drain-source voltage	20	V
$\pm V_{G1S}$ max.	Gate 1-source voltage	8.0	V
$\pm V_{G2S}$ max.	Gate 2-source voltage	8.0	V
I_D max.	Drain current	20	mA
P_{tot} max.	Total device power dissipation ($T_{amb} \leq 25^oC$)	200	mW
T_j max.	Maximum junction temperature	135	^oC
Characteristics			
$I_D = 10mA$, $V_{DS} = 13V$, $V_{G2S} = +4.0V$			
$\lvert y_{fs} \rvert$ typ.	Small signal forward transfer admittance in common source (f = 1kHz)	13	mmho
G_a typ.	Power gain (f = 200MHz)	18	dB
$-C_{rs}$ typ.	Feedback capacitance (f = 10MHz)	25	fF
N typ.	Noise figure at optimum source admittance (f = 200MHz)	3	dB

OUTLINE AND DIMENSIONS

Conforms to J.E.D.E.C. TO-72
B.S. 3934 SO-12A/SB4-3

For details see page 4



Mullard

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{DS} max.	Drain-source voltage	20	V
$\pm V_{G1S}$ max.	Gate 1-source voltage	8.0	V
$\pm V_{G2S}$ max.	Gate 2-source voltage	8.0	V
$\pm V_{G1SM}$ max.	Non-repetitive peak gate 1-source voltage ($t \leq 10ms$)	50	V
$\pm V_{G2SM}$ max.	Non-repetitive peak gate 2-source voltage ($t \leq 10ms$)	50	V
I_D max.	Drain current	20	mA
P_{tot} max.	Total device power dissipation ($T_{amb} \leq 25^oC$)	200	mW

Temperature

T_{stg} min.	-65	^oC
T_{stg} max.	+135	^oC
T_j max.	+135	^oC

THERMAL CHARACTERISTICS

$R_{th(j-amb)}$	0.55	degC/mW

ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^oC$ unless otherwise stated)

		Min.	Typ.	Max.	
$-V_{G1S}$	Gate 1-source cut-off voltage $V_{DS} = 20V$, $I_D = 100\mu A$, $V_{G2S} = +4V$	-	-	5.0	V
$-V_{G2S}$	Gate 2-source cut-off voltage $V_{DS} = 20V$, $I_D = 50\mu A$, $V_{G1S} = 0$	-	-	4.0	V
$-V_{G1S}$	Gate 1-source voltage $I_D = 10mA$, $V_{DS} = 13V$, $V_{G2S} = +4V$	0.6	-	2.8	V
	$I_D = 4mA$, $V_{DS} = 10V$, $V_{G2S} = +4V$	1.0	-	3.2	V
$\pm I_{G1SS}$	Gate 1 leakage current $\pm V_{G1} = 8V$, $V_{G2S} = 0$, $V_{DS} = 0$, $T_j = 135^oC$	-	-	1.0	nA
$\pm I_{G2SS}$	Gate 2 leakage current $\pm V_{G2} = 8V$, $V_{G1S} = 0$, $V_{DS} = 0$, $T_j = 135^oC$	-	-	1.0	nA

ELECTRICAL CHARACTERISTICS (cont'd)

Small signal y-parameters (see also graphs on pages 6 and 7)

$I_D = 10mA$, $V_{DS} = 13V$, $V_{G2S} = +4V$, $T_{amb} = 25^oC$

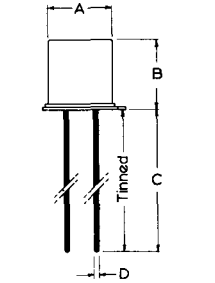
		Min.	Typ.	Max.	
$\|y_{fs}\|$	Forward transfer admittance				
	f = 1kHz	8	13	-	mmho
	f = 200MHz	-	12	-	mmho
	f = 500MHz	-	11.3	-	mmho
$-C_{rs}$	Feedback capacitance				
	f = 10MHz	-	25	-	fF
G_a	Power gain				
	$I_D = 10mA$, $V_{DS} = 13V$, $V_{G2S} = +4V$,				
	f = 200MHz, $G_S = 1.3mmho$, $G_L = 1mmho$,				
	B_S and B_L tuned for maximum gain	-	18	-	dB
G_{UM}	Max. unilateralised power gain (see note 1) $I_D = 10mA$, $V_{DS} = 13V$,				
	$V_{G2S} = +4V$, f = 200MHz	-	20.5	-	dB
	f = 500MHz	-	7.9	-	dB
N	Noise figure at optimum source admittance				
	$I_D = 10mA$, $V_{DS} = 13V$, $V_{G2S} = +4V$,				
	f = 200MHz, $G_{S(opt)}$ typ. = 1.4mmho,				
	$B_{S(opt)}$ typ. = 5.5mmho	-	3.0	4.0	dB

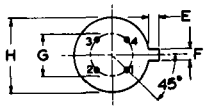
NOTE

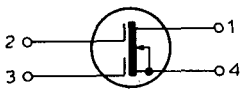
1. $G_{UM} = 10 \log \frac{y_{fs}^2}{4\, g_{is} \times g_{os}}$

OUTLINE AND DIMENSIONS

Conforms to J.E.D.E.C. TO-72







	Millimetres		
	Min.	Nom.	Max.
A	-	-	4.8
B	-	-	5.3
C	12.7	-	-
D	-	0.43	-
E	-	1.0	-
F	-	1.05	-
G	-	2.54	-
H	5.3	5.55	5.8

Connections

1. Drain
2. Gate 2
3. Gate 1
4. Source and substrate connected to case.

SOLDERING AND WIRING RECOMMENDATIONS

1. Devices may be soldered directly into a circuit with a soldering iron at a maximum iron temperature of 245°C for a time of up to 10 seconds at least 1.5mm from the seal. At an iron temperature of 245°C to 400°C the maximum soldering time is 5 seconds at least 5mm from the seal.

2. These devices may be dip-soldered at a solder temperature of 245°C for a maximum soldering time of 5 seconds. The case temperature during dip-soldering must not at any time exceed the maximum storage temperature. These recommendations apply to a device mounted flush on a board having punched-through holes, or spaced at least 1.5mm above a board having plated-through holes.

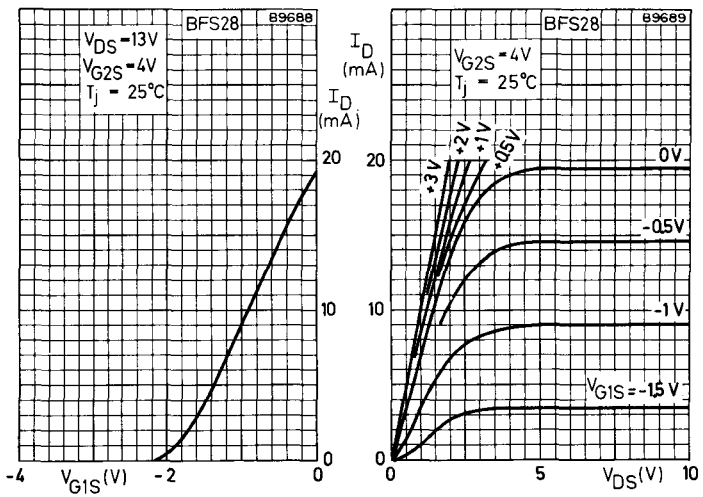
3. Care should be taken not to bend the leads nearer than 1.5mm from the seal.

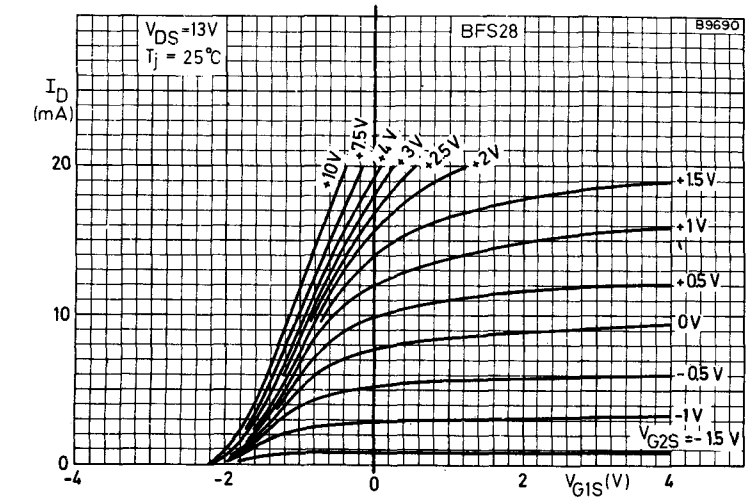
4. If devices are stored at temperatures above 100°C before incorporation into equipment, some deterioration of the external surface is likely to occur which may make soldering into the circuit difficult. Under these circumstances the leads should be retinned using a suitable activated flux.

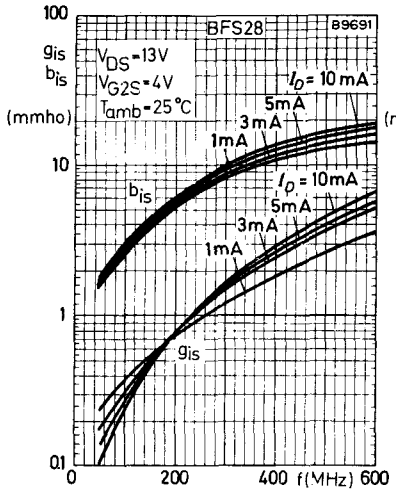
HANDLING NOTE

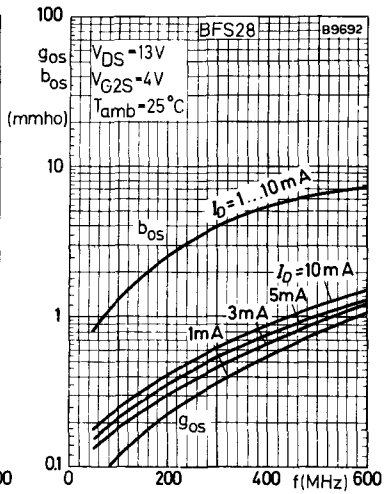
To exclude the possibility of damage to the gate oxide layer by an electrostatic charge building up on the high resistance gate electrode, the device is fitted with a conducting rubber ring around the leads. This ring should not be removed until after the device has been mounted in the circuit.


BFS28
B9687
P_{tot} max (mW)
200
100
0
0
25
50
75
100
125
150
T_{amb} (°C)


BFS28
B9688
V_{DS} = 13V
V_{G2S} = 4V
T_j = 25°C
I_D (mA)
20
10
0
-4
V_{G1S} (V)
-2
0
BFS28
B9689
I_D (mA)
V_{G2S} = 4V
T_j = 25°C
+3V
+2V
+1V
+0.5V
0V
-0.5V
-1V
V_{G1S} = -1.5V
20
10
0
0
5
V_{DS} (V)
10

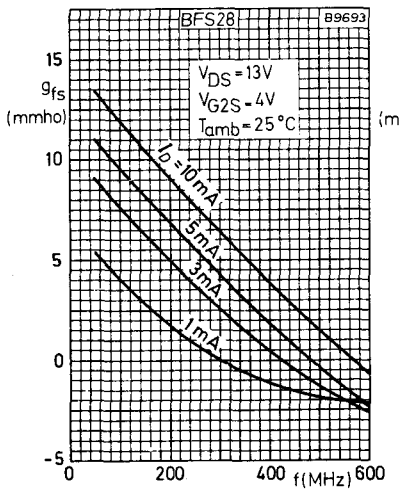

BFS28
B9690
V_{DS}=13V
T_j = 25°C
I_D (mA)
20
10
0
-4
-2
0
2
4
V_{G1S}(V)
+10V
+7.5V
+4V
+3V
+2.5V
+2V
+1.5V
+1V
+0.5V
0V
-0.5V
-1V
V_{G2S} = -1.5V

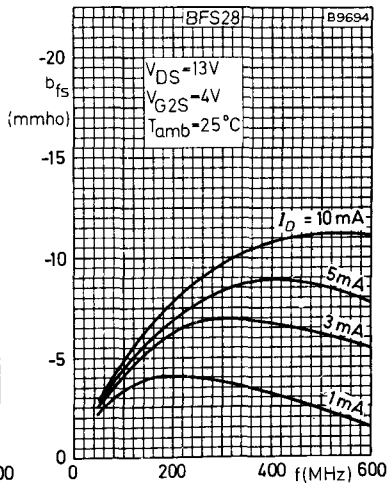

BFS28
B9691
g_{is}
b_{is}
V_{DS}=13V
V_{G2S}=4V
T_{amb}=25°C
(mmho)
100
10
1
0.1
I_D = 10 mA
5mA
3mA
1mA
b_{is}
I_D = 10mA
5mA
3mA
1mA
g_{is}
0
200
400
f(MHz)
600

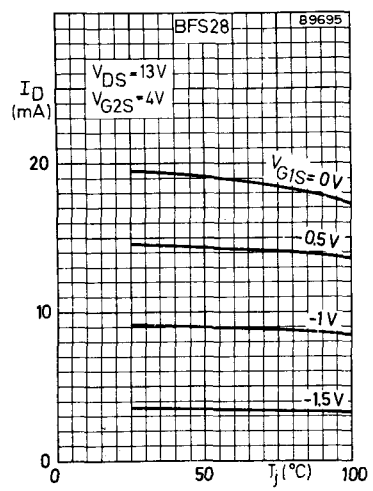

BFS28
B9692
g_{os}
b_{os}
V_{DS}=13V
V_{G2S}=4V
T_{amb}=25°C
(mmho)
100
10
1
0.1
I_D = 1...10mA
b_{os}
I_D = 10mA
5mA
3mA
1mA
g_{os}
0
200
400
f(MHz)
600

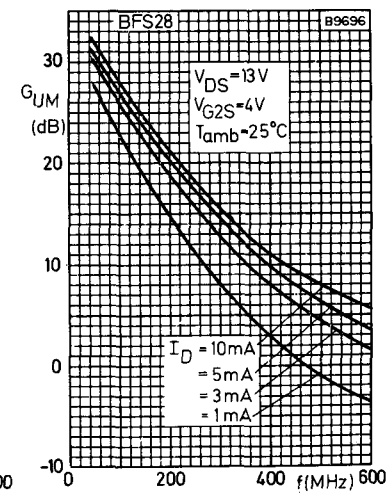
SILICON N-CHANNEL DUAL-INSULATED-GATE FIELD-EFFECT TRANSISTOR

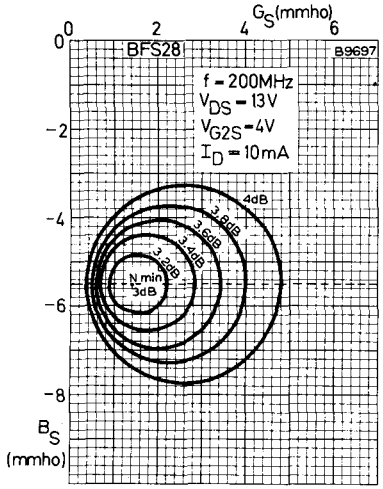
BFS28



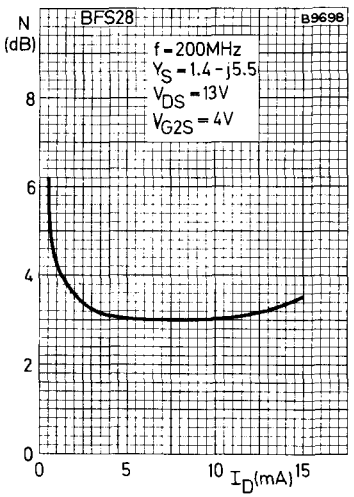








Circles of constant typical noise figure



Typical noise figure versus drain current

N-P-N SILICON PLANAR EPITAXIAL U.H.F. TRANSISTOR

BFT 24

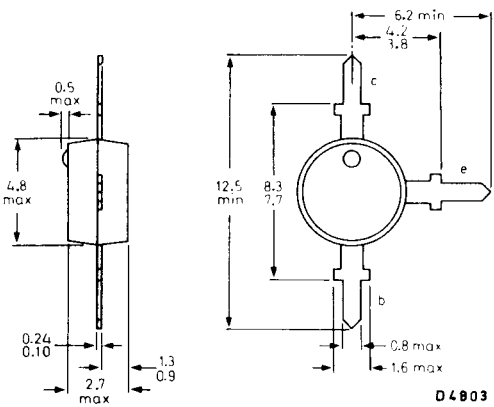
Silicon planar epitaxial n-p-n transistor in a subminiature plastic T-package, primarily intended for use in u.h.f. low power amplifiers such as in pocket phones, paging systems, etc.

The transistor features low current consumption (100μA -1mA), excellent wideband properties and low noise up to high frequencies.

QUICK REFERENCE DATA

V_{CBO}	max.	8.0	V
V_{CEO}	max.	5.0	V
I_C	max.	2.5	mA
P_{tot}	max. ($T_{amb} \leq 135^oC$)	30	mW
T_j	max.	150	^oC
f_T	typ. (I_C = 1.0mA, V_{CE} = 1.0V, f = 500MHz)	2.3	GHz
C_{re}	max. (I_C = 1.0mA, V_{CE} = 1.0V, f = 1.0MHz)	0.4	pF
N	typ. (I_C = 1.0mA, V_{CE} = 1.0V, f = 500MHz, at optimum source impedance)	3.8	dB
G_{UM}	typ. (I_C = 1.0mA, V_{CE} = 1.0V, f = 500MHz)	17	dB

OUTLINE AND DIMENSIONS



All dimensions in millimetres

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

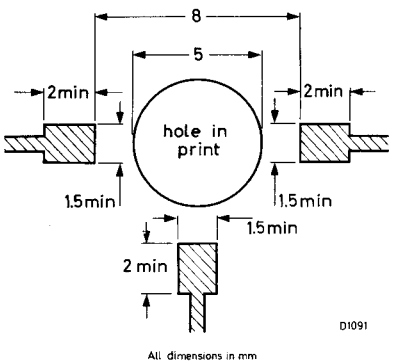
V_{CBO}	max.	8.0	V
V_{CEO}	max.	5.0	V
V_{EBO}	max.	2.0	V
I_C	max.	2.5	mA
I_{CM}	max. (peak value, f > 1.0MHz)	5.0	mA
P_{tot}	max. ($T_{amb} \leq 135^oC$)	30	mW

Temperature

T_{stg}		-65 to +150	^oC
T_j	max.	150	^oC

THERMAL CHARACTERISTIC

$R_{th\ (j\text{-}amb)}$	Thermal resistance from junction to ambient in free air, mounted on a glass-fibre print of 40×25×1mm	0.5	$^oC/mW$



All dimensions in mm

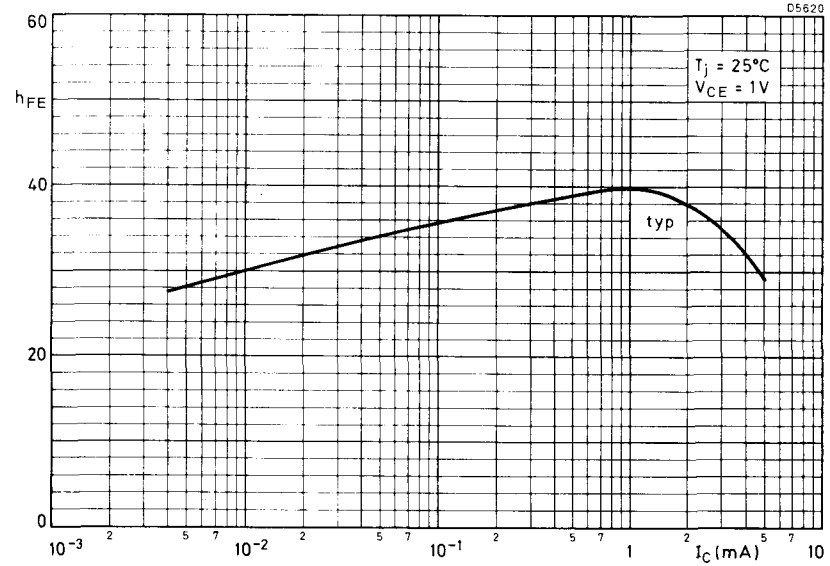
Requirements for a glass-fibre print

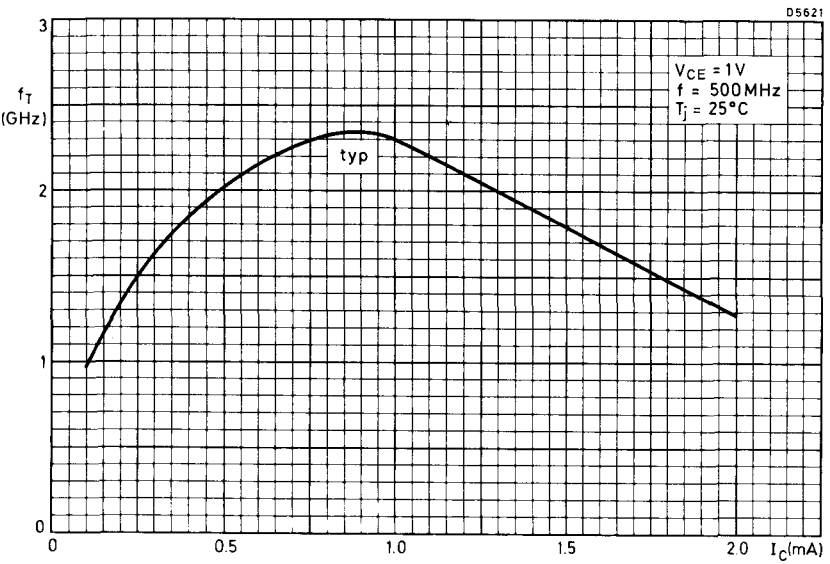
ELECTRICAL CHARACTERISTICS ($T_j = 25^oC$ unless otherwise stated)

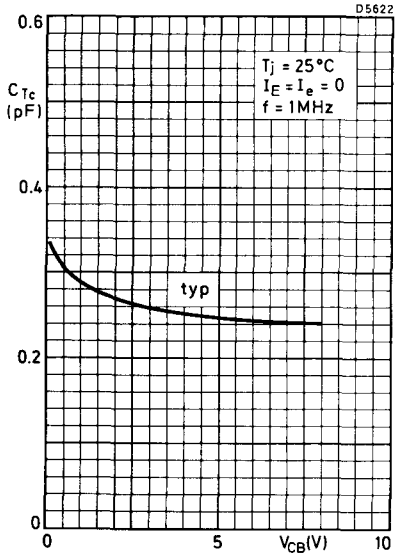
		Min.	Typ.	Max.	
I_{CBO}	Collector cut-off current $I_E = 0$, $V_{CB} = 5.0V$	-	-	50	nA
$*h_{FE}$	Static forward current transfer ratio $I_C = 10\mu A$, $V_{CE} = 1.0V$	20	30	-	
	$I_C = 1.0mA$, $V_{CE} = 1.0V$	20	40	-	
$V_{CE(sat)}$	Collector-emitter saturation voltage $I_C = 10\mu A$, $I_B = 1.0\mu A$	-	-	100	mV
	$I_C = 1.0mA$, $I_B = 0.1mA$	-	-	125	mV
$V_{BE(sat)}$	Base-emitter saturation voltage $I_C = 10\mu A$, $I_B = 1.0\mu A$	-	-	700	mV
	$I_C = 1.0mA$, $I_B = 0.1mA$	-	-	850	mV
$*f_T$	Transition frequency $I_C = 1.0mA$, $V_{CE} = 1.0V$, $f = 500MHz$	1.2	2.3	-	GHz
C_{Tc}	Collector capacitance at $f = 1.0MHz$ $I_E = I_e = 0$, $V_{CB} = 0.5V$	-	-	0.55	pF
C_{Te}	Emitter capacitance at $f = 1.0MHz$ $I_C = I_c = 0$, $V_{EB} = 0$	-	-	0.45	pF
C_{re}	Feedback capacitance at $f = 1.0MHz$ $I_C = 1.0mA$, $V_{CE} = 1.0V$, $T_{amb} = 25^oC$	-	-	0.4	pF
N	Noise figure at optimum source impedance, $f = 500MHz$, $T_{amb} = 25^oC$				
	$I_C = 0.1mA$, $V_{CE} = 1.0V$	-	5.5	-	dB
	$I_C = 1.0mA$, $V_{CE} = 1.0V$	-	3.8	-	dB
G_{UM}	Max. unilateral power gain (s_{re} assumed to be zero), $T_{amb} = 25^oC$				
	$I_C = 1.0mA$, $V_{CE} = 1.0V$, $f = 200MHz$	-	24	-	dB
	$I_C = 1.0mA$, $V_{CE} = 1.0V$, $f = 500MHz$	-	17	-	dB
	$I_C = 1.0mA$, $V_{CE} = 1.0V$, $f = 800MHz$	-	11	-	dB

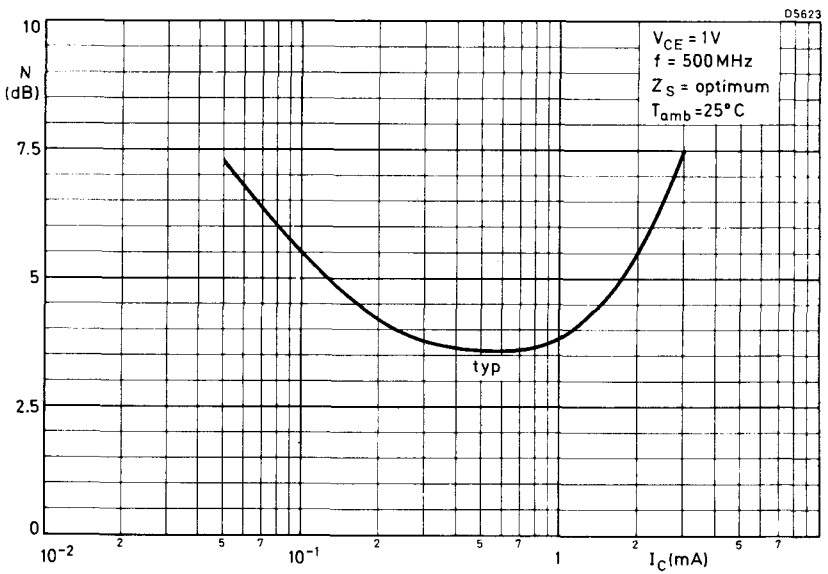
$$G_{UM}\ (\text{in dB}) = 10 \log \frac{|s_{fe}|^2}{(1 - |s_{ie}|^2)(1 - |s_{oe}|^2)}$$

*Measured under pulse conditions.

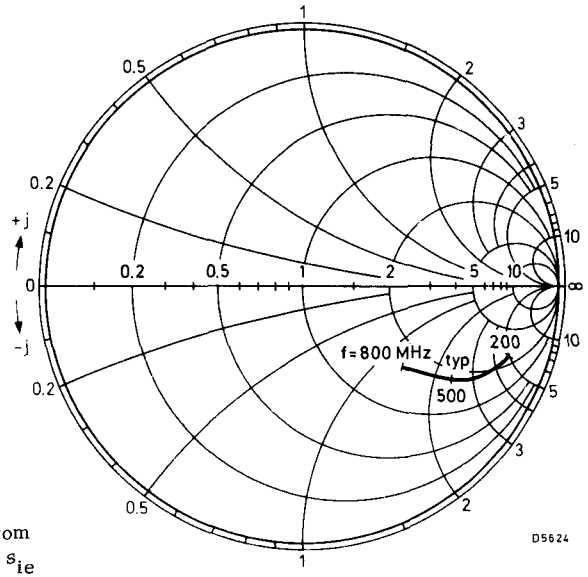

D5620
60
h_{FE}
40
20
0
T_j = 25°C
V_{CE} = 1V
typ
10^{-3}
10^{-2}
10^{-1}
1
10
I_C (mA)


D5621
3
f_T
(GHz)
2
1
0
V_{CE} = 1V
f = 500MHz
T_j = 25°C
typ
0
0.5
1.0
1.5
2.0
I_C(mA)


D5622
0.6
C_{Tc} (pF)
0.4
0.2
0
T_j = 25°C
$I_E = I_e = 0$
f = 1MHz
typ
0
5
V_{CB}(V)
10

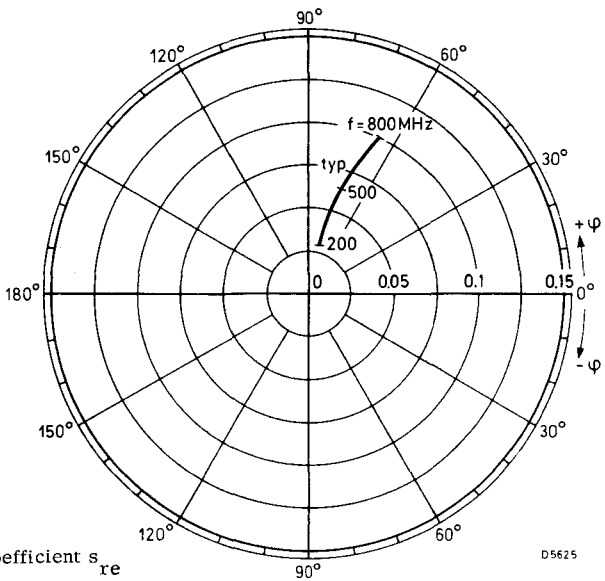

D5623
10
N (dB)
7.5
5
2.5
0
V_{CE} = 1V
f = 500MHz
Z_S = optimum
T_{amb} =25°C
typ
10^{-2}
10^{-1}
1
I_C(mA)

V_{CE} = 1.0V
I_C = 1.0mA
T_{amb} = 25°C



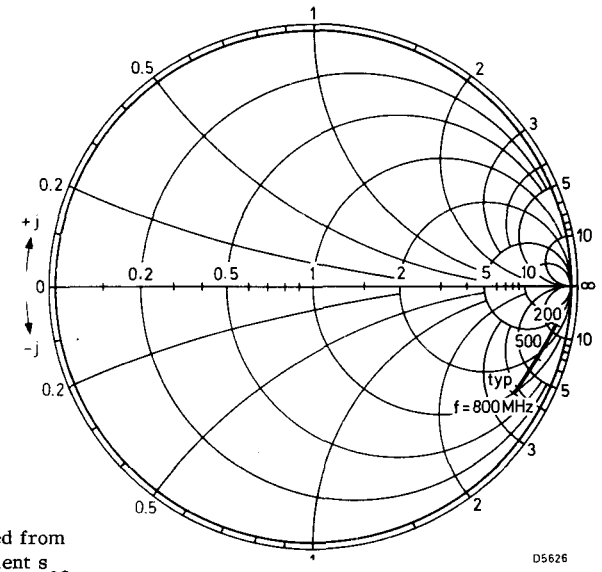
Input impedance derived from input reflection coefficient s_{ie} coordinates in ohm × 50

V_{CE} = 1.0V
I_C = 1.0mA
T_{amb} = 25°C



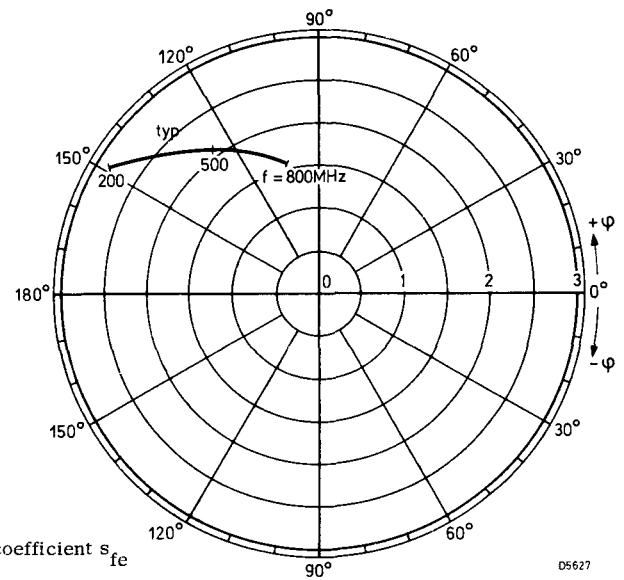
Reverse transmission coefficient s_{re}

V_{CE} = 1.0V
I_C = 1.0mA
T_{amb} = 25°C



Output impedance derived from output reflection coefficient s_{oe} coordinates in ohm × 50

V_{CE} = 1.0V
I_C = 1.0mA
T_{amb} = 25°C



Forward transmission coefficient s_{fe}

μ min. N-P-N SILICON PLANAR EPITAXIAL U.H.F. TRANSISTOR

BFT25

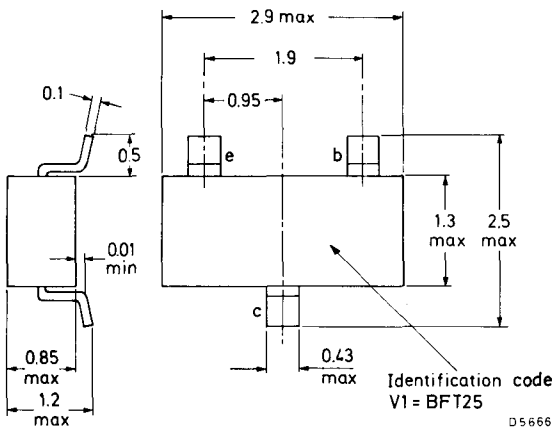
Silicon planar epitaxial n-p-n transistor in a microminiature plastic envelope, primarily intended for use in u.h.f. low power amplifiers, in thick and thin film circuits such as in pocket phones, paging systems, etc.

The transistor features low current consumption (100μA-1mA), excellent wideband properties and low noise up to high frequencies.

QUICK REFERENCE DATA

V_{CBO}	max.		8.0	V
V_{CEO}	max.		5.0	V
I_C	max.		2.5	mA
P_{tot}	max.	($T_{amb} \leq 135^oC$)	30	mW
T_j	max.		150	^oC
f_T	typ.	(I_C = 1.0mA, V_{CE} = 1.0V, f = 500MHz)	2.3	GHz
C_{re}	max.	(I_C = 1.0mA, V_{CE} = 1.0V, f = 1.0MHz)	0.45	pF
N	typ.	(I_C = 1.0mA, V_{CE} = 1.0V, f = 500MHz, at optimum source impedance)	3.8	dB
G_{UM}	typ.	(I_C = 1.0mA, V_{CE} = 1.0V, f = 500MHz)	18	dB

OUTLINE AND DIMENSIONS



All dimensions in millimetres

Plan view from above

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{CBO}	max.		8.0	V
V_{CEO}	max.		5.0	V
V_{EBO}	max.		2.0	V
I_C	max.		2.5	mA
I_{CM}	max.	(peak value, f > 1.0MHz)	5.0	mA
P_{tot}	max.	($T_{amb} \leq 135^oC$, mounted on a ceramic substrate of 15×10×0.5mm	30	mW

Temperature

T_{stg}		-65 to +150	^oC
T_j	max.	150	^oC

THERMAL CHARACTERISTIC

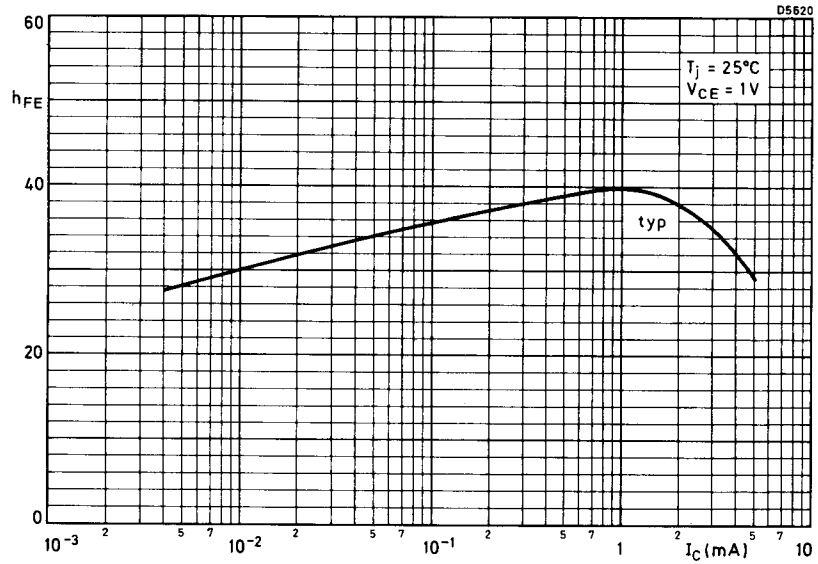
$R_{th(j\text{-}amb)}$	Thermal resistance from junction to ambient in free air, mounted on a ceramic substrate of 15×10×0.5mm	0.5	$^oC/mW$

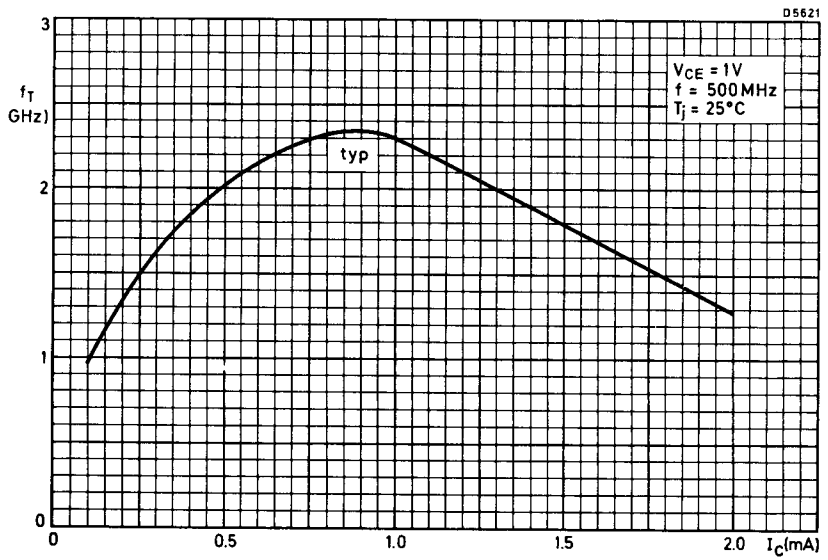
ELECTRICAL CHARACTERISTICS ($T_j = 25^oC$ unless otherwise stated)

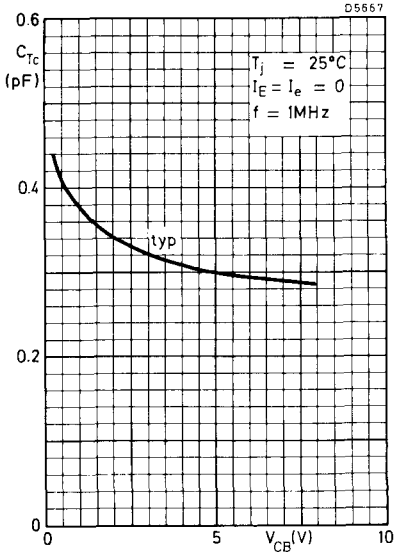
		Min.	Typ.	Max.	
I_{CBO}	Collector cut-off current				
	$I_E = 0$, $V_{CB} = 5.0V$	-	-	50	nA
$*h_{FE}$	Static forward current transfer ratio				
	$I_C = 10\mu A$, $V_{CE} = 1.0V$	20	30	-	
	$I_C = 1.0mA$, $V_{CE} = 1.0V$	20	40	-	
$V_{CE(sat)}$	Collector-emitter saturation voltage				
	$I_C = 10\mu A$, $I_B = 1.0\mu A$	-	-	200	mV
	$I_C = 1.0mA$, $I_B = 0.1mA$	-	-	175	mV
$V_{BE(sat)}$	Base-emitter saturation voltage				
	$I_C = 10\mu A$, $I_B = 1.0\mu A$	-	-	750	mV
	$I_C = 1.0mA$, $I_B = 0.1mA$	-	-	900	mV
$*f_T$	Transition frequency				
	$I_C = 1.0mA$, $V_{CE} = 1.0V$, $f = 500MHz$	1.2	2.3	-	GHz
C_{Tc}	Collector capacitance at $f = 1.0MHz$				
	$I_E = I_e = 0$, $V_{CB} = 0.5V$	-	-	0.6	pF
C_{Te}	Emitter capacitance at $f = 1.0MHz$				
	$I_C = I_c = 0$, $V_{EB} = 0$	-	-	0.5	pF
C_{re}	Feedback capacitance at $f = 1.0MHz$				
	$I_C = 1.0mA$, $V_{CE} = 1.0V$, $T_{amb} = 25^oC$	-	-	0.45	pF
N	Noise figure at optimum source impedance, $f = 500MHz$, $T_{amb} = 25^oC$				
	$I_C = 0.1mA$, $V_{CE} = 1.0V$	-	5.5	-	dB
	$I_C = 1.0mA$, $V_{CE} = 1.0V$	-	3.8	-	dB
G_{UM}	Max. unilateral power gain (s_{re} assumed to be zero), $T_{amb} = 25^oC$				
	$I_C = 1.0mA$, $V_{CE} = 1.0V$, $f = 200MHz$	-	25	-	dB
	$I_C = 1.0mA$, $V_{CE} = 1.0V$, $f = 500MHz$	-	18	-	dB
	$I_C = 1.0mA$, $V_{CE} = 1.0V$, $f = 800MHz$	-	12	-	dB

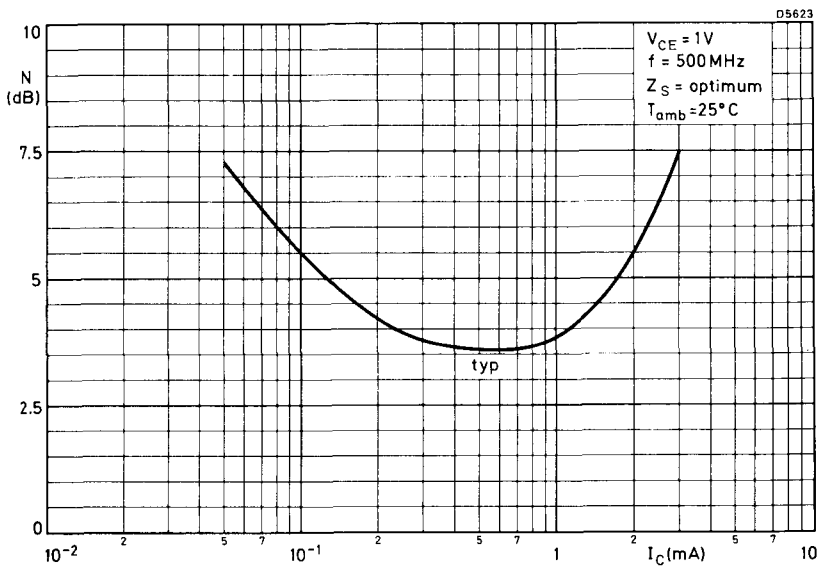
$$G_{UM}\ (\text{in dB}) = 10 \log \frac{|s_{fe}|^2}{(1 - |s_{ie}|^2)(1 - |s_{oe}|^2)}$$

*Measured under pulse conditions.

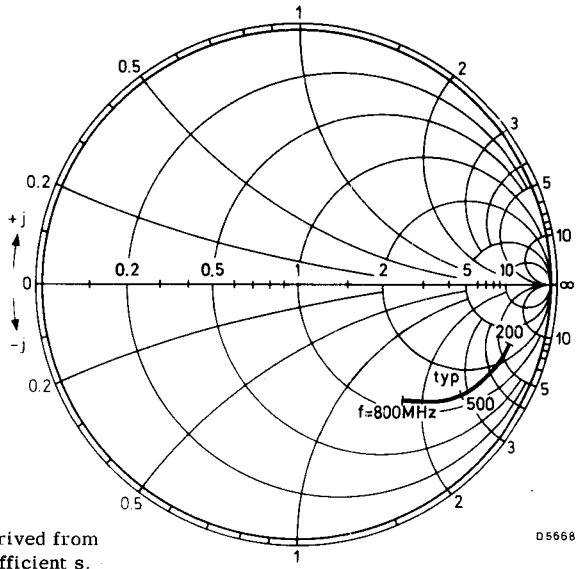

D5620
60
h_{FE}
40
20
0
T_j = 25°C
V_{CE} = 1V
typ
10^{-3}
10^{-2}
10^{-1}
1
10
I_C (mA)


D5621
3
f_T GHz)
2
1
0
V_{CE} = 1V
f = 500MHz
T_j = 25°C
typ
0
0.5
1.0
1.5
2.0
I_C(mA)


D5667
0.6
C_{Tc} (pF)
T_j = 25°C
$I_E = I_e$ = 0
f = 1MHz
0.4
typ
0.2
0
0
5
V_{CB}(V)
10

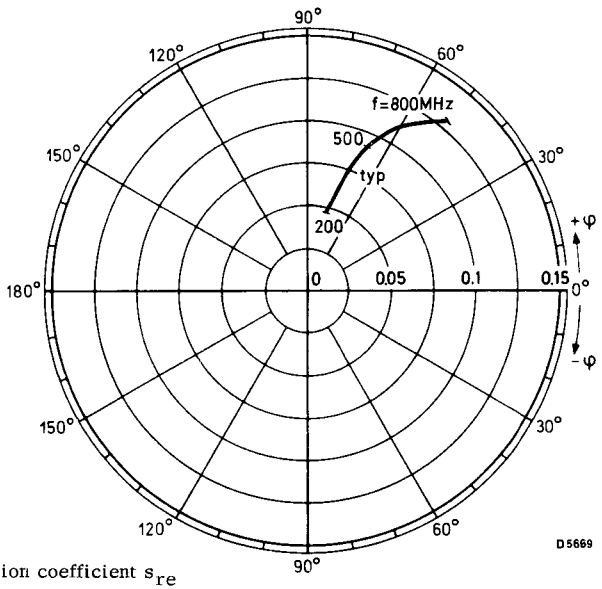

D5623
10
N (dB)
V_{CE} = 1V
f = 500MHz
Z_S = optimum
T_{amb} = 25°C
7.5
5
typ
2.5
0
10^{-2}
2
5
7
10^{-1}
2
5
7
1
2
5
7
10
I_C(mA)

V_{CE} = 1.0V
I_C = 1.0mA
T_{amb} = 25°C



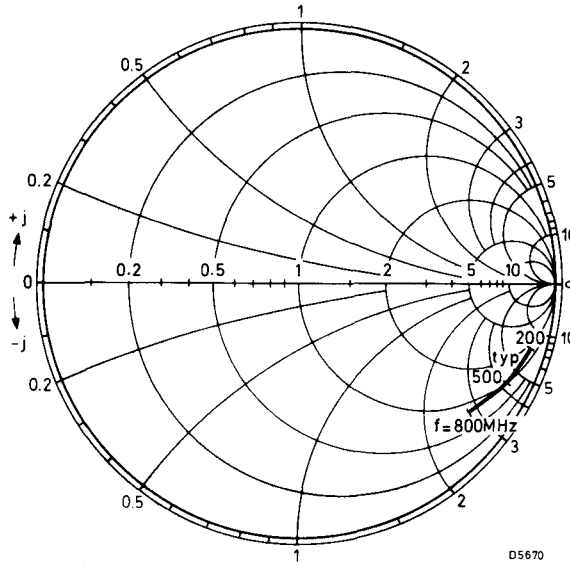
Input impedance derived from input reflection coefficient s_{ie} coordinates in ohm × 50

V_{CE} = 1.0V
I_C = 1.0mA
T_{amb} = 25°C



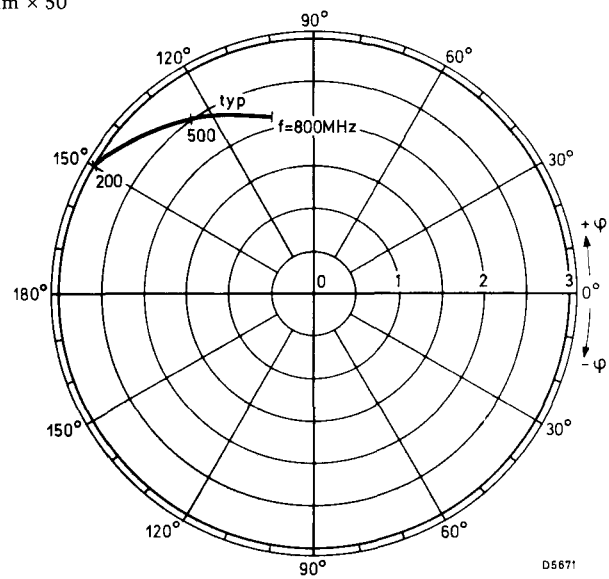
Reverse transmission coefficient s_{re}

V_{CE} = 1.0V
I_C = 1.0mA
T_{amb} = 25°C



Output impedance derived from output reflection coefficient s_{oe} coordinates in ohm × 50

V_{CE} = 1.0V
I_C = 1.0mA
T_{amb} = 25°C



Forward transmission coefficient s_{fe}

N-CHANNEL SILICON FIELD EFFECT TRANSISTORS

BFW10 BFW11

N-Channel depletion mode silicon epitaxial planar junction field effect transistors designed for use in wide-band amplifiers (0 to 300MHz). Their very low noise figure at low frequencies makes them suitable for differential amplifiers, electromedical and nuclear detector pre-amplifiers. They are in TO-72 encapsulation with a shield lead connected to case.

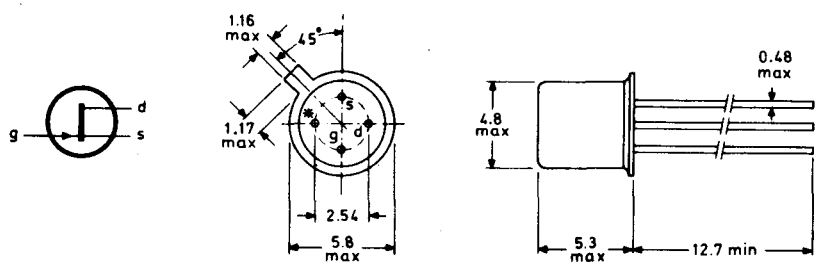
QUICK REFERENCE DATA

$\pm V_{DS}$ max.	30		V
$-V_{GSO}$ max. (open drain)	30		V
P_{tot} max. ($T_{amb} \leq 25^{\circ}C$)	300		mW
	BFW10	BFW11	
I_{DSS} ($V_{DS} = 15V$, $V_{GS} = 0$) min.	8.0	4.0	mA
max.	20	10	mA
$-V_{(P)GS}$ max. ($I_D = 0.5nA$, $V_{DS} = 15V$)	8.0	6.0	V
$-C_{rs}$ max. ($f = 1.0MHz$, $V_{DS} = 15V$, $V_{GS} = 0$)	0.80	0.80	pF
$\lvert y_{fs} \rvert$ min. ($f = 200MHz$, $V_{DS} = 15V$, $V_{GS} = 0$)	3.2	3.2	mA/V
N max. ($f = 100MHz$, $V_{DS} = 15V$, $V_{GS} = 0$, $R_G = 1k\Omega$)	2.5	2.5	dB
$V_n/\sqrt{B}$ max. ($f = 10Hz$, $B = 5.0Hz$)	75	75	$nV/\sqrt{Hz}$

Unless otherwise stated, data are applicable to both types

OUTLINE AND DIMENSIONS

Conforms to J.E.D.E.C. TO-72
B.S. 3934 SO-12A/SB4-3



All dimensions in mm

D2967

Insulated electrodes *Shield lead (connected to case)

Accessories available: 56246, 56263

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

$\pm V_{DS}$ max.	Drain-source voltage ($V_{GS} = 0$)	30	V
V_{DGO} max.	Drain-gate voltage (open source)	30	V
$-V_{GSO}$ max.	Gate-source voltage (open drain)	30	V
I_D max.	Drain current	20	mA
I_G max.	Gate current	10	mA
P_{tot} max.	Power dissipation ($T_{amb} \leq 25^oC$)	300	mW

Temperature

T_{stg} min.	-65	^oC
T_{stg} max.	200	^oC
T_j max.	200	^oC

THERMAL CHARACTERISTIC

$R_{th(j-amb)}$	0.59	$^oC/mW$

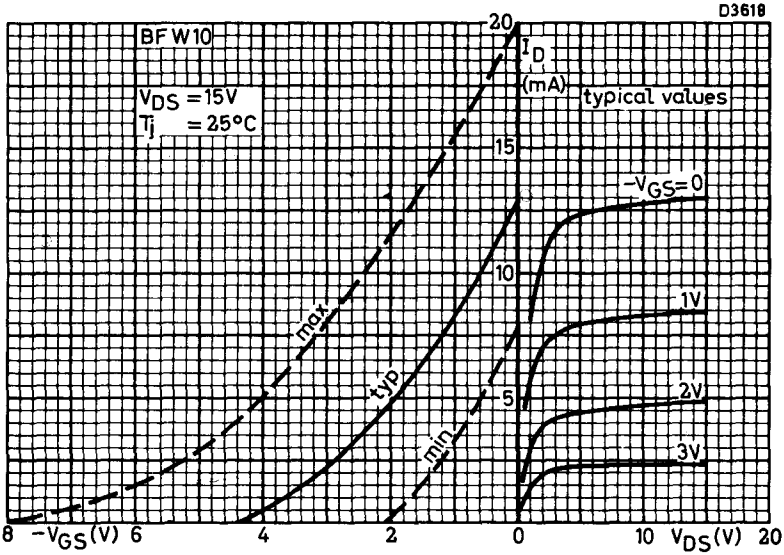
ELECTRICAL CHARACTERISTICS ($T_j = 25^oC$ unless otherwise stated)

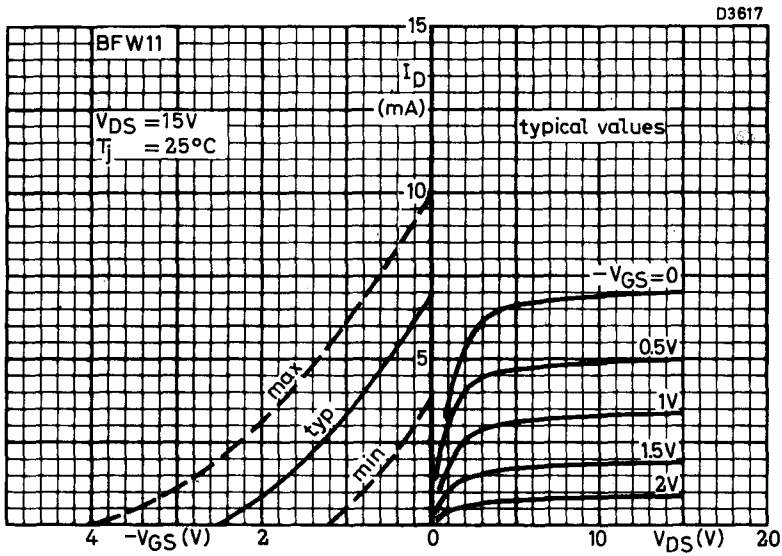
			BFW10	BFW11	
$-I_{GSS}$	Gate cut-off current				
	$-V_{GS} = 20V$, $V_{DS} = 0$	max.	0.1	0.1	nA
	$-V_{GS} = 20V$, $V_{DS} = 0$, $T_j = 150^oC$	max.	0.5	0.5	μA
I_{DSS}	*Drain current				
	$V_{DS} = 15V$, $V_{GS} = 0$	min.	8.0	4.0	mA
		max.	20	10	mA
$-V_{GS}$	Gate-source voltage				
	$I_D = 400\mu A$, $V_{DS} = 15V$	min	2.0	-	V
		max.	7.5	-	V
	$I_D = 50\mu A$, $V_{DS} = 15V$	min.	-	1.25	V
		max.	-	4.0	V

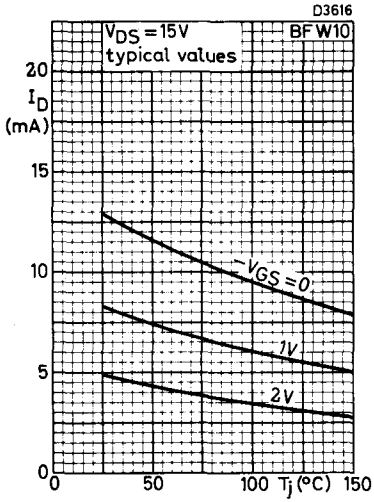
*Measured under pulsed conditions.

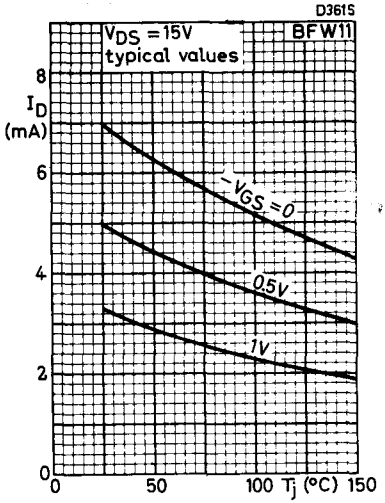
ELECTRICAL CHARACTERISTICS (contd.)

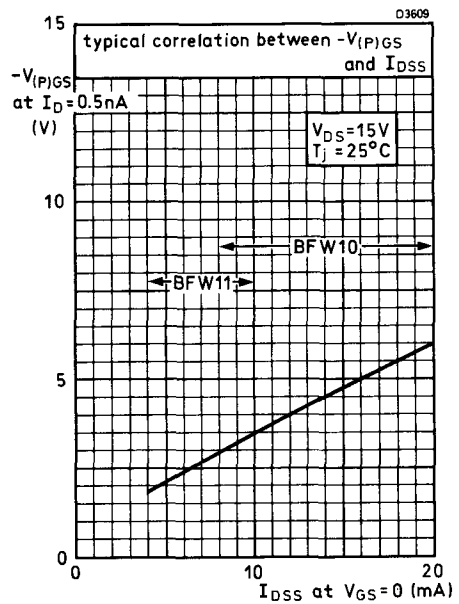
			BFW10	BFW11	
$-V_{(P)GS}$	Gate-source cut-off voltage $I_D = 0.5nA$, $V_{DS} = 15V$	max.	8.0	6.0	V
y-parameters $V_{DS} = 15V$, $V_{GS} = 0$, $T_{amb} = 25^oC$					
f = 1.0kHz					
$\lvert y_{fs} \rvert$	Transfer admittance	min.	3.5	3.0	mA/V
		max.	6.5	6.5	mA/V
$\lvert y_{os} \rvert$	Output admittance	max.	85	50	μA/V
f = 1.0MHz					
C_{is}	Input capacitance	typ.	4.0	4.0	pF
		max.	5.0	5.0	pF
$-C_{rs}$	Feedback capacitance	typ.	0.6	0.6	pF
		max.	0.80	0.80	pF
f = 200MHz					
$\lvert y_{fs} \rvert$	Transfer admittance	min.	3.2	3.2	mA/V
g_{is}	Input conductance	max.	800	800	μA/V
g_{os}	Output conductance	max.	200	100	μA/V
N	Noise figure, $T_{amb} = 25^oC$ $f = 100MHz$, $R_G = 1k\Omega$ $V_{DS} = 15V$, $V_{GS} = 0$, (input tuned to minimum noise)	max.	2.5	2.5	dB
$V_n/\sqrt{B}$	Equivalent noise voltage $V_{DS} = 15V$, $V_{GS} = 0$, $f = 10Hz$, $T_{amb} = 25^oC$	max.	75	75	$nV/\sqrt{Hz}$

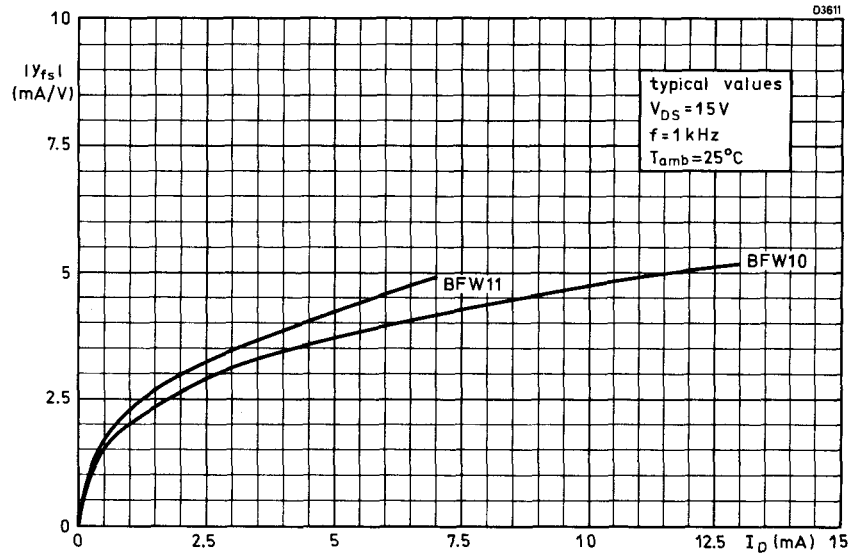

D3618
BFW10
V_{DS} = 15V
T_j = 25°C
I_D (mA)
typical values
20
15
10
5
$-V_{GS}$=0
1V
2V
3V
max
typ
min
8 $-V_{GS}$(V) 6
4
2
0
10 V_{DS}(V) 20

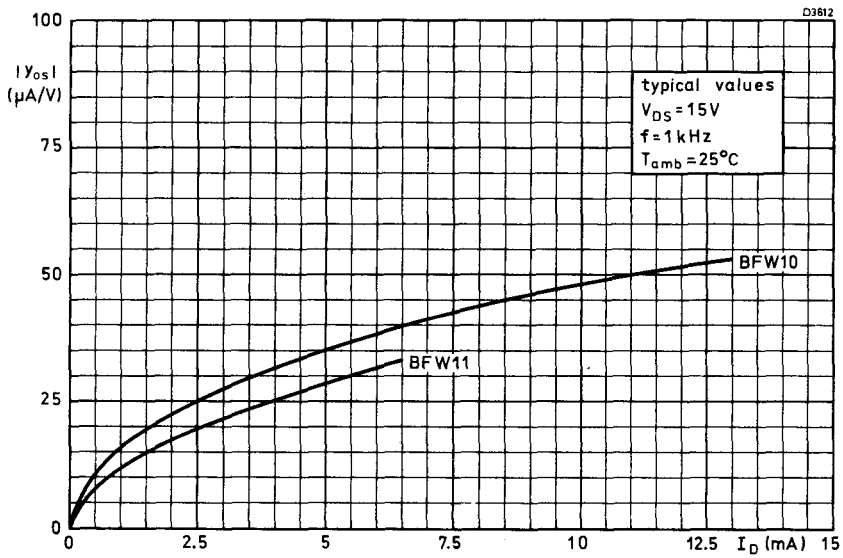

D3617
BFW11
V_{DS} = 15V
T_j = 25°C
I_D (mA)
typical values
15
10
5
$-V_{GS}$=0
0.5V
1V
1.5V
2V
max
typ
min
4 $-V_{GS}$(V) 2
0
10 V_{DS}(V) 20

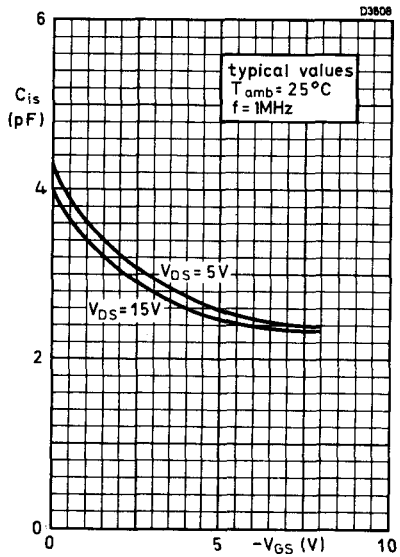

D3616
V_{DS} = 15V
typical values
BFW10
I_D (mA)
20
15
10
5
0
$-V_{GS}$ = 0
1V
2V
0
50
100
T_j (°C)
150

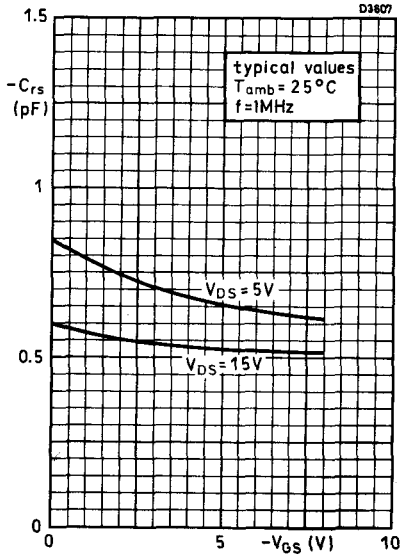

D3615
V_{DS} = 15V
typical values
BFW11
I_D (mA)
8
6
4
2
0
$-V_{GS}$ = 0
0.5V
1V
0
50
100
T_j (°C)
150

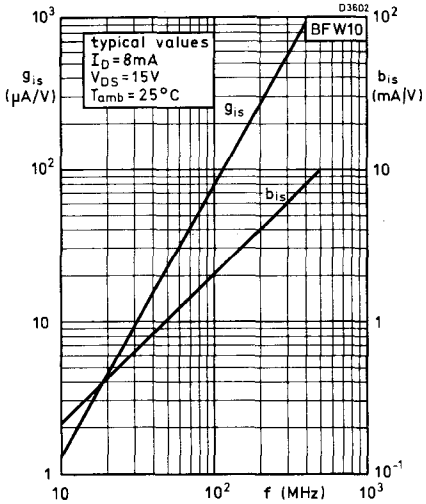

D3609
typical correlation between $-V_{(P)GS}$ and I_{DSS}
$-V_{(P)GS}$ at I_D = 0.5nA (V)
V_{DS} = 15V
T_j = 25°C
BFW10
BFW11
15
10
5
0
0
10
20
I_{DSS} at V_{GS} = 0 (mA)

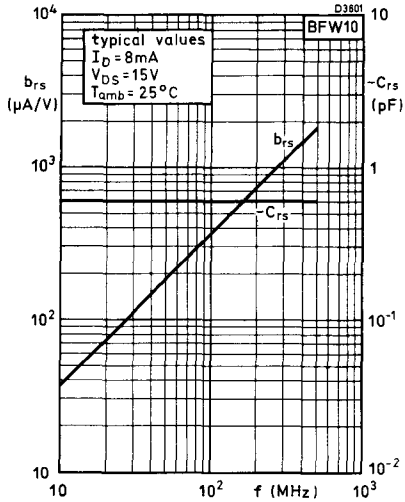

D3611
10
$|y_{fs}|$ (mA/V)
7.5
5
2.5
0
typical values
V_{DS} = 15 V
f = 1 kHz
T_{amb} = 25 °C
BFW11
BFW10
0
2.5
5
7.5
10
12.5
I_D (mA)
15

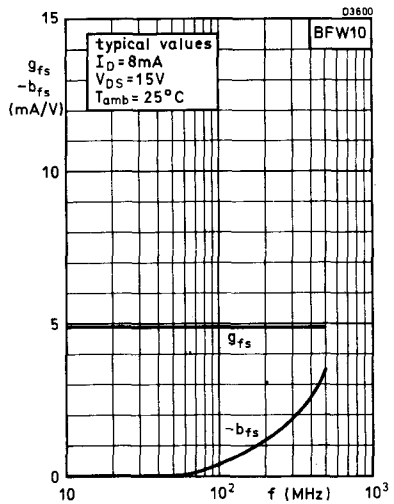

D3612
100
$|y_{os}|$ (μA/V)
75
50
25
0
typical values
V_{DS} = 15 V
f = 1 kHz
T_{amb} = 25 °C
BFW10
BFW11
0
2.5
5
7.5
10
12.5
I_D (mA)
15

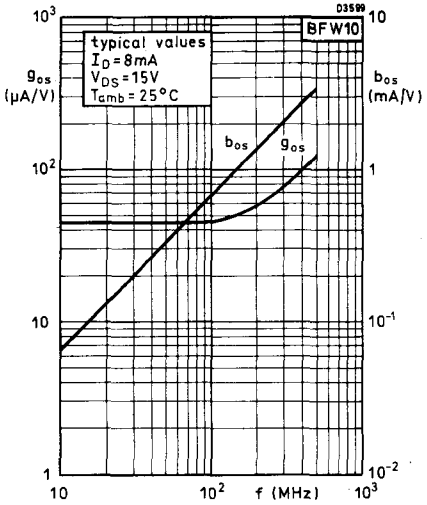

D3608
typical values
T_{amb} = 25°C
f = 1MHz
C_{is} (pF)
6
4
2
0
V_{DS} = 5V
V_{DS} = 15V
0
5
$-V_{GS}$ (V)
10

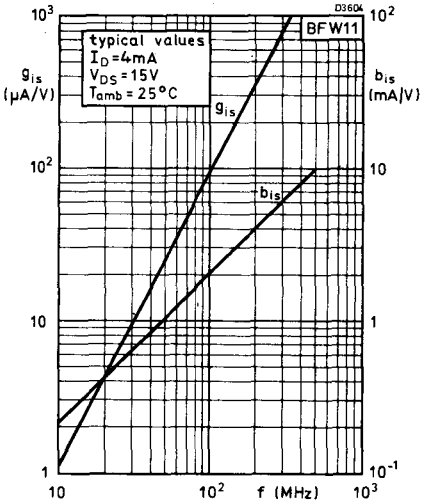

D3607
typical values
T_{amb} = 25°C
f = 1MHz
$-C_{rs}$ (pF)
1.5
1
0.5
0
V_{DS} = 5V
V_{DS} = 15V
0
5
$-V_{GS}$ (V)
10

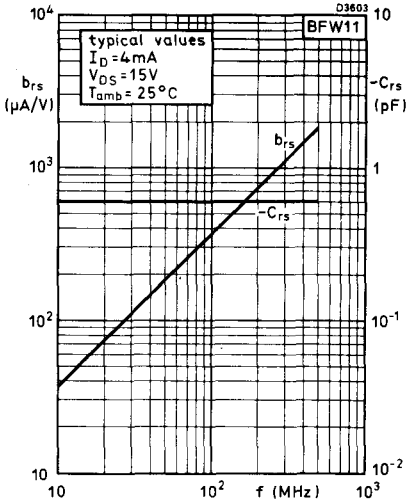

D3602
BFW10
typical values
I_D = 8mA
V_{DS} = 15V
T_{amb} = 25°C
g_{is} (μA/V)
b_{is} (mA/V)
g_{is}
$-b_{is}$
f (MHz)

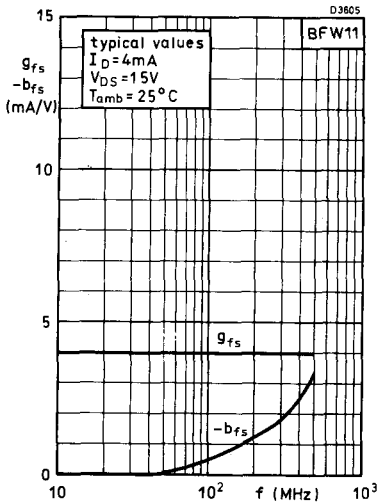

D3601
BFW10
typical values
I_D = 8mA
V_{DS} = 15V
T_{amb} = 25°C
b_{rs} (μA/V)
$-C_{rs}$ (pF)
b_{rs}
$-C_{rs}$
f (MHz)

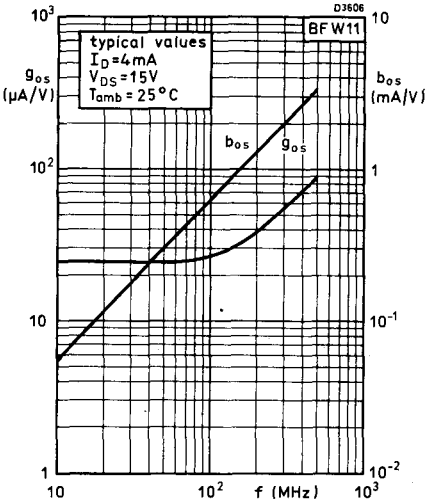

D3600
BFW10
typical values
I_D = 8mA
V_{DS} = 15V
T_{amb} = 25°C
g_{fs} $-b_{fs}$ (mA/V)
g_{fs}
$-b_{fs}$
f (MHz)

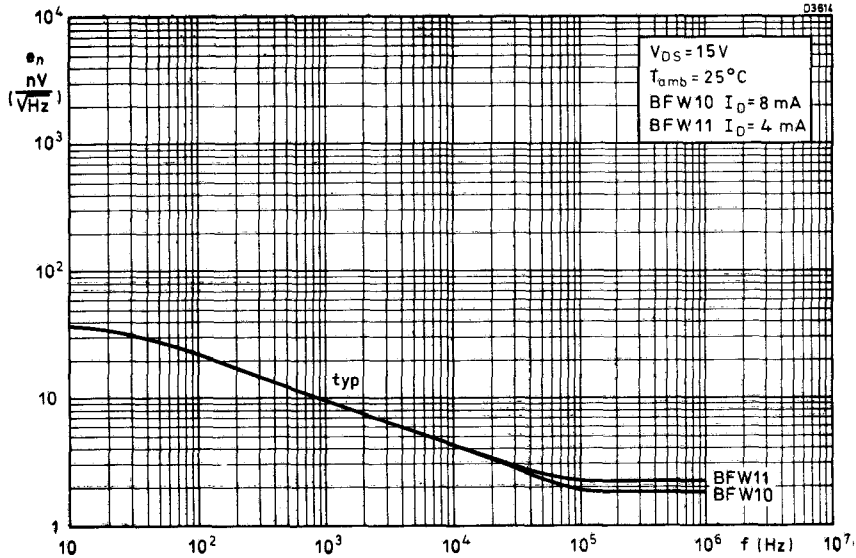

D3599
BFW10
typical values
I_D = 8mA
V_{DS} = 15V
T_{amb} = 25°C
g_{os} (μA/V)
b_{os} (mA/V)
b_{os}
g_{os}
f (MHz)

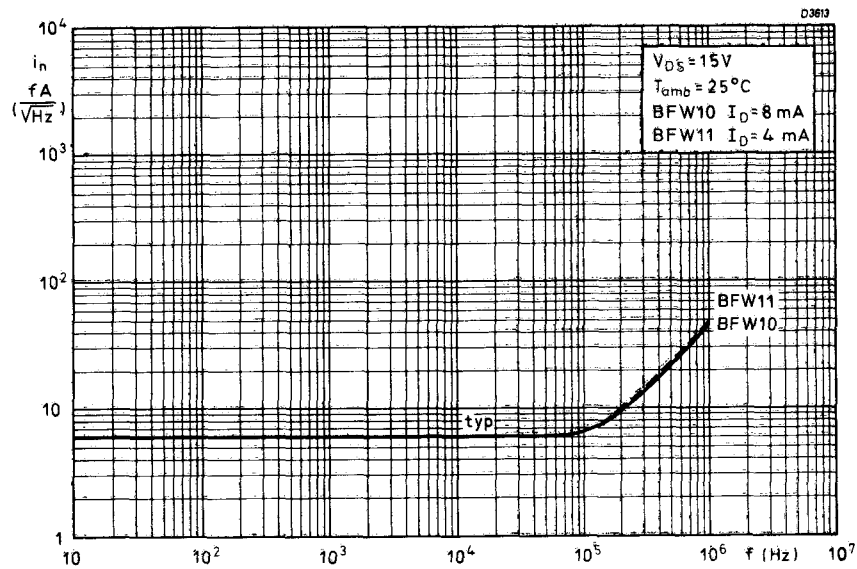

D3604
BFW11
typical values
I_D = 4mA
V_{DS} = 15V
T_{amb} = 25°C
g_{is} (μA/V)
b_{is} (mA/V)
g_{is}
b_{is}
10^3
10^2
10
1
10^2
10
1
10^{-1}
10
10^2
f (MHz)
10^3

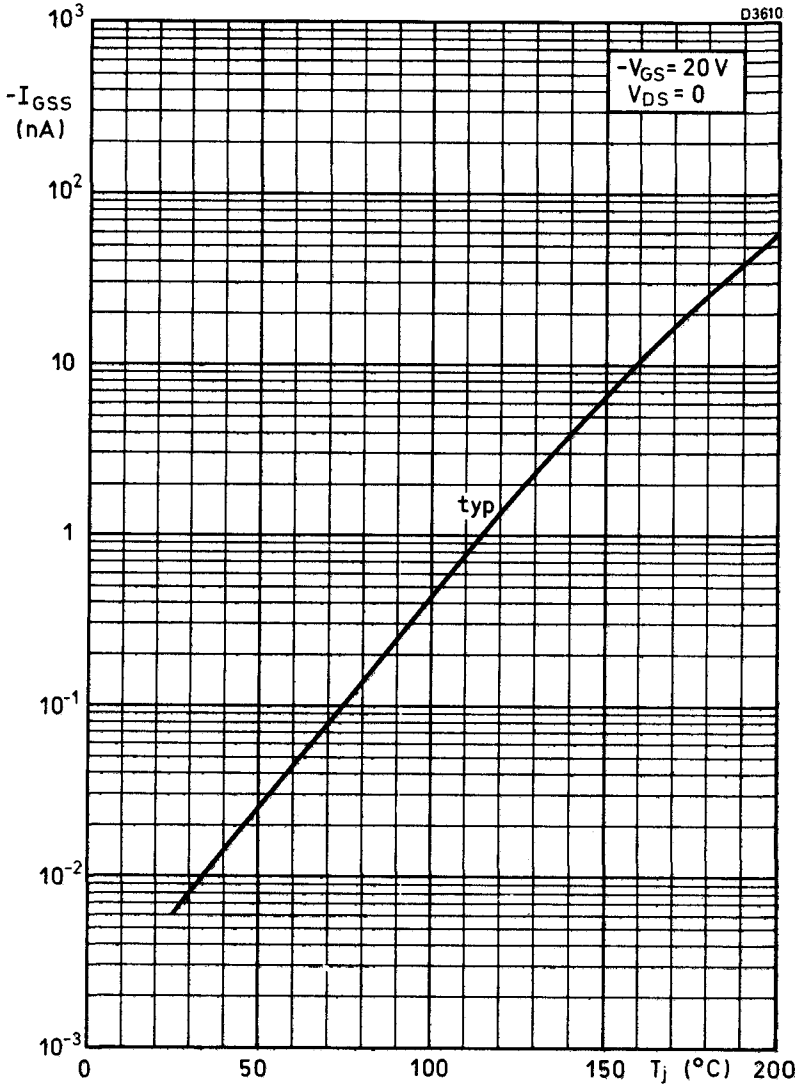

D3603
BFW11
typical values
I_D = 4mA
V_{DS} = 15V
T_{amb} = 25°C
b_{rs} (μA/V)
$-C_{rs}$ (pF)
b_{rs}
$-C_{rs}$
10^4
10^3
10^2
10
10
1
10^{-1}
10^{-2}
10
10^2
f (MHz)
10^3


D3605
BFW11
typical values
I_D = 4mA
V_{DS} = 15V
T_{amb} = 25°C
g_{fs}
$-b_{fs}$ (mA/V)
g_{fs}
$-b_{fs}$
15
10
5
0
10
10^2
f (MHz)
10^3


D3606
BFW11
typical values
I_D = 4mA
V_{DS} = 15V
T_{amb} = 25°C
g_{os} (μA/V)
b_{os} (mA/V)
b_{os}
g_{os}
10^3
10^2
10
1
10
10^{-1}
10^{-2}
10
10^2
f (MHz)
10^3


D3614
10^4
e_n
nV
$(\frac{}{\sqrt{Hz}})$
10^3
10^2
10
1
V_{DS} = 15 V
T_{amb} = 25 °C
BFW10 I_D = 8 mA
BFW11 I_D = 4 mA
typ
BFW11
BFW10
10
10^2
10^3
10^4
10^5
10^6
f (Hz)
10^7


D3613
10^4
i_n
fA
$(\frac{}{\sqrt{Hz}})$
10^3
10^2
10
1
V_{DS} = 15 V
T_{amb} = 25 °C
BFW10 I_D = 8 mA
BFW11 I_D = 4 mA
BFW11
BFW10
typ
10
10^2
10^3
10^4
10^5
10^6
f (Hz)
10^7


D3610
$-V_{GS}$ = 20 V
V_{DS} = 0
typ
$-I_{GSS}$ (nA)
10^3
10^2
10
1
10^{-1}
10^{-2}
10^{-3}
0
50
100
150
T_j (°C)
200

N-P-N SILICON PLANAR EPITAXIAL U.H.F. TRANSISTOR

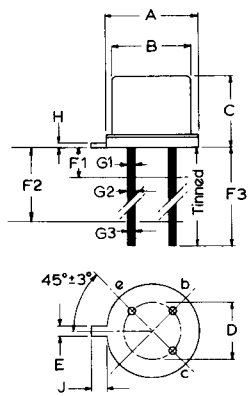
BFW16A

N-P-N silicon planar epitaxial, multi-emitter transistor with extremely good intermodulation properties and a high power gain. The BFW16A is primarily intended for the final and driver stages of channel and band aerial amplifiers with high output power in bands I to V (40-860MHz), and for the final stage of wideband vertical deflection amplifiers in high speed oscilloscopes. Encapsulated in a metal TO-39 envelope with the collector connected to case. The BFW16A is a ruggedized version of BFW16, which it succeeds.

QUICK REFERENCE DATA		
V_{CBOM} max.	40	V
V_{CEO} max.	25	V
I_{CM} max. (f > 1.0MHz)	300	mA
P_{tot} max. ($T_{case} \leq 125^{o}C$)	1.5	W
T_j max.	200	^{o}C
f_T typ. (I_C = 150mA, V_{CE} = 15V, f = 500MHz)	1.2	GHz
$-C_{re}$ typ. (I_C = 10mA, V_{CE} = 15V, f = 1.0MHz)	1.7	pF
G_p typ. (I_C = 70mA, V_{CE} = 18V) f = 200MHz	16	dB
f = 800MHz	6.5	dB
P_o typ. (I_C = 70mA, V_{CE} = 18V) f = 200MHz	150	mW
f = 800MHz	90	mW

OUTLINE AND DIMENSIONS

Conforms to B.S. 3934 SO-3/SB3-3B
J.E.D.E.C. TO-39



	Millimetres		
	Min.	Typ.	Max.
A	9.10	-	9.40
B	8.2	-	8.5
C	6.15	-	6.60
D	-	5.08	-
E	0.71	-	0.86
F1	-	-	0.51
F2	12.7	-	-
F3	12.7	-	15
G1	-	-	1.01
G2	0.41	-	0.48
G3	-	-	0.53
H	-	0.4	-
J	0.74	-	1.01

Collector connected to case
Accessories available:- 56218, 56245, 56265

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{CBOM} max. (peak)	40	V
V_{CERM} max. (peak, $R_{BE} \leq 50\Omega$, $I_C = 10mA$)	40	V
V_{CEO} max. ($I_C = 10mA$)	25	V
V_{EBO} max.	2.0	V
I_C max.	150	mA
I_{CM} max. (f > 1.0MHz)	300	mA
P_{tot} max. ($T_{case} \leq 125^oC$)	1.5	W

Temperature

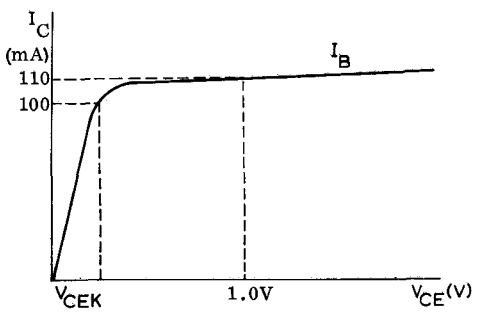
T_{stg} min.	-65	^oC
T_{stg} max.	200	^oC
T_j max.	200	^oC

THERMAL CHARACTERISTICS

$R_{th(j\text{-}amb)}$	in free air	250	degC/W
$R_{th(j\text{-}case)}$		50	degC/W
$R_{th(case\text{-}h)}$	when mounted with a top clamping washer of accessory 56218 and a boron nitride washer for electrical insulation	1.2	degC/W

ELECTRICAL CHARACTERISTICS ($T_j = 25^oC$ unless otherwise stated)

		Min.	Typ.	Max.	
I_{CBO}	Collector cut-off current $V_{CB} = 20V$, $I_E = 0$, $T_j = 150^oC$	-	-	20	μA
V_{CEK}	Collector-emitter knee voltage $I_C = 100mA$, I_B = the value for which $I_C = 110mA$, at $V_{CE} = 1.0V$	-	-	0.75	V



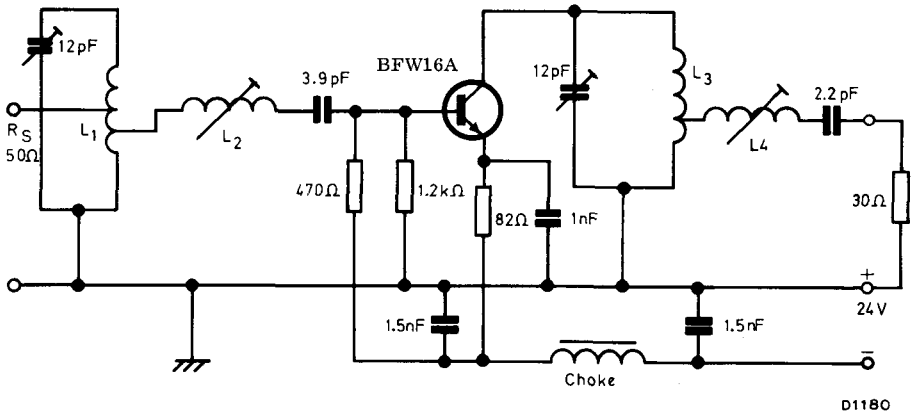
ELECTRICAL CHARACTERISTICS (contd.)

		Min.	Typ.	Max.	
h_{FE}	Static forward current transfer ratio				
	I_C = 50mA, V_{CE} = 5.0V	25	-	-	
	I_C = 150mA, V_{CE} = 5.0V	25	-	-	
f_T	Transition frequency				
	I_C = 150mA, V_{CE} = 15V, f = 500MHz	-	1.2	-	GHz
C_{Tc}	Collector capacitance				
	V_{CB} = 15V, I_E = I_e = 0, f = 1.0MHz	-	-	4.0	pF
$-C_{re}$	Feedback capacitance				
	I_C = 10mA, V_{CE} = 15V, f = 1.0MHz, T_{amb} = 25°C	-	1.7	-	pF
N	Noise figure				
	I_C = 30mA, V_{CE} = 15V, f = 200MHz, R_s = 75Ω, T_{amb} = 25°C	-	-	6.0	dB
G_p	Power gain (not neutralised)				
	I_C = 70mA, V_{CE} = 18V, T_{amb} = 25°C f = 200MHz	-	16	-	dB
	f = 800MHz	-	6.5	-	dB

Intermodulation characteristics

P_o	Output power (see test circuits)				
	I_C = 70mA, V_{CE} = 18V, v.s.w.r. at output < 2, intermodulation factor = -30dB, T_{amb} = 25°C				
	f = 200MHz, f_p = 202MHz, f_q = 205MHz, $f_{(2q-p)}$ = 208MHz (channel 9)	130	150	-	mW
	f = 800MHz, f_p = 798MHz, f_q = 802MHz, $f_{(2q-p)}$ = 806MHz (channel 62)	70	90	-	mW

POWER OUTPUT TEST CIRCUIT (f=200MHz)



L_1 = 3 turns of 1.4mm silver plated copper wire, winding pitch 2.7mm, int. dia. 8mm, taps 1.5 and 0.5 turns from earth.

L_2 = 5.5 turns of 1.4mm silver plated copper wire, winding pitch 2.2mm, int. dia. 8mm.

L_3 = 3 turns of 1.4mm silver plated copper wire, winding pitch 3.3mm, int. dia. 8mm.

L_4 = 5.5 turns of 1.4mm silver plated copper wire, winding pitch 2.2mm, int. dia. 11mm.

ADJUSTMENT OF TEST CIRCUIT

Basis of adjustment

Intermodulation distortion at d_{im} = -30dB is caused by clipping in h.f. output current and voltage.
The maximum undistorted output power is attained when

a) Clipping in current and voltage is simultaneous; this occurs if

$$R_{load} = (V_{CE} - V_{cek})/I_C$$

Where V_{cek} is the high frequency knee voltage

b) The h.f. collector current is as low as possible; this occurs if

$$-C_{load} = +C_{oe}$$

Where C_{oe} is the output capacitance of the transistor with short-circuited input.

Experimentally obtained values of R_{load} and C_{load}, for maximum output power at an intermodulation factor of -30dB, are:

$$R_{load} = 220\Omega,\ C_{load} = -5.6pF$$

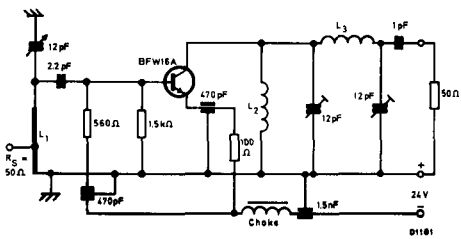
In this case 4pF are provided by C_{oe} of the transistor itself and 1.6pF by the mounting system, with the boron nitride washer between the transistor and the chassis.

ADJUSTMENT OF TEST CIRCUIT (contd.)

Procedure

1. Remove the transistor and connect a dummy, consisting of a 220Ω resistor in parallel with a 5.6pF capacitor, between the collector and the emitter connections of the output circuit.
2. Tune and match the output circuit for zero reflection at 205MHz (i.e., v.s.w.r. = 1).
3. Replace the dummy by the transistor. Tune and match the input circuit for maximum power gain and good bandpass curve. The v.s.w.r. of the output will then be ≤ 2 over most of the channel. Corrections can be made by tuning L_2.

POWER OUTPUT TEST CIRCUIT (f = 800MHz)



L_1 = 25 × 7 × 0.85mm silver plated copper strip, input tap at 5mm from earth.
L_2 = 13 turns of 0.6mm enamelled copper wire, int. dia. 8mm.
L_3 = 1.5 turns of 1.3mm copper wire, int. dia. 8mm.

ADJUSTMENT OF TEST CIRCUIT

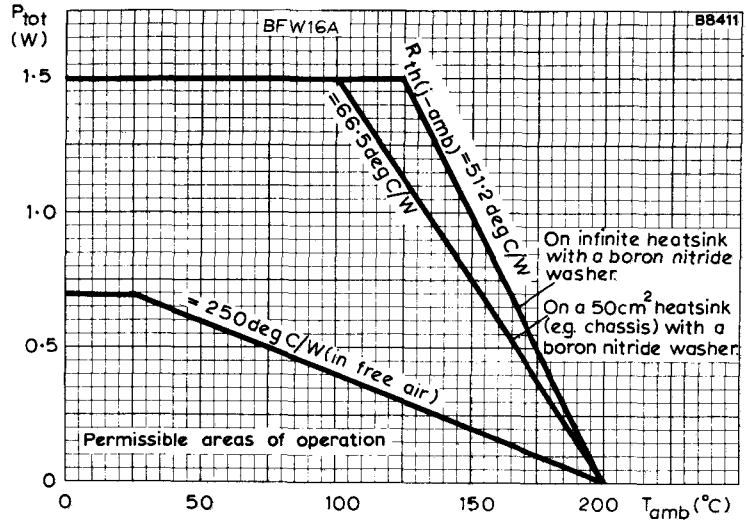
At 800MHz a dummy cannot be used to adjust for optimum collector load, because at these frequencies the impedance transformations of the dummy are too high.
A small signal with a frequency of the midchannel 802MHz is fed to the input. The signal is increased until clipping occurs, that is until the output power no longer increases linearly with increasing input signal. Care should be taken not to allow the voltage swing to exceed the V_{CER} value as this may result in the destruction of the transistor by second breakdown.
The output circuit is then tuned to eliminate clipping.

The output P_o is given by

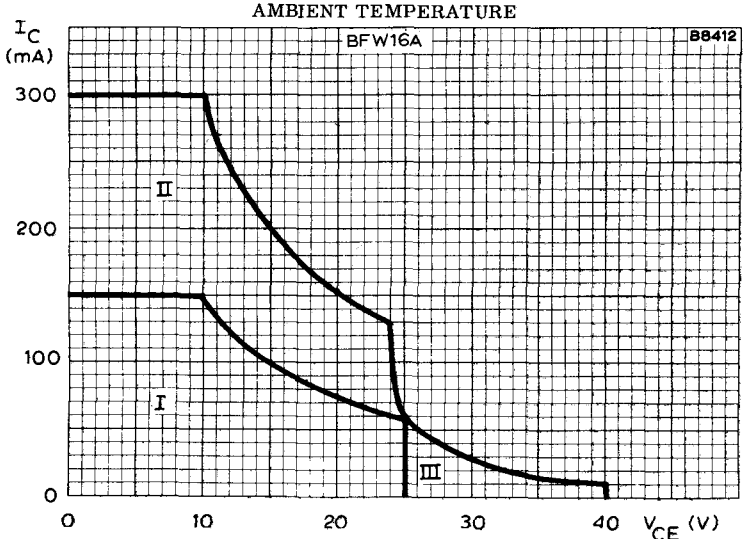
$$P_o = I_C(V_{CE} - V_{cek})/2 = 480mW$$

where V_{cek} is the high frequency knee voltage

Keeping the input signal as small as possible at P_o = 480mW, the output circuit is adjusted for minimum intermodulation. The input circuit is then adjusted for maximum gain and good bandpass curve. The v.s.w.r. is found to be ≤ 2 over the whole channel.



MAXIMUM PERMISSIBLE TOTAL DISSIPATION PLOTTED AGAINST AMBIENT TEMPERATURE

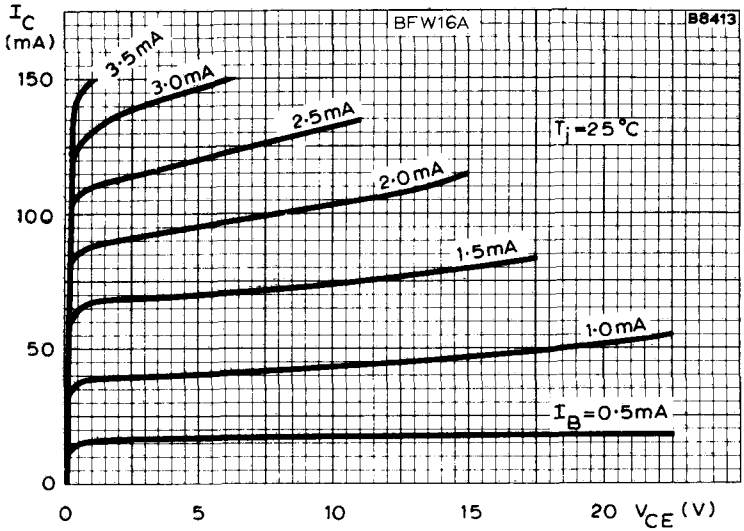


AREAS OF SAFE OPERATION

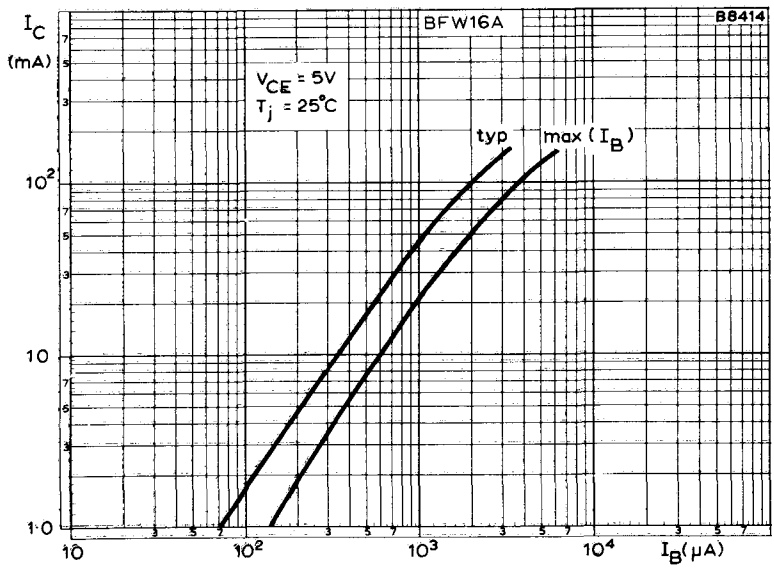
I. D.C. and A.C. operation is allowed under all base-emitter conditions, provided no limiting values are exceeded.

II. Operation is allowed under all base-emitter conditions at $f \geq 1MHz$, provided no limiting values are exceeded.

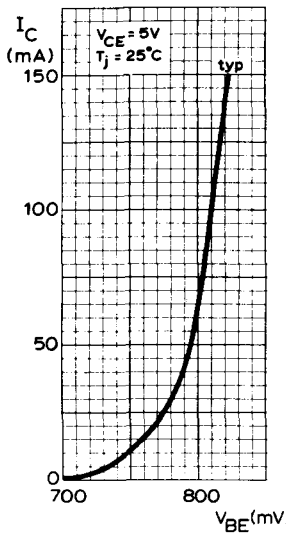
III. Operation is allowed under pulse conditions, provided the transistor is cut-off, $R_{BE} \leq 50\Omega$, and $f \geq 1MHz$.



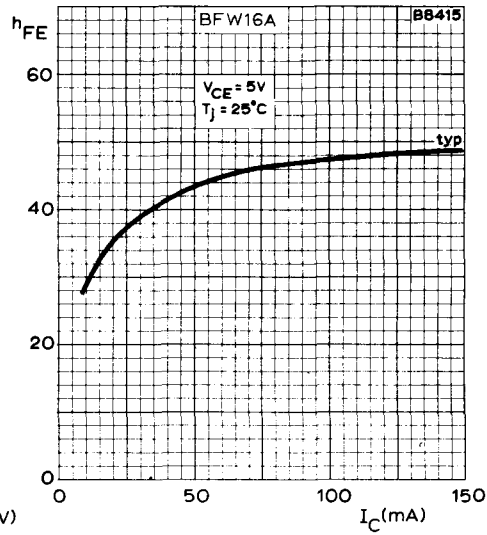
TYPICAL OUTPUT CHARACTERISTICS



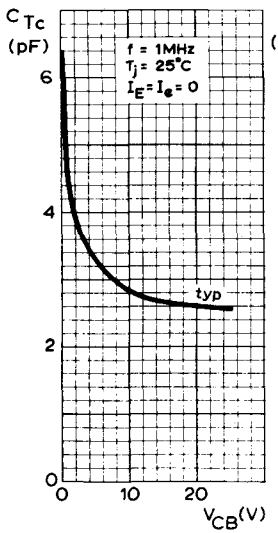
TRANSFER CHARACTERISTICS



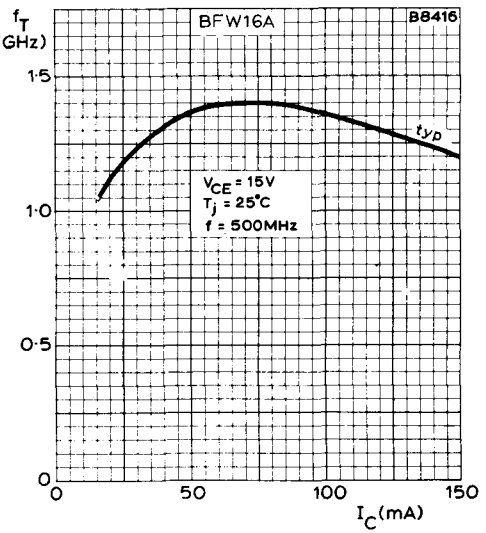
Typical mutual characteristics



Typical static forward current transfer ratio versus collector current



Typical collector capacitance versus collector-base voltage



Typical transition frequency versus collector current

APPLICATION INFORMATION

Performance of channel and band amplifiers

Frequency range	channel 4 61-68	channel 9 202-209	channel 55 742-750	band I 47-68	band II 87.5-108	band III 174-230	MHz
Transistor used in:							
final stage	BFW16A	BFW16A	BFW16A	BFW16A	BFW16A	BFW16A	
driver stage		BFW16A	BFW16A			BFW16A	
second stage			BFY90				
first stage	BFY90	BFY90	BFY90	BFY90	BFY90	BFY90	
Output power at:							
d_{im} = -30dB	150*	150*	100				mW
d_{im} = -50dB					30		mW
d_{im} = -60dB				10		10	mW
Power gain	50	44	26.5	51	43	39	dB
Noise figure	7	6	8	6.0-6.5	6.5	6.5	dB
V.S.W.R. over the whole channel or band							
for the input	< 2	< 2	< 2	< 2	< 2	< 2	
for the output	< 2	< 2	< 2	< 2	< 2	< 2	
Load impedance	30	30	50	30	30	30	Ω
Source impedance	60	60	50	60	60	60	Ω

*V_o = 2.2V over R_L = 30Ω or

V_o = 3V over R_L = 60Ω

N-P-N SILICON PLANAR EPITAXIAL V.H.F. TRANSISTOR

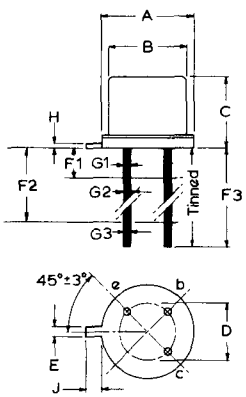
BFW17A

N-P-N silicon planar epitaxial, multi-emitter transistor with extremely good intermodulation properties and a high power gain. The BFW17A is primarily intended for the final and driver stages of channel and band aerial amplifiers with high output in bands I, II and III (40-230MHz). Encapsulated in a metal TO-39 envelope with the collector connected to the case. The BFW17A is a ruggedized version of the BFW17, which it succeeds.

QUICK REFERENCE DATA		
V_{CBOM} max.	40	V
V_{CEO} max.	25	V
I_{CM} max. (f > 1.0MHz)	300	mA
P_{tot} max. ($T_{case} \leq 125^{o}C$)	1.5	W
T_j max.	200	^{o}C
f_T typ. (I_C=150mA, V_{CE}=15V, f=500MHz)	1.1	GHz
$-C_{re}$ typ. (I_C=10mA, V_{CE}=15V, f=1.0MHz)	1.7	pF
G_p typ. (I_C=70mA, V_{CE}=18V, f=200MHz)	16	dB
P_o typ. (I_C=70mA, V_{CE}=18V, f=200MHz)	150	mW

OUTLINE AND DIMENSIONS

Conforms to B.S. 3934 SO-3/SB3-3B
J.E.D.E.C. TO-39



Collector connected to case

Accessories available:
56218, 56245, 56265

	Millimetres		
	Min.	Typ.	Max.
A	9.10	-	9.40
B	8.2	-	8.5
C	6.15	-	6.60
D	-	5.08	-
E	0.71	-	0.86
F1	-	-	0.51
F2	12.7	-	-
F3	12.7	-	15
G1	-	-	1.01
G2	0.41	-	0.48
G3	-	-	0.53
H	-	0.4	-
J	0.74	-	1.01

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{CBOM} max. (peak)	40	V
V_{CERM} max. (peak, $R_{BE} \leq 50\Omega$, $I_C = 10mA$)	40	V
V_{CEO} max. ($I_C = 10mA$)	25	V
V_{EBO} max.	2.0	V
I_C max.	150	mA
I_{CM} max. (f > 1.0MHz)	300	mA
P_{tot} max. ($T_{case} \leq 125^oC$)	1.5	W

Temperature

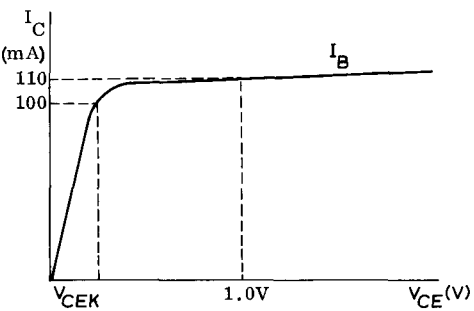
T_{stg} min.	-65	^oC
T_{stg} max.	200	^oC
T_j max.	200	^oC

THERMAL CHARACTERISTICS

$R_{th(j\text{-amb})}$	in free air	250	degC/W
$R_{th(j\text{-case})}$		50	degC/W
$R_{th(case\text{-h})}$	when mounted with a top clamping washer of accessory 56218 and a boron nitride washer for electrical insulation	1.2	degC/W

ELECTRICAL CHARACTERISTICS ($T_j = 25^oC$ unless otherwise stated)

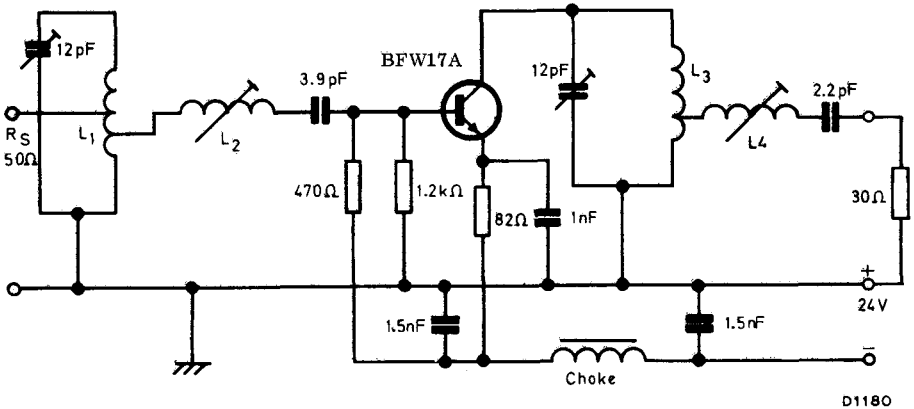
		Min.	Typ.	Max.	
I_{CBO}	*Collector cut-off current* $V_{CB} = 20V$, $I_E = 0$, $T_j = 150^oC$	-	-	20	μA
V_{CEK}	Collector-emitter knee voltage $I_C = 100mA$, I_B = the value for which $I_C = 110mA$, at $V_{CE} = 1.0V$	-	-	0.75	V



ELECTRICAL CHARACTERISTICS (contd.)

		Min.	Typ.	Max.	
h_{FE}	Static forward current transfer ratio				
	I_C=50mA, V_{CE}=5.0V	25	-	-	
	I_C=150mA, V_{CE}=5.0V	25	-	-	
f_T	Transition frequency I_C=150mA, V_{CE}=15V, f=500MHz	-	1.1	-	GHz
C_{Tc}	Collector capacitance V_{CB}=15V, I_E=I_e=0, f=1.0MHz	-	-	4.0	pF
$-C_{re}$	Feedback capacitance I_C=10mA, V_{CE}=15V, f=1.0MHz, T_{amb}=25°C	-	1.7	-	pF
G_p	Power gain (not neutralised) I_C=70mA, V_{CE}=18V, f=200MHz, T_{amb}=25°C	-	16	-	dB
Intermodulation characteristics					
P_o	Output power (see test circuit) I_C=70mA, V_{CE}=18V, f=200MHz, intermodulation factor=-30dB, v.s.w.r. at output <2.0, T_{amb}=25°C f_p=202MHz, f_q=205MHz, $f_{(2q-p)}$=208MHz (channel 9)	-	150	-	mW

POWER OUTPUT TEST CIRCUIT (f = 200MHz)



L_1 = 3 turns of 1.4mm silver plated copper wire, winding pitch 2.7mm, int. dia. 8mm, taps 1.5 and 0.5 turns from earth.

L_2 = 5.5 turns of 1.4mm silver plated copper wire, winding pitch 2.2mm, int. dia. 8mm.

L_3 = 3 turns of 1.4mm silver plated copper wire, winding pitch 3.3mm, int. dia. 8mm.

L_4 = 5.5 turns of 1.4mm silver plated copper wire, winding pitch 2.2mm, int. dia. 11mm.

ADJUSTMENT OF TEST CIRCUIT

Basis of adjustment

Intermodulation distortion at d_{im} = -30dB is caused by clipping in h.f. output current and voltage.
The maximum undistorted output power is attained when

a) Clipping in current and voltage is simultaneous; this occurs if

$$R_{load} = (V_{CE} - V_{cek})/I_C$$

Where V_{cek} is the high frequency knee voltage

b) The h.f. collector current is as low as possible; this occurs if

$$-C_{load} = +C_{oe}$$

Where C_{oe} is the output capacitance of the transistor with short-circuited input.

Experimentally obtained values of R_{load} and C_{load}, for maximum output power at an intermodulation factor of -30dB, are:

$$R_{load} = 220\Omega,\ C_{load} = -5.6pF$$

In this case 4pF are provided by C_{oe} of the transistor itself and 1.6pF by the mounting system, with the boron nitride washer between the transistor and the chassis.

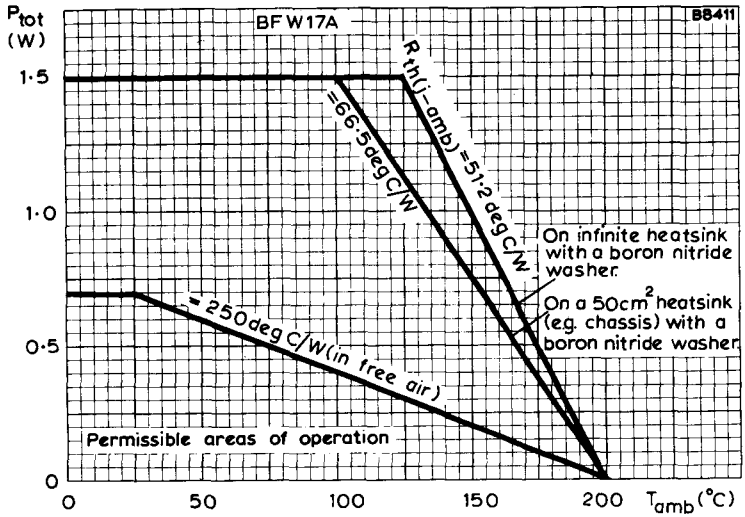
ADJUSTMENT OF TEST CIRCUIT (contd.)

Procedure

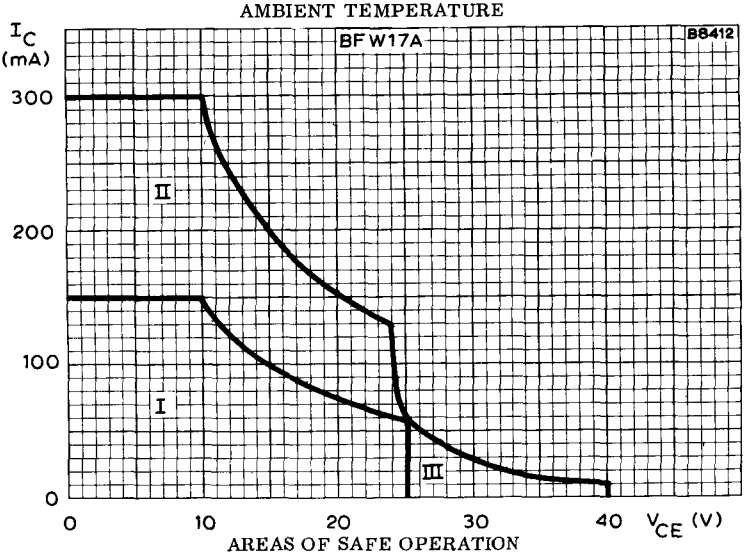
1. Remove the transistor and connect a dummy, consisting of a 220Ω resistor in parallel with a 5.6pF capacitor, between the collector and the emitter connections of the output circuit.

2. Tune and match the output circuit for zero reflection at 205MHz (i.e., v.s.w.r. = 1).

3. Replace the dummy by the transistor. Tune and match the input circuit for maximum power gain and good bandpass curve. The v.s.w.r. of the output will then be ≤ 2 over most of the channel. Corrections can be made by tuning L_2.



MAXIMUM PERMISSIBLE TOTAL DISSIPATION PLOTTED AGAINST AMBIENT TEMPERATURE

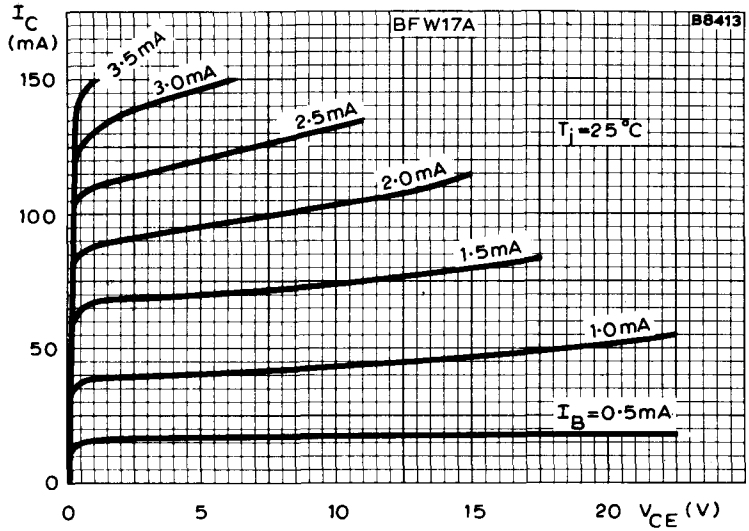


AREAS OF SAFE OPERATION

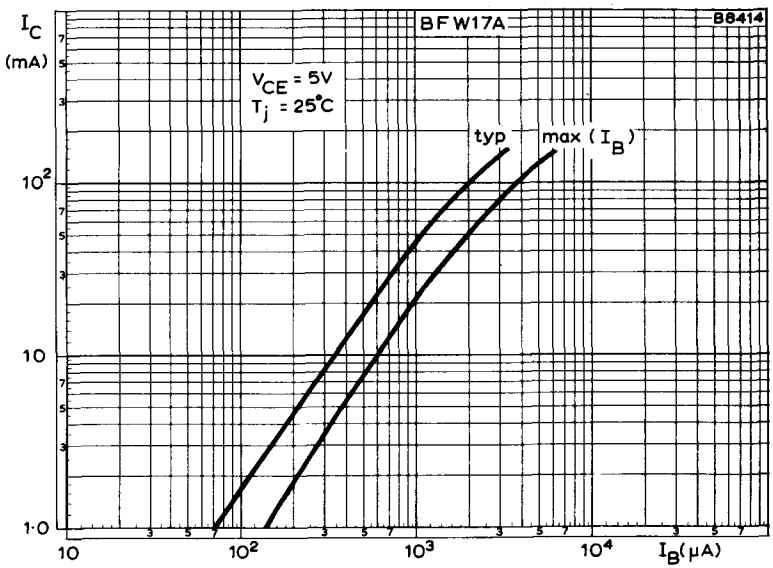
I. D.C. and A.C. operation is allowed under all base-emitter conditions, provided no limiting values are exceeded.

II. Operation is allowed under all base-emitter conditions at $f \geq 1MHz$, provided no limiting values are exceeded.

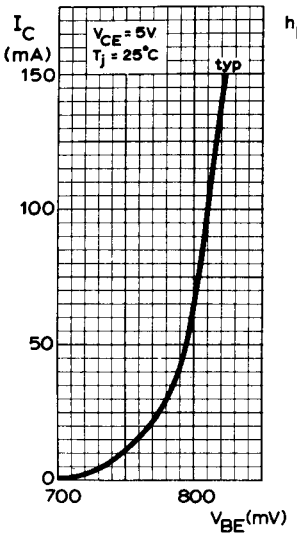
III. Operation is allowed under pulse conditions, provided the transistor is cut-off, $R_{BE} \leq 50\Omega$ and $f \geq 1MHz$.



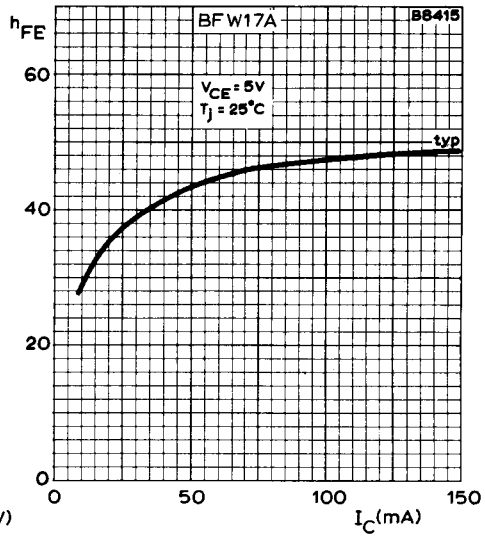
TYPICAL OUTPUT CHARACTERISTICS



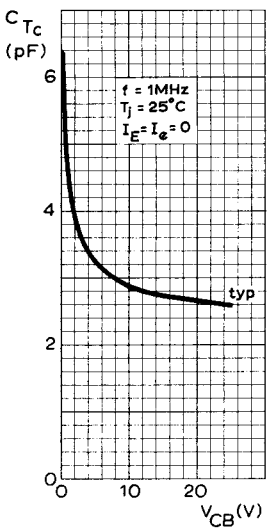
TRANSFER CHARACTERISTICS



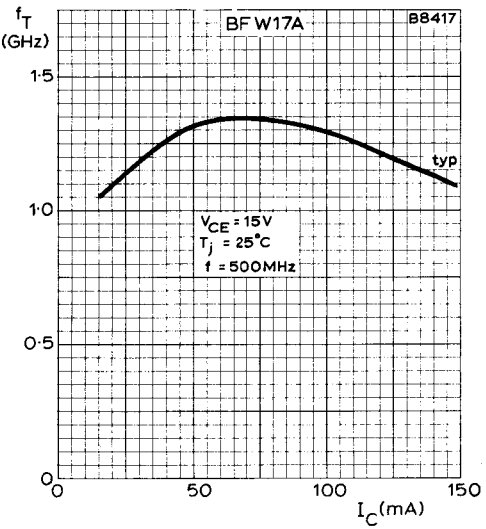
Typical mutual characteristics



Typical static forward current transfer ratio versus collector current



Typical collector capacitance versus collector-base voltage



Typical transition frequency versus collector current

N-P-N SILICON PLANAR EPITAXIAL TRANSISTOR

BFW30

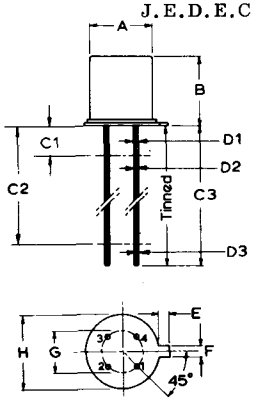
N-P-N silicon planar epitaxial, multi-emitter transistor with extremely good intermodulation properties and a high power gain. The BFW30 is primarily intended for wideband vertical amplifiers in high speed oscilloscopes, wideband aerial amplifiers (40–860MHz) and television distribution amplifiers. Encapsulated in a metal TO-72 envelope with all electrodes insulated from the case. Shield lead connected to case.

QUICK REFERENCE DATA

V_{CBOM} max.	20	V
V_{CEO} max.	10	V
I_{CM} max. (f>1.0MHz)	100	mA
P_{tot} max. ($T_{amb} \leq 25^{o}C$)	250	mW
T_j max.	200	^{o}C
f_T typ. (I_C=50mA, V_{CE}=5.0V, f=500MHz)	1.6	GHz
$-C_{re}$ typ. (I_C=2.0mA, V_{CE}=5.0V, f=1.0MHz)	0.8	pF
G_p typ. (I_C=30mA, V_{CE}=5.0V) f=200MHz	21	dB
f=800MHz	7.5	dB
d_{im} typ. (I_C=30mA, V_{CE}=6.0V, R_L=37.5Ω, f_p=183MHz, V_o=100mV f_q=200MHz, V_o=100mV $f_{(2q-p)}$=217MHz)	-60	dB

OUTLINE AND DIMENSIONS

Conforms to B.S. 3934 SO-12A/SB4-3
J.E.D.E.C. TO-72



Viewed from underside

Millimetres

	Min.	Nom.	Max.
A	4.53	-	4.8
B	4.66	-	5.33
C1	-	-	0.51
C2	12.7	-	-
C3	12.7	-	15
D1	-	-	1.01
D2	0.41	-	0.48
D3	-	-	0.53
E	0.84	-	1.17
F	0.92	-	1.16
G	-	2.54	-
H	5.31	-	5.84

Connections
1. Emitter
2. Base
3. Collector
4. Shield (connected to case)

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{CBOM} max. (peak)	20	V
V_{CERM} max. (peak, $R_{BE} \leq 50\Omega$, $I_C = 10mA$)	20	V
V_{CEO} max. ($I_C = 10mA$)	10	V
V_{EBO} max.	2.5	V
I_C max.	50	mA
I_{CM} max. ($f > 1.0MHz$)	100	mA
P_{tot} max. ($T_{amb} \leq 25^oC$)	250	mW

Temperature

T_{stg} min.	-65	^oC
T_{stg} max.	200	^oC
T_j max. operating	200	^oC

THERMAL CHARACTERISTICS

$R_{th(j-amb)}$ in free air	0.7	degC/mW
$R_{th(j-case)}$	0.5	degC/mW

ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^oC$ unless otherwise stated)

		Min.	Typ.	Max.	
I_{CBO}	Collector cut-off current $V_{CB} = 10V$, $I_E = 0$	-	-	50	nA
h_{FE}	Static forward current transfer ratio				
	$I_C = 25mA$, $V_{CE} = 5.0V$	25	-	-	
	$I_C = 50mA$, $V_{CE} = 5.0V$	25	-	-	
f_T	*Transition frequency $I_C = 50mA$, $V_{CE} = 5.0V$, $f = 500MHz$	-	1.6	-	GHz
C_{tc}	**Collector capacitance $V_{CB} = 10V$, $I_E = I_e = 0$, $f = 1.0MHz$	-	-	1.5	pF
$-C_{re}$	*Feedback capacitance $V_{CE} = 5.0V$, $I_C = 2.0mA$, $f = 1.0MHz$	-	0.8	-	pF

*Fourth lead (case) grounded
**Fourth lead (case) not connected

ELECTRICAL CHARACTERISTICS (cont'd)

		Min.	Typ.	Max.	
G_p	*Power gain (not neutralised)				
	I_C=30mA, V_{CE}=5.0V, f=200MHz	19	21	-	dB
	f=800MHz	-	7.5	-	dB
N	*Noise figure				
	V_{CE}=5.0V, I_C=2.0mA,				
	f=500MHz, R_S=50Ω	-	-	5.0	dB
d_{im}	*Intermodulation distortion (see fig.1)				
	I_C=30mA, V_{CE}=6.0V, R_L=37.5Ω,				
	f_p=183MHz, V_o=100mV				
	f_q=200MHz, V_o=100mV				
	$f_{(2q-p)}$=217MHz	-	-60	-	dB

*Fourth lead (case) grounded

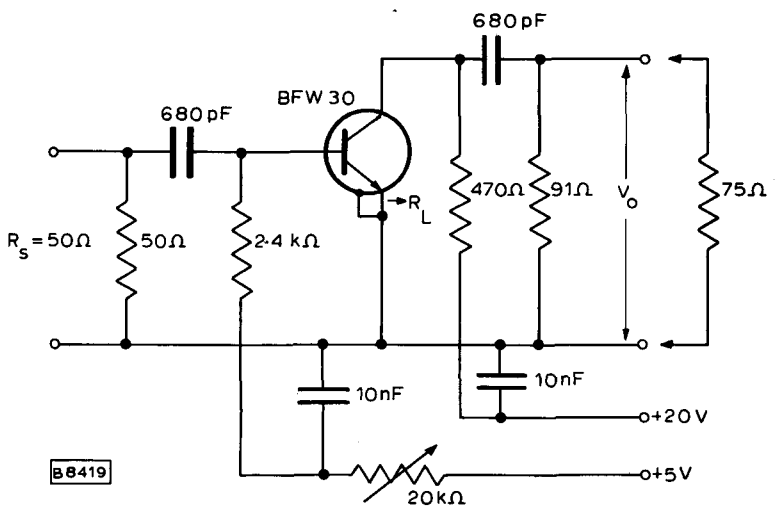
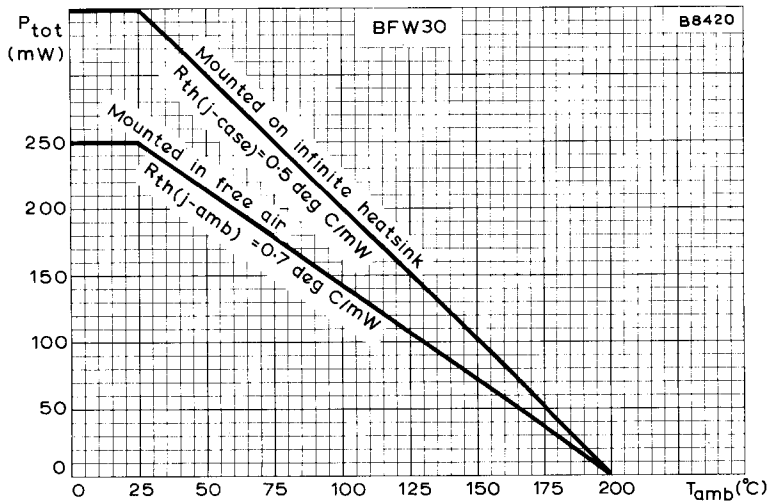
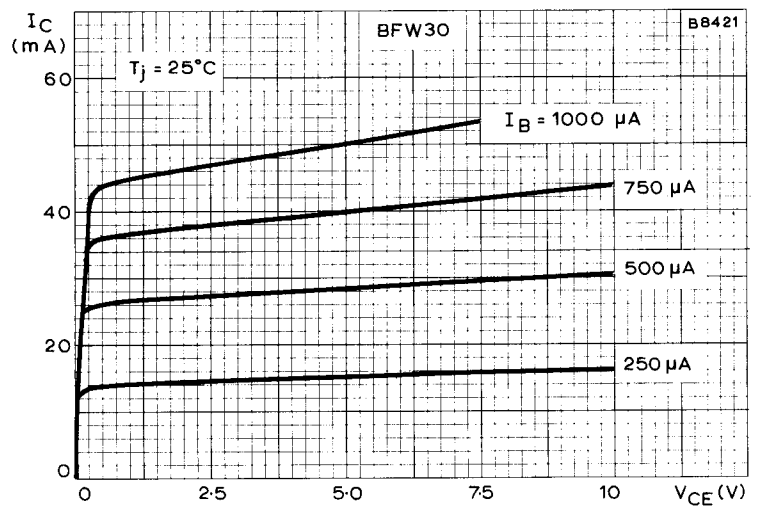


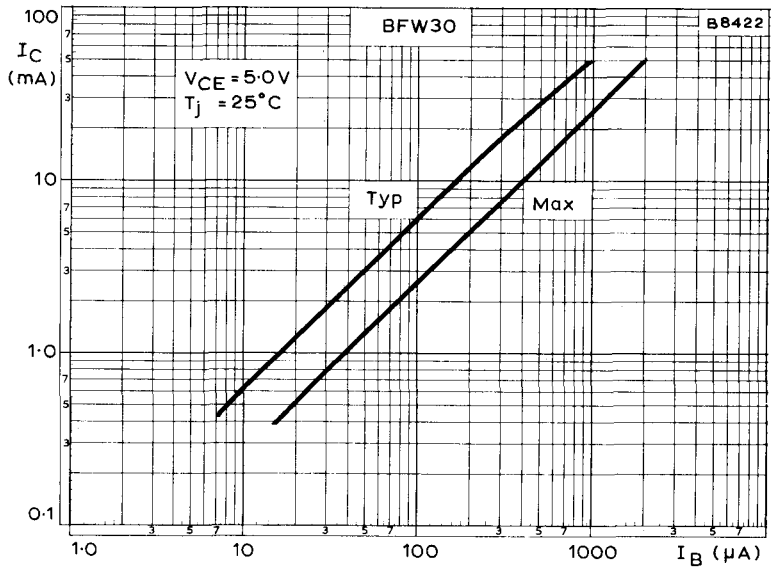
Fig.1



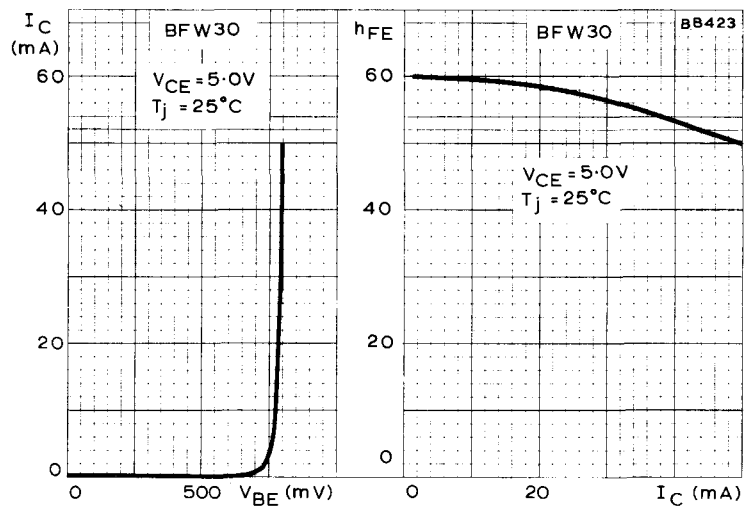
MAXIMUM PERMISSIBLE TOTAL DISSIPATION PLOTTED AGAINST AMBIENT TEMPERATURE



TYPICAL OUTPUT CHARACTERISTICS

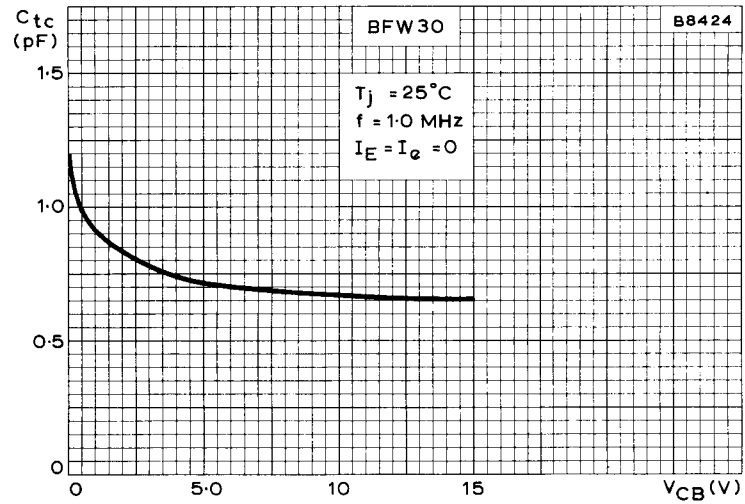


TRANSFER CHARACTERISTICS

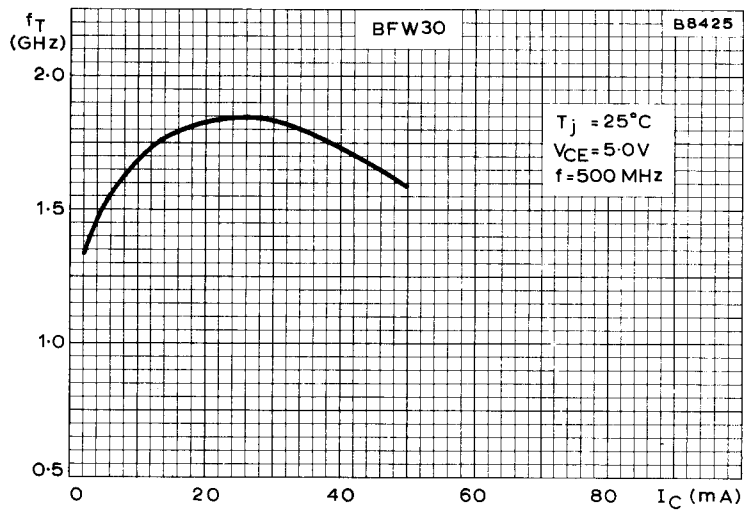


Typical mutual characteristic

Typical static forward current transfer ratio versus collector current



TYPICAL COLLECTOR CAPACITANCE PLOTTED AGAINST COLLECTOR-BASE VOLTAGE



TYPICAL TRANSITION FREQUENCY PLOTTED AGAINST COLLECTOR CURRENT

N-CHANNEL SILICON FIELD EFFECT TRANSISTOR

BFW61

The BFW61 is an n-channel silicon epitaxial planar junction field effect transistor for general purpose industrial applications.

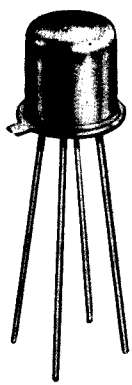
QUICK REFERENCE DATA			
V_{DSS} max.		±25	V
V_{GSO} max.		-25	V
$V_{(P)GS}$ max.		8.0	V
I_{DSS} (V_{DS}=15V, V_{GS}=0)	min.	2.0	mA
	max.	20	mA
P_{tot} max. (T_{amb}≤25°C)		300	mW
y_{fs} min.		1.6	mmho
$-C_{rs}$ max.		2.0	pF

OUTLINE AND DIMENSIONS

Conforms to J.E.D.E.C. TO-72

B.S. 3934 SO-12A/SB4-3

For details see page 4.



RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{DSS} max.	Drain-source voltage	±25	V
V_{DGO} max.	Drain-gate voltage	25	V
V_{GSO} max.	Gate-source voltage	-25	V
I_D max.	Drain current	20	mA
I_G max.	Gate current	10	mA
P_{tot} max.	Total device dissipation ($T_{amb} \leq 25^oC$)	300	mW

Temperature

T_{stg}	Storage temperature range	-65 to +200	^oC
T_j max.	Max. junction temperature	200	^oC

THERMAL CHARACTERISTIC

$R_{th(j-amb)}$	0.59	degC/mW

ELECTRICAL CHARACTERISTICS ($T_j = 25^oC$ unless otherwise stated)

		Min.	Max.	
$-I_{GSS}$	Gate cut-off current $-V_{GS} = 20V$, $V_{DS} = 0$	-	1.0	nA
	$-V_{GS} = 20V$, $V_{DS} = 0$, $T_j = 150^oC$	-	1.0	μA
I_{DSS}	*Drain current $V_{DS} = 15V$, $V_{GS} = 0$	2.0	20	mA
$-V_{GS}$	Gate-source voltage $I_D = 200\mu A$, $V_{DS} = 15V$	0.5	7.5	V
$-V_{(P)GS}$	Gate-source cut-off voltage $I_D = 1.0nA$, $V_{DS} = 15V$	-	8.0	V

*Measured under pulse conditions.

ELECTRICAL CHARACTERISTICS (cont'd)

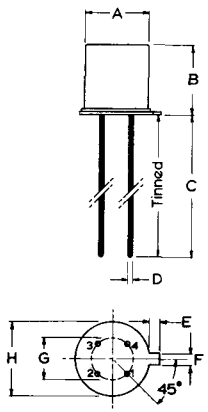
Small signal y-parameters		Min.	Max.	
Common source, V_{DS}=15V, V_{GS}=0				
y_{fs}	Forward transfer admittance f=1.0kHz	2.0	6.5	mmho
y_{os}	Output admittance f=1.0kHz	-	85	μmho
C_{is}	Input capacitance f=1.0MHz	-	6.0	pF
$-C_{rs}$	Reverse transfer capacitance f=1.0MHz	-	2.0	pF
y_{fs}	Forward transfer admittance f=10MHz	1.6	-	mmho

SOLDERING AND WIRING RECOMMENDATIONS

1. Devices may be soldered directly into a circuit with a soldering iron at a maximum iron temperature of 245°C for a time of up to 10 seconds at least 1.5mm from the seal. At an iron temperature of 245°C to 400°C the maximum soldering time is 5 seconds at least 5mm from the seal.
2. These devices may be dip-soldered at a solder temperature of 245°C for a maximum soldering time of 5 seconds. The case temperature during dip-soldering must not at any time exceed the maximum storage temperature. These recommendations apply to a device mounted flush on a board having punched-through holes, or spaced at least 1.5mm above a board having plated-through holes.
3. Care should be taken not to bend the leads nearer than 1.5mm from the seal.
4. If devices are stored at temperatures above 100°C before incorporation into equipment, some deterioration of the external surface is likely to occur which may make soldering into the circuit difficult. Under these circumstances the leads should be retinned using a suitable activated flux.

OUTLINE, DIMENSIONS AND CONNECTIONS

Conforms to J.E.D.E.C. TO-72



	Millimetres		
	Min.	Nom.	Max.
A	-	-	4.8
B	-	-	5.3
C	12.7	-	-
D	-	0.43	-
E	-	1.0	-
F	-	1.05	-
G	-	2.54	-
H	5.3	5.55	5.8

Pinning

1. Source
2. Drain
3. Gate
4. Shield lead connected to case

P-N-P SILICON PLANAR EPITAXIAL TRANSISTORS

BFX29 BFX87 BFX88

BFX29 is also available to BS9365—F010

P-N-P silicon planar epitaxial transistors for general purpose industrial applications. Encapsulated in TO-5 envelope with the collector connected to can.

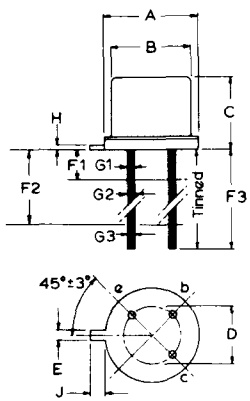
QUICK REFERENCE DATA

		BFX29	BFX87	BFX88	
$-V_{CBO}$ max.		60	50	40	V
$-V_{CEO}$ max.		60	50	40	V
$-I_{CM}$ max.					600 mA
P_{tot} max. ($T_{amb} \leq 25^{o}C$)					600 mW
h_{FE} ($-I_C = 10mA$, $-V_{CE} = 10V$)					
	min.	50	40	40	
	typ.	125	125	125	
f_T min. ($-I_C = 50mA$, $-V_{CE} = 10V$, $f = 100MHz$)					100 MHz

Unless otherwise stated, data is applicable to all types

OUTLINE AND DIMENSIONS

Conforms to B.S. 3934 SO-3/SB3-3A
J.E.D.E.C. TO-5



The collector is electrically connected to the envelope

	Millimetres		
	Min.	Nom.	Max.
A	9.10	-	9.40
B	8.20	-	8.50
C	6.10	-	6.60
D	-	5.08	-
E	0.71	-	0.86
F1	-	-	0.51
F2	12.7	-	-
F3	38.1	-	41.3
G1	-	-	1.01
G2	0.41	-	0.48
G3	-	-	0.53
H	-	0.4	-
J	0.74	-	1.0

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

	BFX29	BFX87	BFX88	
$-V_{CBO}$ max.	60	50	40	V
$-V_{CEO}$ max.	60	50	40	V
$-V_{EBO}$ max.	5.0	4.0	4.0	V
$-I_C$ max.			600	mA
$-I_{CM}$ max.			600	mA
I_{EM} max.			600	mA
P_{tot} max. ($T_{amb} \leq 25^oC$)			600	mW

Temperature

T_{stg} range	-65 to +200	^oC
T_j max.	+200	^oC

THERMAL CHARACTERISTIC

$R_{th(j-amb)}$	292	degC/W

ELECTRICAL CHARACTERISTICS ($T_j = 25^oC$ unless otherwise stated)

			Min.	Typ.	Max.	
$-I_{CBO}$	Collector cut-off current					
	$-V_{CB} = 60V$, $I_E = 0$	BFX29	-	1.0	500	nA
	$-V_{CB} = 50V$, $I_E = 0$	BFX87	-	1.0	500	nA
	$-V_{CB} = 40V$, $I_E = 0$	BFX88	-	1.0	500	nA
	$-V_{CB} = 50V$, $I_E = 0$	BFX29	-	0.5	50	nA
	$-V_{CB} = 40V$, $I_E = 0$	BFX87	-	0.5	50	nA
	$-V_{CB} = 30V$, $I_E = 0$	BFX88	-	0.5	50	nA
	$-V_{CB} = 50V$, $I_E = 0$, $T_j = 100^oC$	BFX29	-	0.03	2.0	μA
	$-V_{CB} = 40V$, $I_E = 0$, $T_j = 100^oC$	BFX87	-	0.03	2.0	μA
	$-V_{CB} = 30V$, $I_E = 0$, $T_j = 100^oC$	BFX88	-	0.03	2.0	μA
$-I_{EBO}$	Emitter cut-off current					
	$-V_{EB} = 5.0V$, $I_C = 0$	BFX29	-	30	500	nA
	$-V_{EB} = 4.0V$, $I_C = 0$	BFX87,88	-	2.0	500	nA
	$-V_{EB} = 3.0V$, $I_C = 0$	BFX29,87, BFX88	-	1.0	100	nA

ELECTRICAL CHARACTERISTICS (cont'd)

			Min.	Typ.	Max.	
h_{FE}	Static forward current transfer ratio					
	$-I_C = 0.1mA$, $-V_{CE} = 10V$	BFX29	20	90	-	
	$-I_C = 1.0mA$, $-V_{CE} = 10V$	BFX29,87, BFX88	40	105	-	
	$-I_C = 10mA$, $-V_{CE} = 10V$	BFX29	50	125	-	
		BFX87,88	40	125	-	
	$-I_C = 50mA$, $-V_{CE} = 10V$	BFX29	50	125	-	
	$-I_C = 150mA$, $-V_{CE} = 10V$	BFX29,87, BFX88	40	90	-	
	$-I_C = 500mA$, $-V_{CE} = 10V$	BFX87,88	25	40	-	
$-V_{CE(sat)}$	Collector-emitter saturation voltage					
	$-I_C = 150mA$, $-I_B = 15mA$		-	0.15	0.40	V
$-V_{BE(sat)}$	Base-emitter saturation voltage					
	$-I_C = 30mA$, $-I_B = 1.0mA$		-	0.77	0.90	V
	$-I_C = 150mA$, $-I_B = 15mA$		-	1.05	1.30	V
C_{tc}	Collector capacitance					
	$-V_{CB} = 10V$, $I_E = I_e = 0$, $f = 1.0MHz$		-	6.0	12	pF
C_{te}	Emitter capacitance					
	$-V_{EB} = 2.0V$, $I_C = I_c = 0$, $f = 1.0MHz$		-	18	30	pF
f_T	Transition frequency					
	$-I_C = 50mA$, $-V_{CE} = 10V$, $f = 100MHz$, $T_{amb} = 25^oC$		100	360	-	MHz

ELECTRICAL CHARACTERISTICS (cont'd)

Saturated switching times (see test circuits)

		Min.	Typ.	Max.	
t_{on}	Turn-on time	-	25	60	ns
t_{off}	Turn-off time	-	55	150	ns

h-parameters

Measured at $-I_C = 10mA$, $-V_{CE} = 10V$, $f = 1.0kHz$, $T_{amb} = 25^oC$

		Min.	Typ.	Max.	
h_{ie}	Input impedance	-	600	-	Ω
h_{re}	Voltage feedback ratio	-	1.50	-	$\times 10^{-4}$
h_{fe}	Forward current transfer ratio	-	155	-	
h_{oe}	Output admittance	-	104	-	μmho

SOLDERING AND WIRING RECOMMENDATIONS

1. When using a soldering iron, transistors may be soldered directly into the circuit, but heat conducted to the junction should if possible be kept to a minimum by the use of a thermal shunt.

2. Transistors may be dip-soldered at a solder temperature of 245^oC for a maximum soldering time of 5 seconds. The case temperature during soldering must not at any time exceed the maximum storage temperature. These recommendations apply to a transistor mounted flush on a board having punched-through holes, or spaced at least 1.5mm above a board having plated-through holes.

3. Care should be taken not to bend the leads nearer than 1.5mm from the seal.

4. If devices are stored at temperatures above 100^oC before incorporation into equipment, some deterioration of the external surface is likely to occur which may make soldering into the circuit difficult. Under these circumstances the leads should be retinned using a suitable activated flux.

TEST CIRCUITS

Saturated turn-on switching time

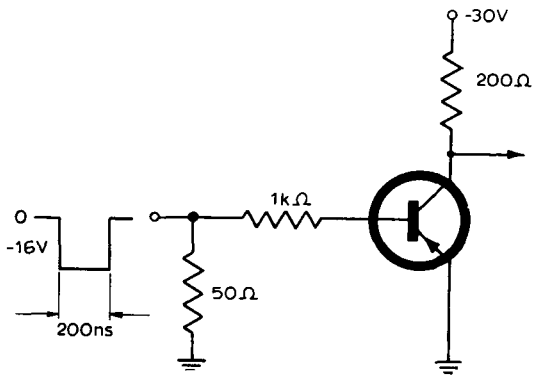


Fig.1

Saturated turn-off switching time

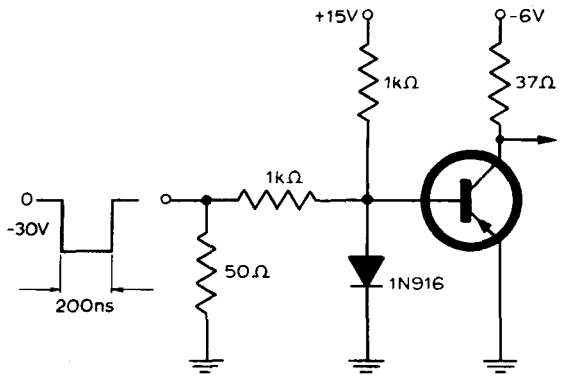
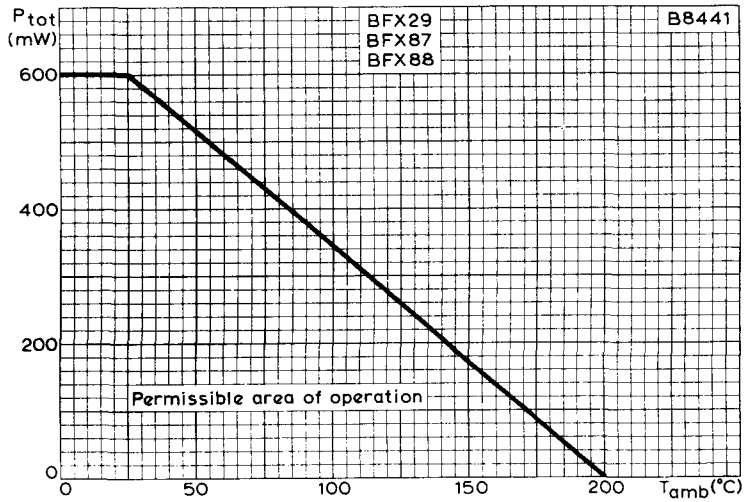
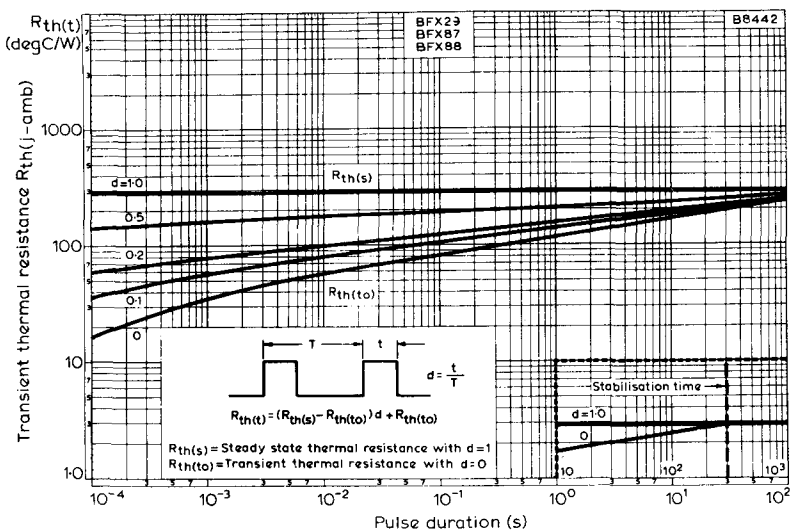


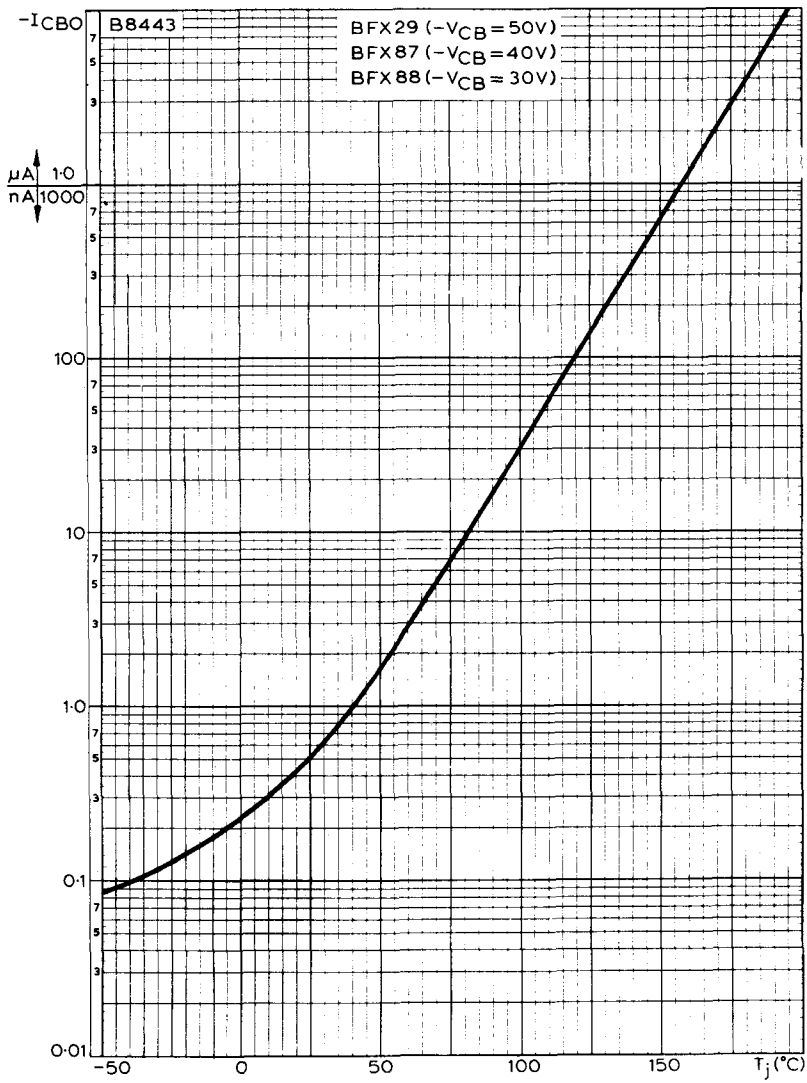
Fig.2



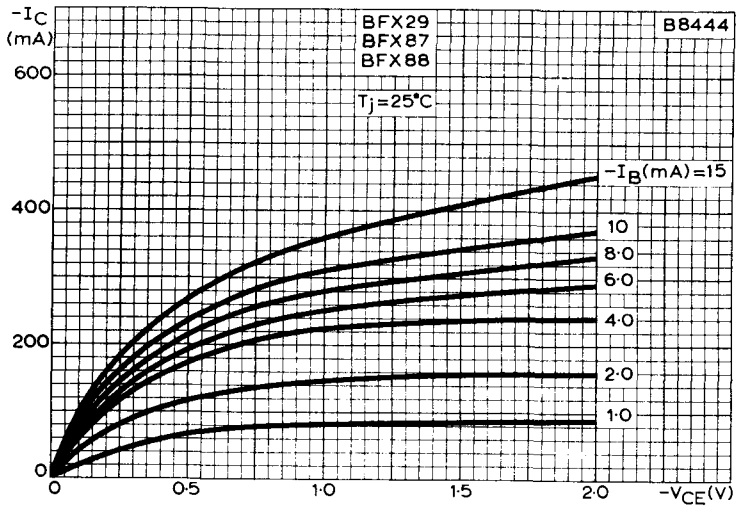
MAXIMUM TOTAL DISSIPATION PLOTTED AGAINST AMBIENT TEMPERATURE

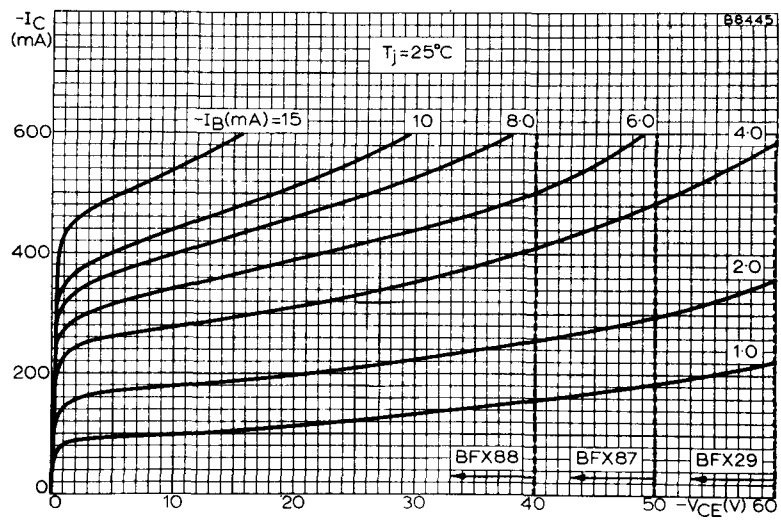


TRANSIENT THERMAL RESISTANCE FOR VARIOUS DUTY FACTORS PLOTTED AGAINST PULSE DURATION

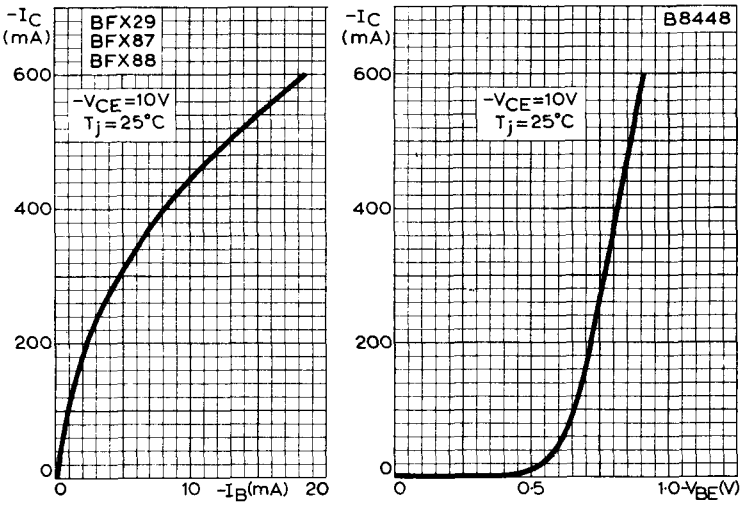


TYPICAL VARIATION OF COLLECTOR CUT-OFF CURRENT
WITH JUNCTION TEMPERATURE

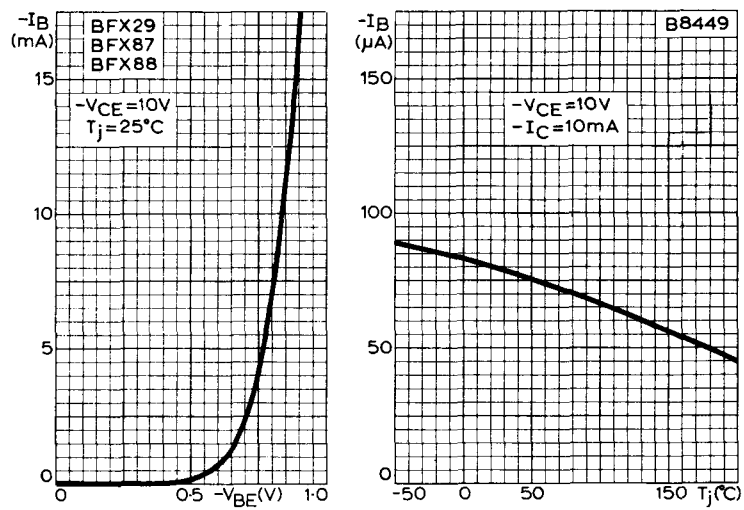




TYPICAL OUTPUT CHARACTERISTICS AT LOW AND HIGH COLLECTOR-EMITTER VOLTAGES

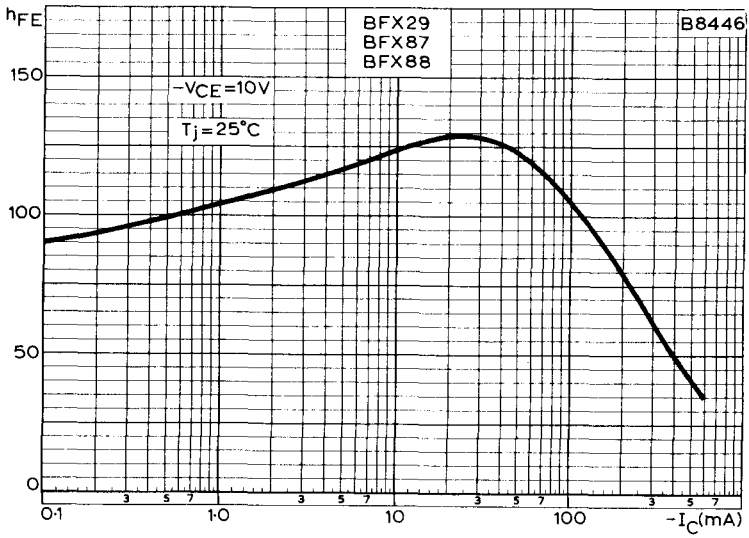


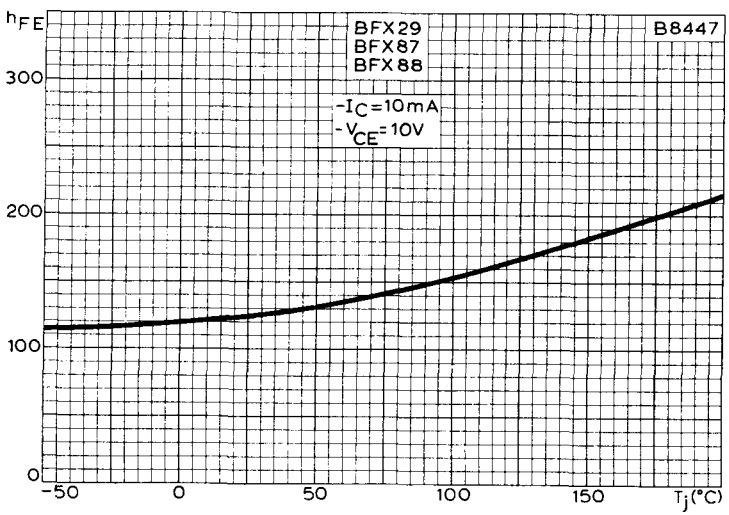
TYPICAL TRANSFER AND MUTUAL CHARACTERISTICS



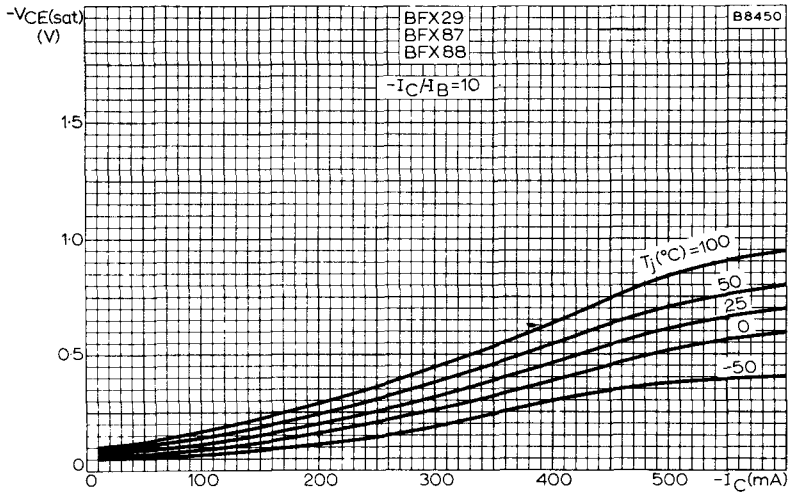
Typical input characteristic

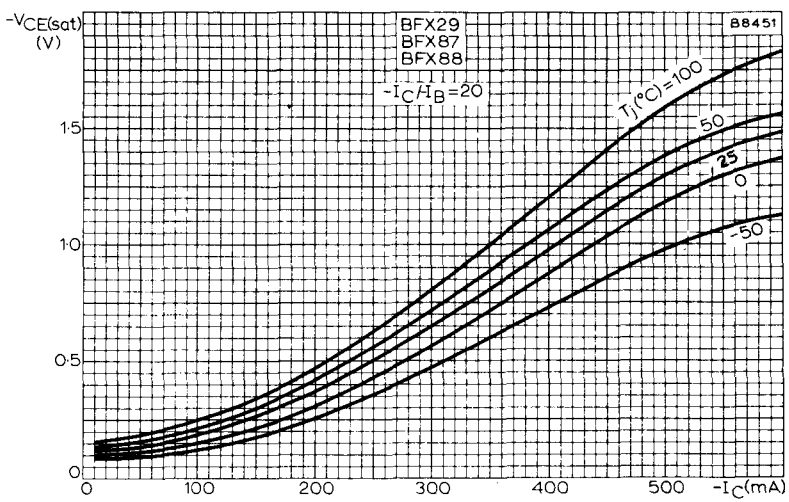
Typical base current versus junction temperature



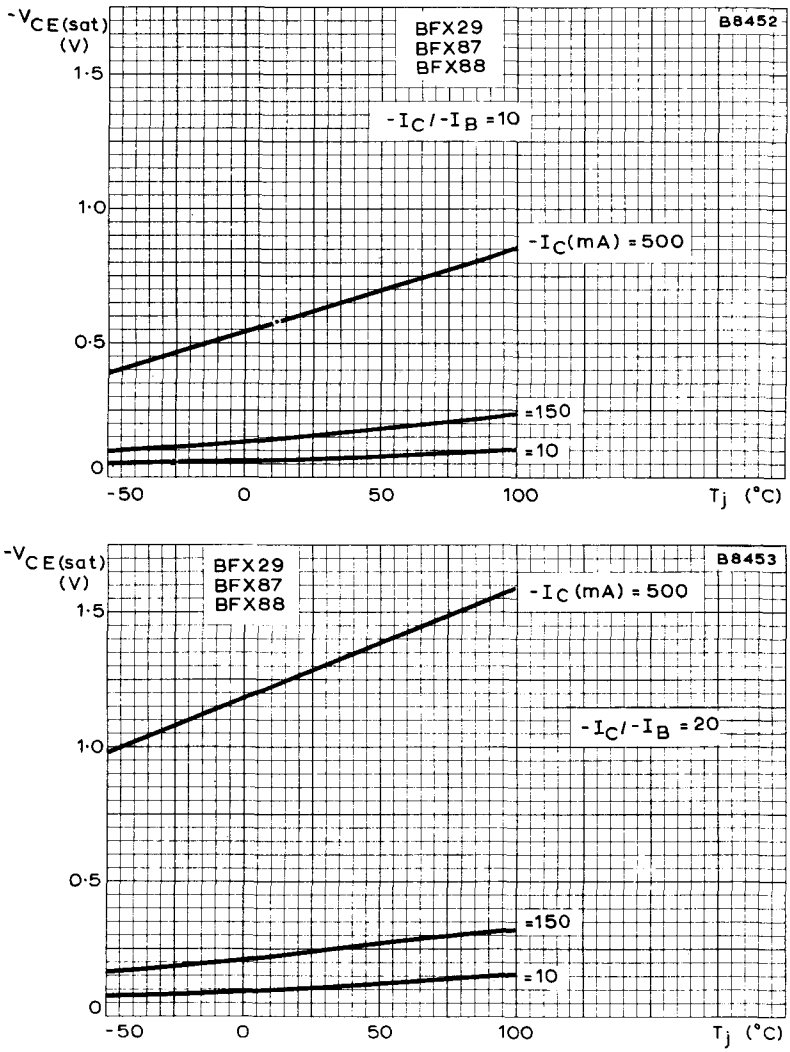


TYPICAL VATIATION OF STATIC FORWARD CURRENT TRANSFER RATIO WITH COLLECTOR CURRENT AND JUNCTION TEMPERATURE

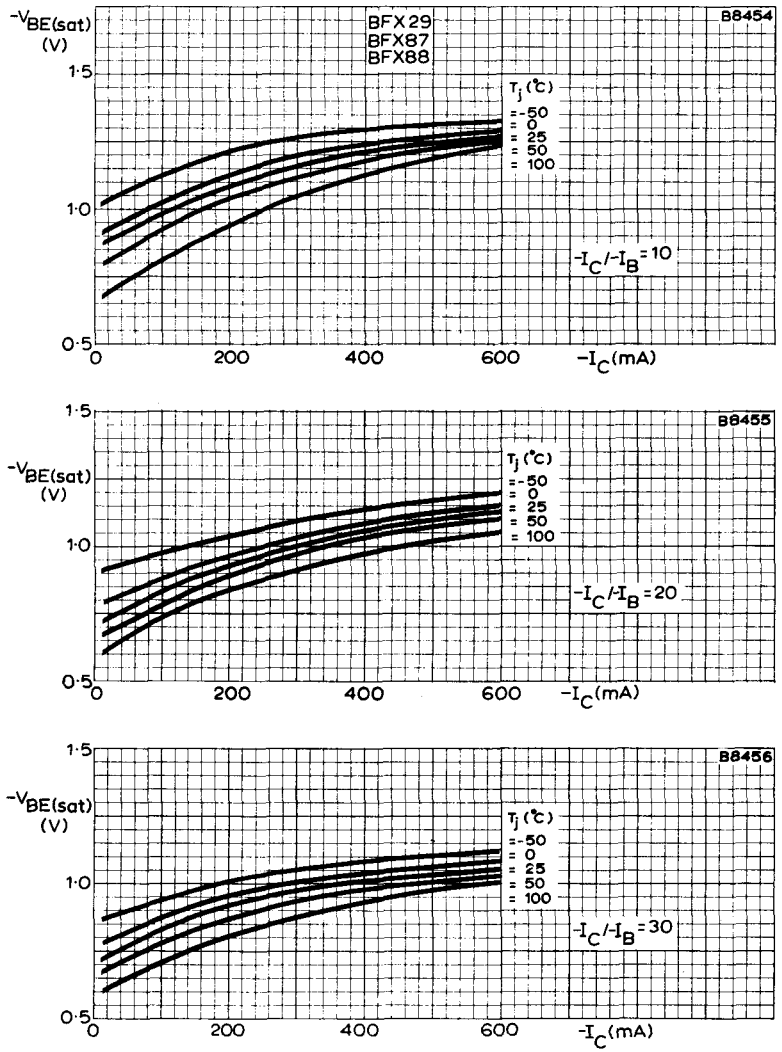




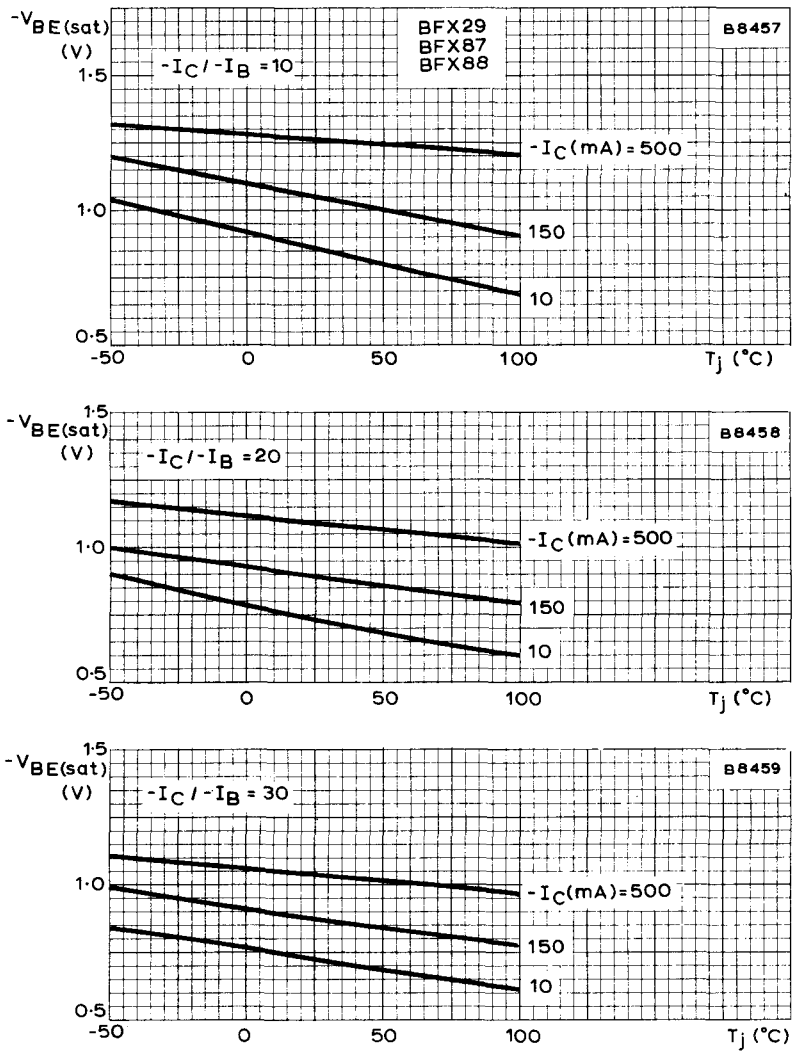
TYPICAL VARIATION OF COLLECTOR-EMITTER SATURATION VOLTAGE WITH COLLECTOR CURRENT



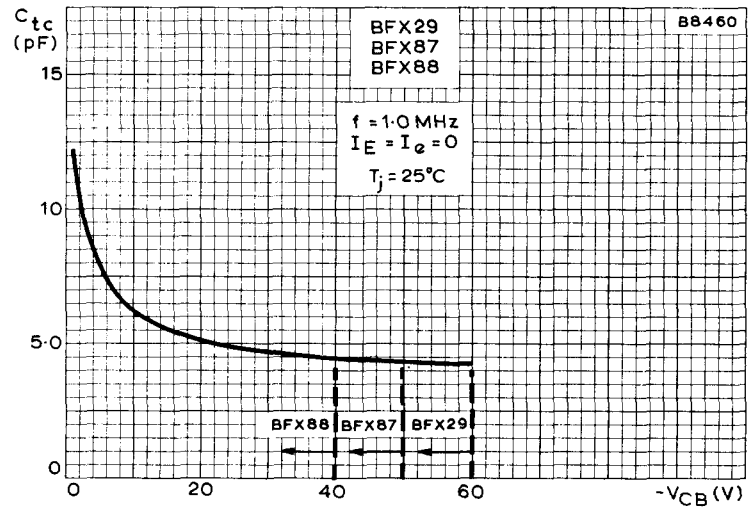
TYPICAL VARIATION OF COLLECTOR-EMITTER SATURATION VOLTAGE WITH JUNCTION TEMPERATURE



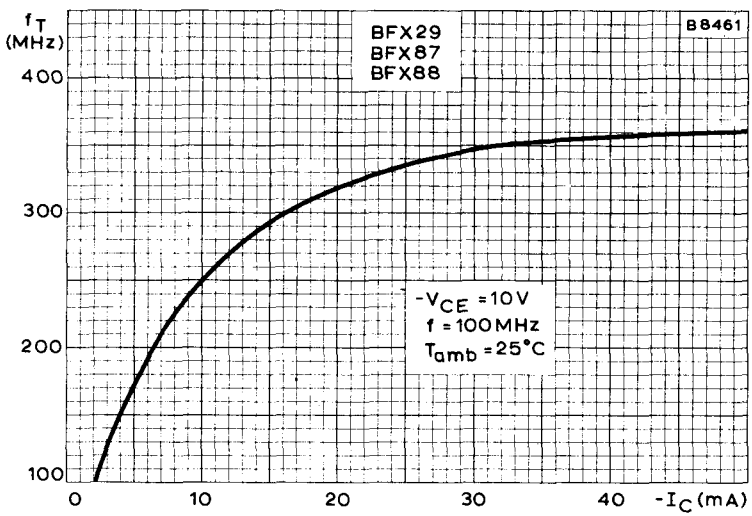
TYPICAL VARIATION OF BASE-EMITTER SATURATION VOLTAGE WITH COLLECTOR CURRENT



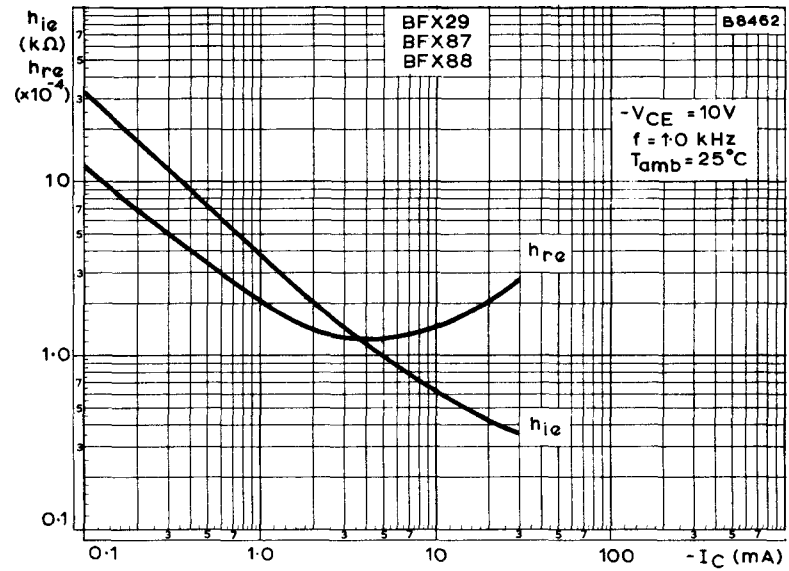
TYPICAL VARIATION OF BASE-EMITTER SATURATION VOLTAGE WITH JUNCTION TEMPERATURE



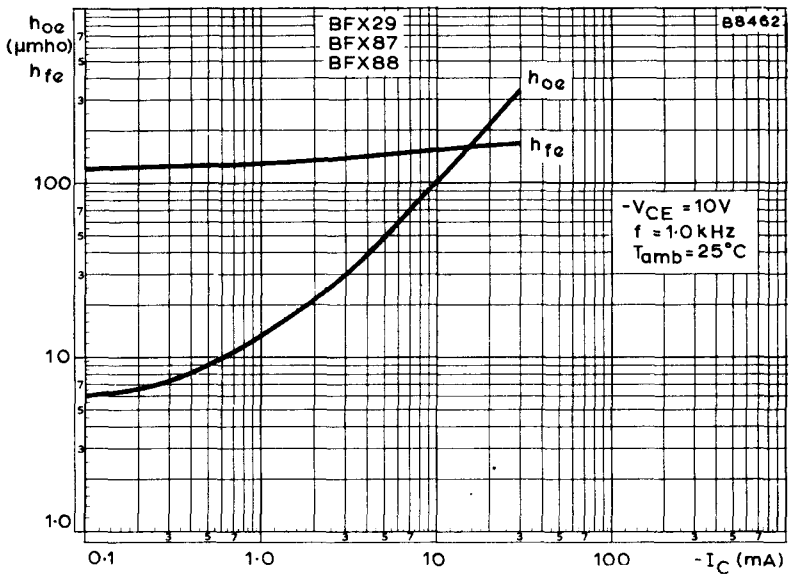
TYPICAL VARIATION OF COLLECTOR CAPACITANCE WITH COLLECTOR-BASE VOLTAGE



TYPICAL VARIATION OF TRANSITION FREQUENCY WITH COLLECTOR CURRENT



TYPICAL INPUT IMPEDANCE AND TYPICAL VOLTAGE FEEDBACK RATIO PLOTTED AGAINST COLLECTOR CURRENT



TYPICAL FORWARD CURRENT TRANSFER RATIO AND TYPICAL OUTPUT ADMITTANCE PLOTTED AGAINST COLLECTOR CURRENT

P-N-P SILICON PLANAR EPITAXIAL TRANSISTOR

BFX30

Also available to BS9365—F011

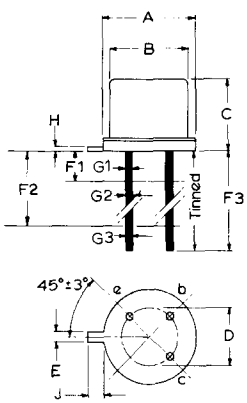
Silicon p-n-p planar epitaxial transistor intended for switching applications. Encapsulated in TO-5 envelope with the collector connected to can.

QUICK REFERENCE DATA			
$-V_{CBO}$ max.		65	V
$-V_{CEO}$ max.		65	V
$-I_{CM}$ max.		600	mA
P_{tot} max. ($T_{amb} \leq 25^{o}C$)		600	mW
h_{FE} ($-I_C = 10mA$, $-V_{CE} = 0.4V$)	min.	50	
	typ.	90	
	max.	200	
t_s max. ($-I_C = 100mA$, $-I_{Bon} = I_{Boff} = 10mA$		250	ns

OUTLINE AND DIMENSIONS

Conforms to B.S. 3934 SO-3/SB3-3A

J.E.D.E.C. TO-5



Collector connected to can

	Millimetres		
	Min.	Nom.	Max.
A	9.10	-	9.40
B	8.20	-	8.50
C	6.10	-	6.60
D	-	5.08	-
E	0.71	-	0.86
F1	-	-	0.51
F2	12.7	-	-
F3	38.1	-	41.3
G1	-	-	1.01
G2	0.41	-	0.48
G3	-	-	0.53
H	-	0.4	-
J	0.74	-	1.0

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

$-V_{CBO}$ max.	65	V
$-V_{CEO}$ max.	65	V
$-V_{EBO}$ max.	5.0	V
$-I_C$ max.	600	mA
$-I_{CM}$ max.	600	mA
$-I_{EM}$ max.	600	mA
P_{tot} max. ($T_{amb} \leq 25^oC$)	600	mW

Temperature

T_{stg} min.	-65	^oC
T_{stg} max.	200	^oC
T_j max.	200	^oC

THERMAL CHARACTERISTIC

$R_{th(j\text{-}amb)}$	292	degC/W

ELECTRICAL CHARACTERISTICS ($T_j = 25^oC$ unless otherwise stated)

		Min.	Typ.	Max.	
$-I_{CBO}$	Collector cut-off current				
	$-V_{CB} = 65V$, $I_E = 0$	-	1.0	500	nA
	$-V_{CB} = 50V$, $I_E = 0$	-	0.5	50	nA
	$-V_{CB} = 50V$, $I_E = 0$, $T_j = 100^oC$	-	0.03	2.0	μA
$-I_{EBO}$	Emitter cut-off current				
	$-V_{EB} = 5.0V$, $I_C = 0$	-	30	500	nA
	$-V_{EB} = 3.0V$, $I_C = 0$	-	1.0	100	nA
$-V_{BE(sat)}$	Base-emitter saturation voltage				
	$-I_C = 30mA$, $-I_B = 1.0mA$	-	0.77	0.90	V
	$-I_C = 150mA$, $-I_B = 15mA$	-	1.05	1.30	V
h_{FE}	Static forward current transfer ratio				
	$-I_C = 1.0mA$, $-V_{CE} = 0.4V$	40	80	-	
	$-I_C = 10mA$, $-V_{CE} = 0.4V$	50	90	200	
	$-I_C = 50mA$, $-V_{CE} = 0.4V$	20	92	-	
	$-I_C = 150mA$, $-V_{CE} = 0.4V$	10	50	-	

ELECTRICAL CHARACTERISTICS (cont'd)

		Min.	Typ.	Max.	
C_{tc}	Collector capacitance $-V_{CB}=10V$, $I_E=I_e=0$, $f=1.0MHz$	-	6.0	12	pF
C_{te}	Emitter capacitance $-V_{EB}=2.0V$, $I_C=I_c=0$, $f=1.0MHz$	-	18	30	pF

Saturated switching times (see page 4)

$-I_C=100mA$, $-I_{Bon}=I_{Boff}=10mA$, $V_{EE}=10V$, $V_{BEoff}=2.0V$

t_d	Delay time	-	9	15	ns
t_r	Rise time	-	18	40	ns
t_{on}	Turn-on time (t_d+t_r)	-	27	50	ns
t_s	Storage time	-	95	250	ns
t_f	Fall time	-	30	50	ns
t_{off}	Turn-off time (t_s+t_f)	-	125	290	ns

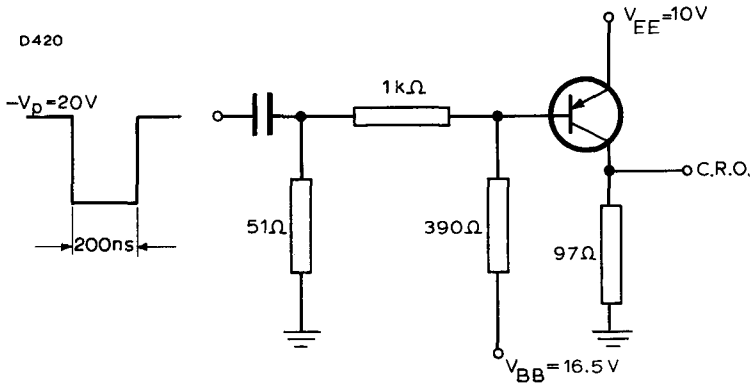
SOLDERING AND WIRING RECOMMENDATIONS

1. When using a soldering iron, transistors may be soldered directly into the circuit, but heat conducted to the junction should if possible be kept to a minimum by the use of a thermal shunt.
2. Transistors may be dip-soldered at a solder temperature of 245°C for a maximum soldering time of 5 seconds. The case temperature during soldering must not at any time exceed the maximum storage temperature. These recommendations apply to a transistor mounted flush on a board having punched-through holes, or spaced at least 1.5mm above a board having plated-through holes.
3. Care should be taken not to bend the leads nearer than 1.5mm from the seal.
4. If devices are stored at temperatures above 100°C before incorporation into equipment, some deterioration of the external surface is likely to occur which may make soldering into the circuit difficult. Under these circumstances the leads should be retinned using a suitable activated flux.

ELECTRICAL CHARACTERISTICS (cont'd)

Saturated switching times

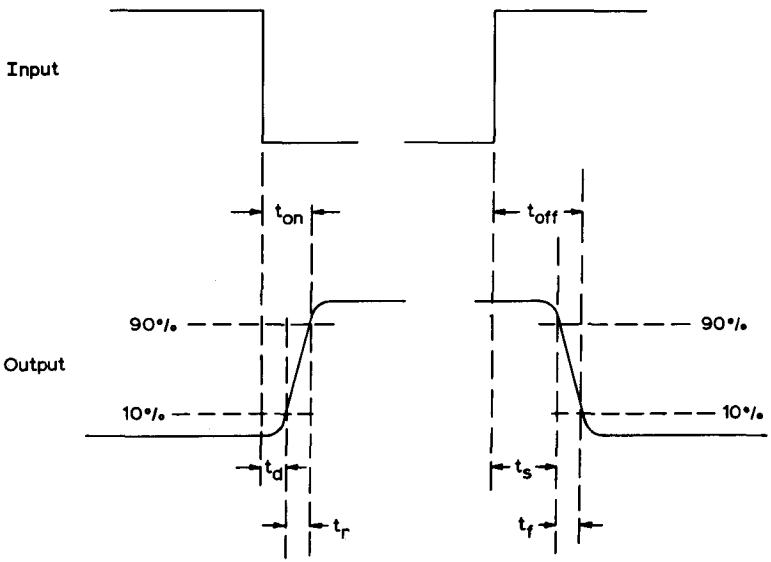
Test circuit

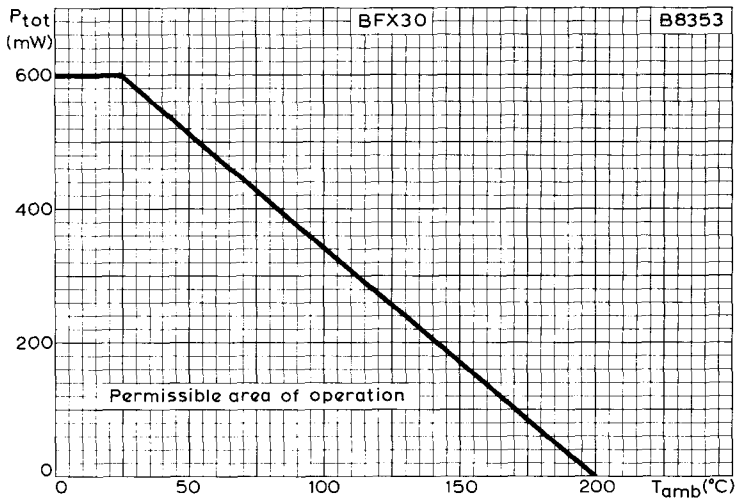


$-I_C$=100mA, $-I_{B(on)} = I_{B(off)}$=10mA

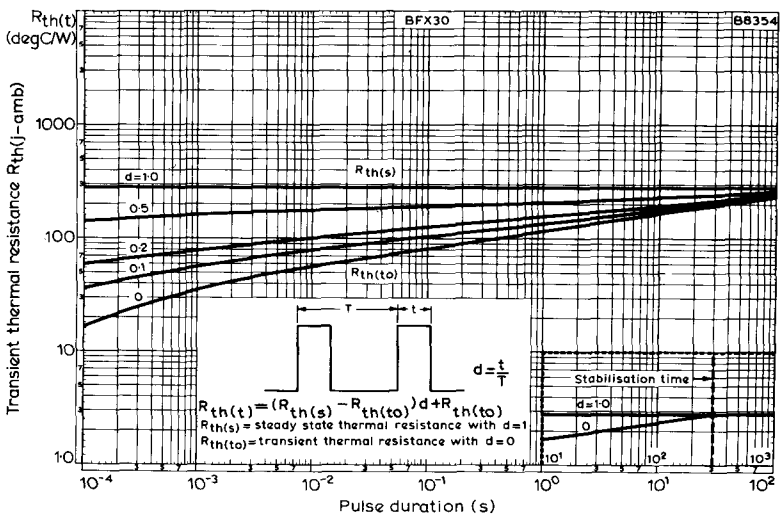
$V_{BE(off)}$=2·0V

Waveforms

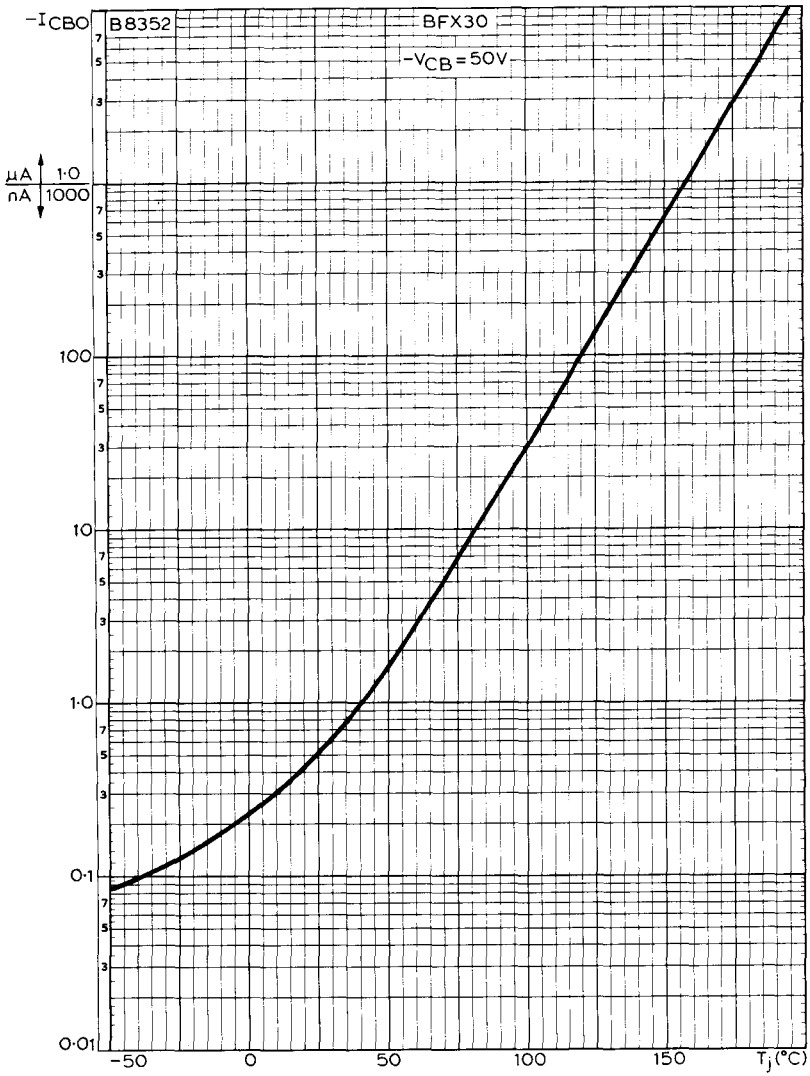




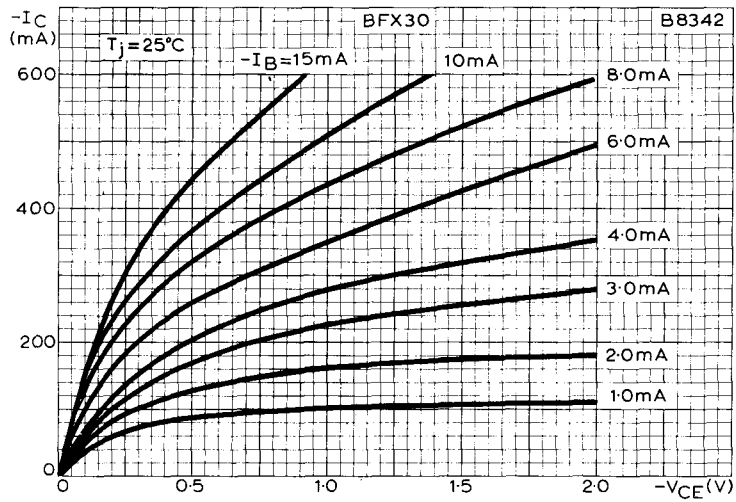
TOTAL DISSIPATION PLOTTED AGAINST AMBIENT TEMPERATURE

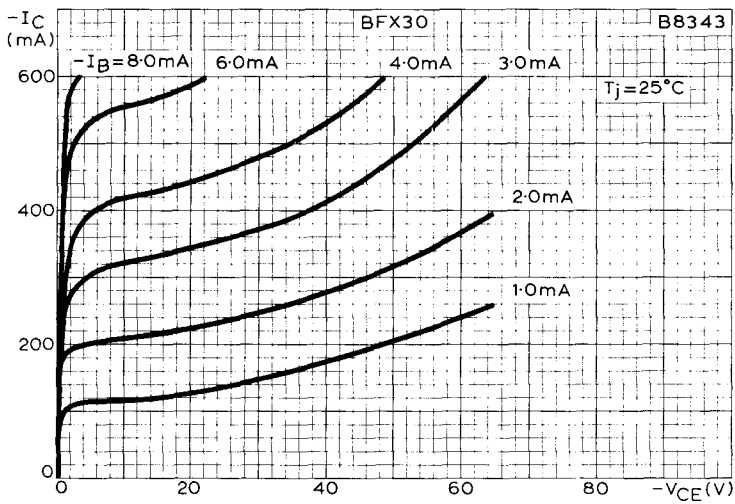


TRANSIENT THERMAL RESISTANCE FOR VARIOUS DUTY FACTORS
PLOTTED AGAINST PULSE DURATION

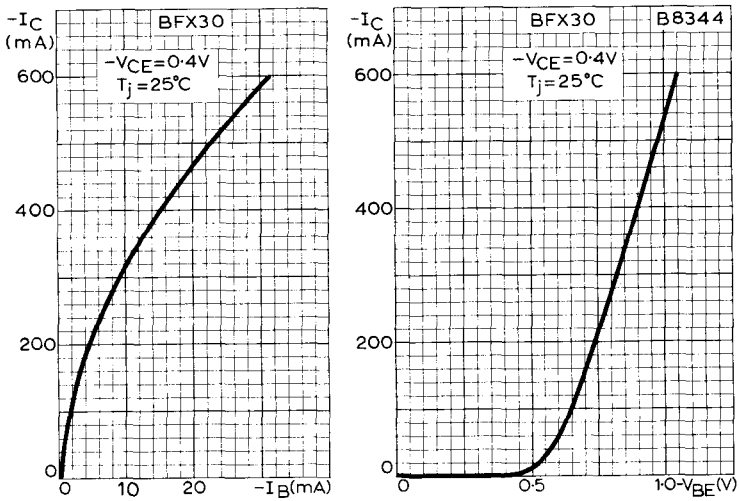


TYPICAL VARIATION OF COLLECTOR CUT-OFF CURRENT WITH JUNCTION TEMPERATURE

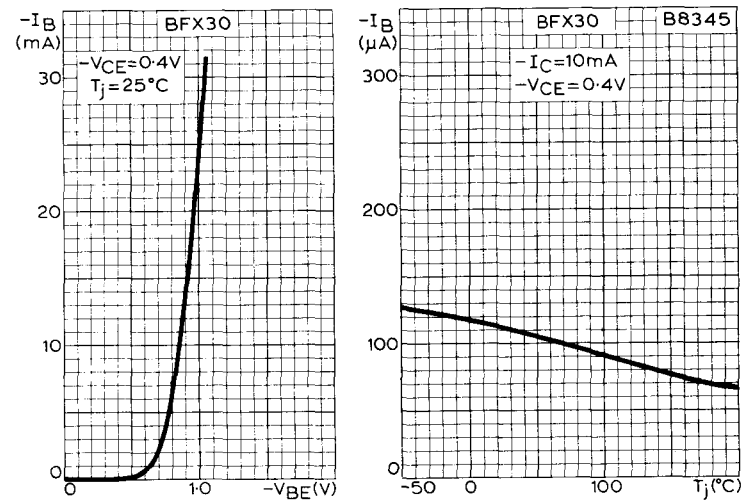




TYPICAL OUTPUT CHARACTERISTICS AT LOW AND HIGH COLLECTOR-EMITTER VOLTAGES

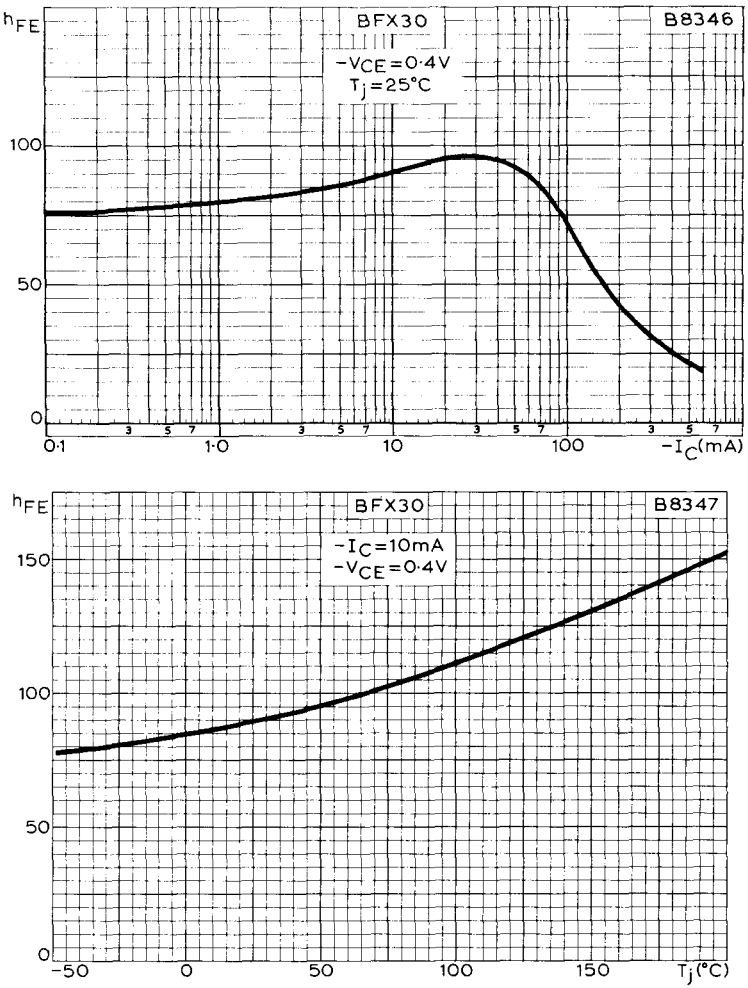


TYPICAL TRANSFER AND MUTUAL CHARACTERISTICS

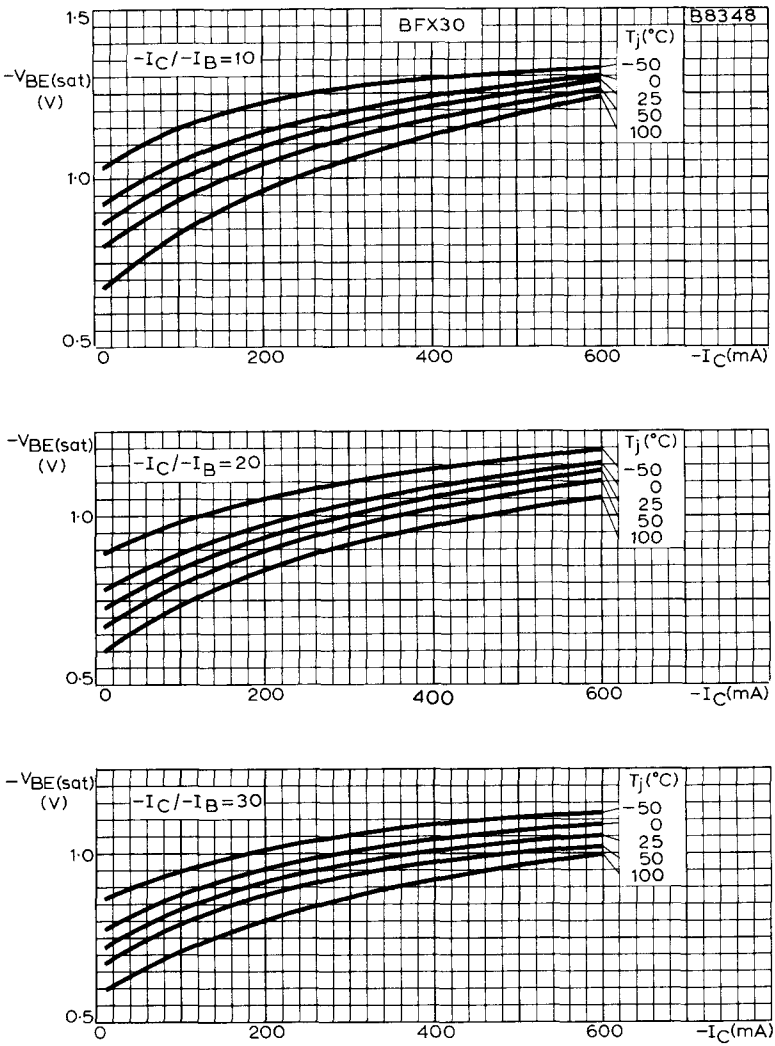


Typical input characteristics

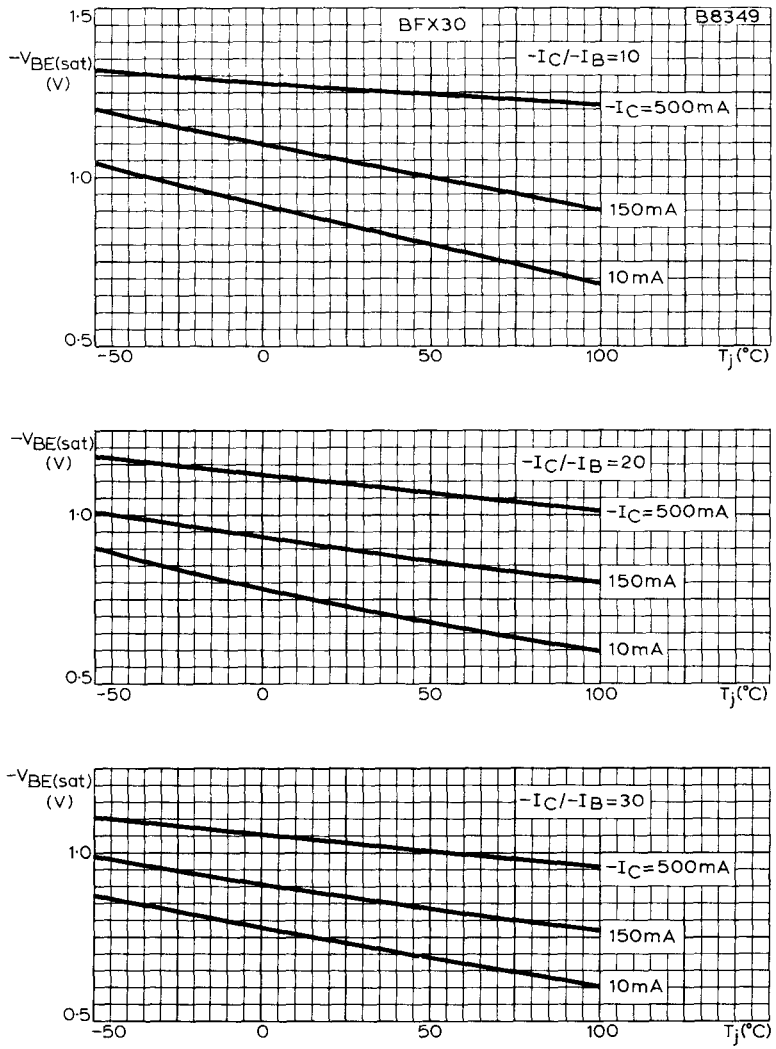
Typical base current versus junction temperature



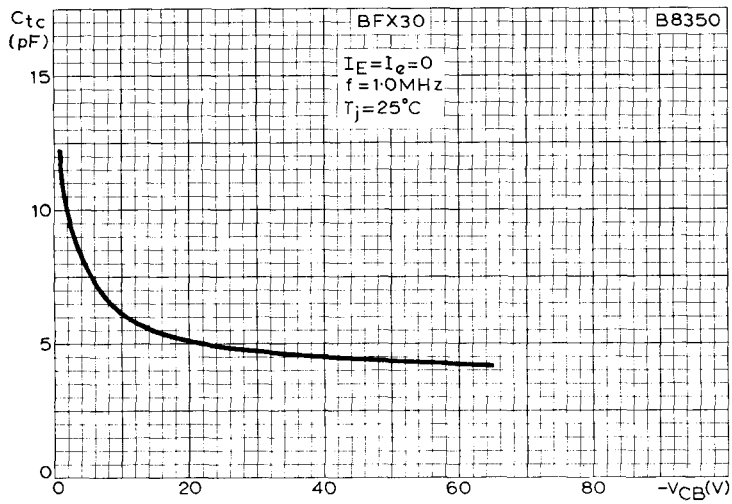
TYPICAL VARIATION OF STATIC FORWARD CURRENT TRANSFER RATIO WITH COLLECTOR CURRENT AND JUNCTION TEMPERATURE



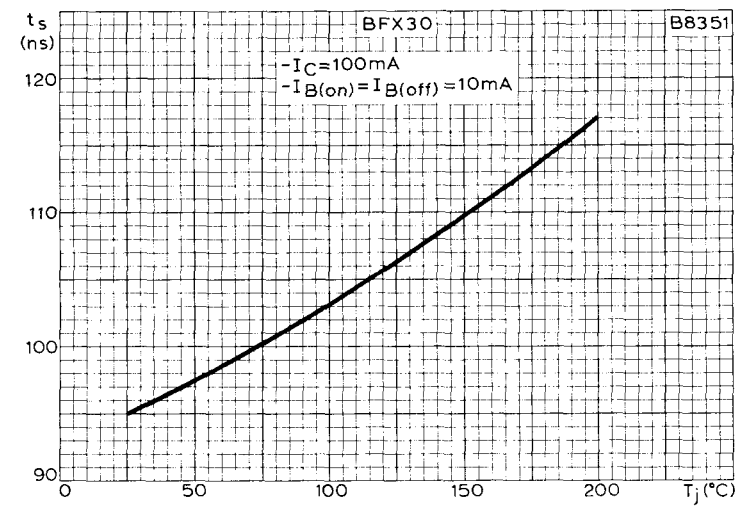
TYPICAL VARIATION OF BASE-EMITTER SATURATION VOLTAGE WITH COLLECTOR CURRENT AND I_C/I_B RATIO



TYPICAL VARIATION OF BASE-EMITTER SATURATION VOLTAGE WITH JUNCTION TEMPERATURE AND I_C/I_B RATIO



TYPICAL VARIATION OF COLLECTOR CAPACITANCE WITH COLLECTOR-BASE VOLTAGE



TYPICAL VARIATION OF STORAGE TIME WITH JUNCTION TEMPERATURE

N-P-N SILICON PLANAR EPITAXIAL TRANSISTORS

BFX84
BFX85
BFX86

Silicon n-p-n planar epitaxial transistors for general purpose industrial applications. Encapsulated in TO-5 envelope with the collector connected to can.

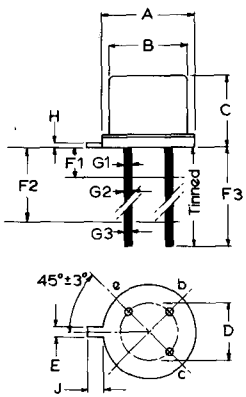
QUICK REFERENCE DATA

	BFX84	BFX85	BFX86	
V_{CBO} max.	100	100	40	V
V_{CEO} max.	60	60	35	V
I_{CM} max.	1.0	1.0	1.0	A
P_{tot} max. $T_{amb} \leq 25^{o}C$	800	800	800	mW
$T_{case} \leq 100^{o}C$	2.86	2.86	2.86	W
h_{FE} (I_C = 150mA, V_{CE} = 10V) min.	30	70	70	
typ.	112	142	142	
f_T min. (I_C = 50mA, V_{CE} = 10V, f = 35MHz, $T_{amb} = 25^{o}C$)	50	50	50	MHz

Unless otherwise stated data is applicable to all types

OUTLINE AND DIMENSIONS

Conforms to B.S. 3934 SO-3/SB3-3A
J.E.D.E.C. TO-5



The collector is electrically connected to the envelope

	Millimetres		
	Min.	Nom.	Max.
A	9.10	-	9.40
B	8.20	-	8.50
C	6.10	-	6.60
D	-	5.08	-
E	0.71	-	0.86
F1	-	-	0.51
F2	12.7	-	-
F3	38.1	-	41.3
G1	-	-	1.01
G2	0.41	-	0.48
G3	-	-	0.53
H	-	0.4	-
J	0.74	-	1.0

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

	BFX84	BFX85	BFX86	
V_{CBO} max.	100	100	40	V
V_{CE} max. (cut-off, $I_C \leq 1mA$)	100	100	40	V
V_{CEO} max.	60	60	35	V
V_{EBO} max.		6.0		V
I_C max.		1.0		A
I_{CM} max.		1.0		A
$-I_E$ max.		1.0		A
$-I_{EM}$ max.		1.0		A
I_B max.		100		mA
$\pm I_{BM}$ max.		100		mA
P_{tot} max. $T_{amb} \leq 25^oC$		800		mW
$T_{case} \leq 25^oC$		5.0		W
$T_{case} > 25, < 100^oC$		2.86		W

Temperature

T_{stg}	-65 to +200	^oC
T_j max.	200	^oC

THERMAL CHARACTERISTICS

$R_{th(j\text{-}amb)}$ in free air	220	degC/W
$R_{th(j\text{-}case)}$	35	degC/W

BFX84

ELECTRICAL CHARACTERISTICS ($T_j = 25^oC$ unless otherwise stated)

		Min.	Typ.	Max.	
I_{CBO}	Collector cut-off current				
	$V_{CB} = 100V$, $I_E = 0$	-	10	500	nA
	$V_{CB} = 100V$, $I_E = 0$, $T_j = 100^oC$	-	0.5	30	μA
	$V_{CB} = 80V$, $I_E = 0$	-	2.0	50	nA
	$V_{CB} = 80V$, $I_E = 0$, $T_j = 100^oC$	-	0.1	2.5	μA
I_{EBO}	Emitter cut-off current				
	$V_{EB} = 6.0V$, $I_C = 0$	-	10	500	nA
	$V_{EB} = 5.0V$, $I_C = 0$	-	2.0	50	nA
	$V_{EB} = 5.0V$, $I_C = 0$, $T_j = 100^oC$	-	0.1	2.5	μA
h_{FE}	Static forward current transfer ratio				
	$I_C = 10mA$, $V_{CE} = 10V$	20	80	-	
	$I_C = 150mA$, $V_{CE} = 10V$	30	112	-	
	$I_C = 500mA$, $V_{CE} = 10V$	20	70	-	
	$I_C = 1.0A$, $V_{CE} = 10V$	15	35	-	
$V_{CE(sat)}$	Collector-emitter saturation voltage				
	$I_C = 10mA$, $I_B = 1.0mA$	-	0.06	0.15	V
	$I_C = 150mA$, $I_B = 15mA$	-	0.15	0.35	V
	$I_C = 500mA$, $I_B = 50mA$	-	0.35	1.00	V
	$I_C = 1.0A$, $I_B = 100mA$	-	0.66	1.60	V
$V_{BE(sat)}$	Base-emitter saturation voltage				
	$I_C = 10mA$, $I_B = 1.0mA$	-	0.69	1.2	V
	$I_C = 150mA$, $I_B = 15mA$	-	0.92	1.3	V
	$I_C = 500mA$, $I_B = 50mA$	-	1.15	1.5	V
	$I_C = 1.0A$, $I_B = 100mA$	-	1.40	2.0	V
C_{Tc}	Collector capacitance $V_{CB} = 10V$, $I_E = I_e = 0$, $f = 1.0MHz$	-	7.0	12	pF

ELECTRICAL CHARACTERISTICS (contd.)

		Min.	Typ.	Max.	
f_T	Transition frequency $I_C = 50mA$, $V_{CE} = 10V$, $f = 35MHz$, $T_{amb} = 25^oC$	50	185	-	MHz
	Saturated switching times				
	$I_C = 150mA$, $I_{B(on)} = -I_{B(off)} = 15mA$, $-V_{EE} = 10V$, $-V_{BE(off)} = 2.0V$				
t_d	Delay time	-	15	-	ns
t_r	Rise time	-	40	-	ns
t_{on}	Turn-on time	-	55	-	ns
t_s	Storage time	-	300	-	ns
t_f	Fall time	-	60	-	ns
t_{off}	Turn-off time	-	360	-	ns
	h-parameters				
h_{fe}	$I_C = 1.0mA$, $V_{CE} = 5.0V$, $f = 1.0kHz$, $T_{amb} = 25^oC$	20	65	-	
h_{ie}	$I_C = 10mA$, $V_{CE} = 5.0V$, $f = 1.0kHz$, $T_{amb} = 25^oC$	-	250	750	Ω
h_{re}		-	0.85	5.0	$\times 10^{-4}$
h_{fe}		25	80	-	
h_{oe}		-	35	80	μmho

BFX86

ELECTRICAL CHARACTERISTICS ($T_j = 25^oC$ unless otherwise stated)

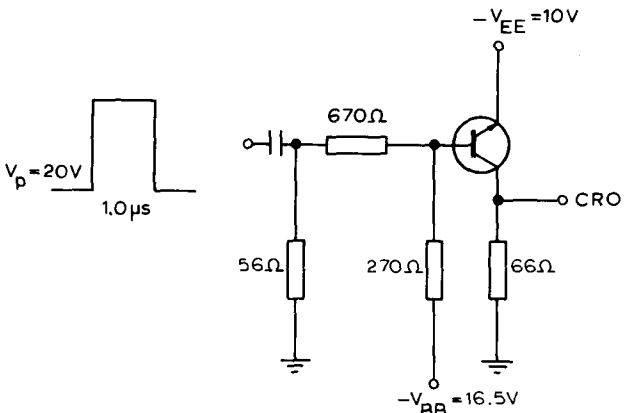
		Min.	Typ.	Max.	
I_{CBO}	Collector cut-off current				
	$V_{CB} = 40V$, $I_E = 0$	-	10	500	nA
	$V_{CB} = 40V$, $I_E = 0$, $T_j = 100^oC$	-	0.5	30	μA
	$V_{CB} = 30V$, $I_E = 0$	-	2.0	50	nA
	$V_{CB} = 30V$, $I_E = 0$, $T_j = 100^oC$	-	0.1	2.5	μA
I_{EBO}	Emitter cut-off current				
	$V_{EB} = 6.0V$, $I_C = 0$	-	10	500	nA
	$V_{EB} = 5.0V$, $I_C = 0$	-	2.0	50	nA
	$V_{EB} = 5.0V$, $I_C = 0$, $T_j = 100^oC$	-	0.1	2.5	μA
h_{FE}	Static forward current transfer ratio				
	$I_C = 10mA$, $V_{CE} = 10V$	50	90	-	
	$I_C = 150mA$, $V_{CE} = 10V$	70	142	-	
	$I_C = 500mA$, $V_{CE} = 10V$	30	90	-	
	$I_C = 1.0A$, $V_{CE} = 10V$	15	50	-	
$V_{CE(sat)}$	Collector-emitter saturation voltage				
	$I_C = 10mA$, $I_B = 1.0mA$	-	0.06	0.15	V
	$I_C = 150mA$, $I_B = 15mA$	-	0.15	0.35	V
	$I_C = 500mA$, $I_B = 50mA$	-	0.35	1.00	V
	$I_C = 1.0A$, $I_B = 100mA$	-	0.66	1.60	V
$V_{BE(sat)}$	Base-emitter saturation voltage				
	$I_C = 10mA$, $I_B = 1.0mA$	-	0.69	1.2	V
	$I_C = 150mA$, $I_B = 15mA$	-	0.92	1.3	V
	$I_C = 500mA$, $I_B = 50mA$	-	1.15	1.5	V
	$I_C = 1.0A$, $I_B = 100mA$	-	1.40	2.0	V
C_{Tc}	Collector capacitance $V_{CB} = 10V$, $I_E = I_e = 0$, $f = 1.0MHz$	-	7.0	12	pF

ELECTRICAL CHARACTERISTICS (contd.)

		Min.	Typ.	Max.	
f_T	Transition frequency $I_C = 50mA$, $V_{CE} = 10V$, $f = 35MHz$, $T_{amb} = 25^oC$	50	185	-	MHz
Saturated switching times					
	$I_C = 150mA$, $I_{B(on)} = -I_{B(off)} = 15mA$, $-V_{EE} = 10V$, $-V_{BE(off)} = 2.0V$				
t_d	Delay time	-	15	-	ns
t_r	Rise time	-	40	-	ns
t_{on}	Turn-on time	-	55	-	ns
t_s	Storage time	-	300	-	ns
t_f	Fall time	-	60	-	ns
t_{off}	Turn-off time	-	360	-	ns
h-parameters					
h_{fe}	$I_C = 1.0mA$, $V_{CE} = 5.0V$, $f = 1.0kHz$, $T_{amb} = 25^oC$	20	65	-	
h_{ie}	$I_C = 10mA$, $V_{CE} = 5.0V$, $f = 1.0kHz$, $T_{amb} = 25^oC$	-	250	750	Ω
h_{re}		-	0.85	5.0	$\times 10^{-4}$
h_{fe}		25	80	-	
h_{oe}		-	35	80	μmho

MEASUREMENT OF SATURATED SWITCHING TIMES

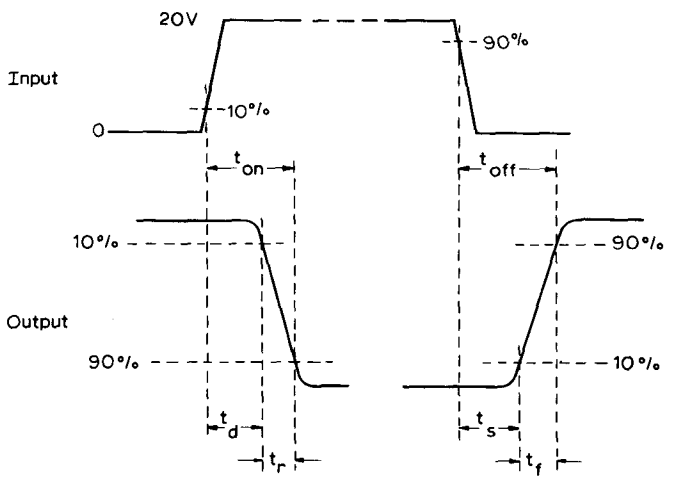
Test circuit



I_C=150mA, $I_{B(on)}$ = $-I_{B(off)}$ =15mA

$-V_{BE(off)}$ = 2.0 V

Switching waveforms



OPERATING NOTES

1. Dissipation and heatsink considerations

a) Steady-state conditions

The maximum steady-state dissipation P_s is given by the relationship:

$$P_{s\ max.} = \frac{T_{j\ max.} - T_{amb}}{R_{th(j-amb)}}$$

Where $T_{j\ max.}$ is the maximum permissible operating junction temperature,
T_{amb} is the ambient temperature,
$R_{th(j-amb)}$ is the total thermal resistance between junction and ambient.

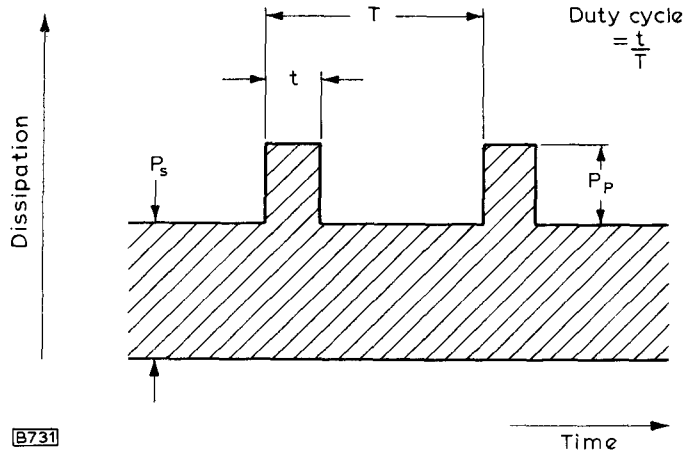
Page 13 gives the maximum allowable steady-state dissipation versus ambient temperature for the device mounted in free air and with infinite heatsink.

b) Pulse conditions (rectangular pulses)

The maximum pulse power P_p is given by the formula

$$P_p = \frac{(T_{j\ max.} - T_{amb}) - (P_s . R_{th(j-amb)})}{R_{th(t)} + d . R_{th(case-amb)}}$$

Where P_s is the steady-state dissipation excluding that in the pulses,
$R_{th(t)}$ is effective transient thermal resistance of the device between junction and case, and is a function of the pulse duration t, and duty cycle d,
d is the duty cycle, and is equal to the pulse duration t divided by the periodic time T,
$R_{th(case-amb)}$ is the total thermal resistance between case and ambient and is equal to the difference between $R_{th(j-amb)}$ and the thermal resistance from junction to case $R_{th(j-case)}$.



b) Pulse conditions (rectangular pulses) (cont'd)

Example

The following example shows how to calculate the maximum permissible peak dissipation of a BFX84 mounted in free air at a temperature not exceeding 65°C. The steady-state dissipation under the bottomed condition is 350mW, the pulse width is 1ms and the duty cycle is 0.2.

The transient thermal resistance $R_{th(t)}$ = 15.5degC/W (page 13)

$$P_p \text{ max.} = \frac{(200-65) - (0.35\times220)}{15.5+0.2(220-35)}$$

$$= \frac{135-77}{15.5+37}$$

$$= 1.1\text{W}$$

The peak pulse dissipation of 1.1W is therefore allowed provided that the voltage and current ratings of the device are not exceeded.

c) Pulse conditions (other than rectangular)

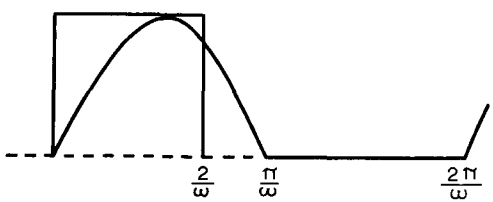
For sinusoidal and irregular shaped waveforms, the power pulse is converted to an equivalent rectangular pulse of the same average and peak values, and treated as in the previous section.

Example

The following example illustrates how to find the maximum permissible peak dissipation of a BFX84 operating in a class 'B' circuit at 1kHz. The device is mounted on a heatsink of thermal resistance equal to 50degC/W and at an ambient temperature not exceeding 100°C. Assuming that the waveform is sinusoidal for half period and zero for the other half.

Average of sinewave over half cycle = $2P_p/\pi$

Therefore equivalent rectangular pulse width of same amplitude and average value



B3559

$$t = \frac{2}{\omega}$$

$$= \frac{2}{2\pi \times 10^3}$$

$$= 0.318\text{ms}$$

Duty cycle, $d = \frac{1}{\pi}$

c) Pulse conditions (other than rectangular) (cont'd)

$$\text{Duty cycle, } d = \frac{2}{\omega} \Big/ \frac{2\pi}{\omega} = \frac{1}{\pi} = 0.318$$

From page 13

$$R_{th(t)} = 6.8\text{degC/W } (d=0)$$
$$R_{th(s)} = 35\text{degC/W}$$
$$R_{th(t)} \text{ at } d=0.318 = (35-6.8) \times 0.318 + 6.8$$
$$= 15.8\text{degC/W}$$

$$P_p \text{ max.} = \frac{(200-100)-0}{15.8+0.318\times 50}$$

$$= \frac{100}{31.7} = 3.15\text{W}$$

A peak power of 3.15W is therefore permissible provided that the voltage and current ratings of the device are not exceeded.

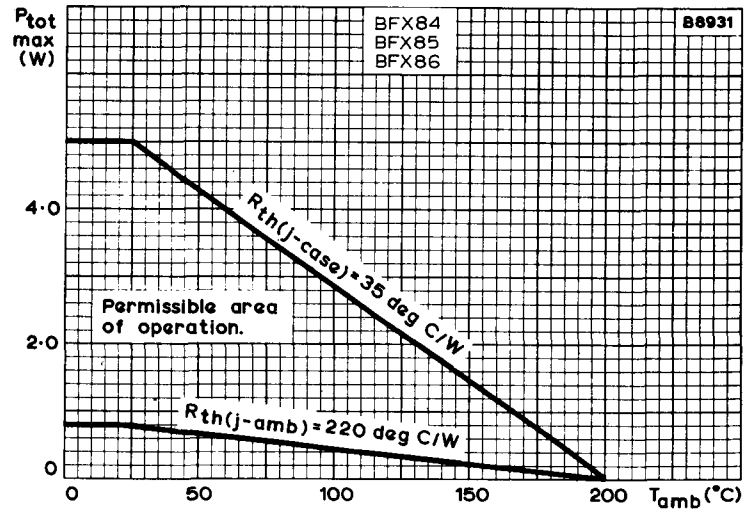
SOLDERING AND WIRING RECOMMENDATIONS

1. When using a soldering iron, transistors may be soldered directly into the circuit, but heat conducted to the junction should if possible be kept to a minimum by the use of a thermal shunt.

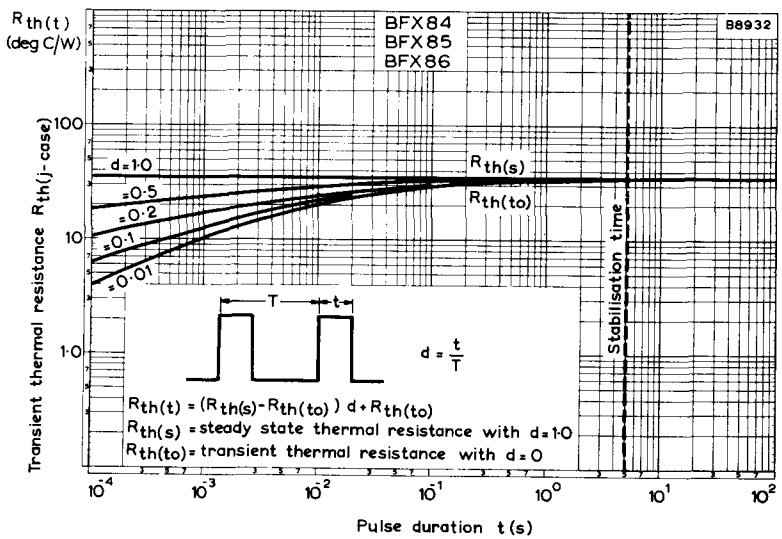
2. Transistors may be dip-soldered at a solder temperature of 245°C for a maximum soldering time of 5 seconds. The case temperature during soldering must not at any time exceed the maximum storage temperature. These recommendations apply to a transistor mounted flush on a board having punched-through holes, or spaced at least 1.5mm above a board having plated-through holes.

3. Care should be taken not to bend the leads nearer than 1.5mm from the seal.

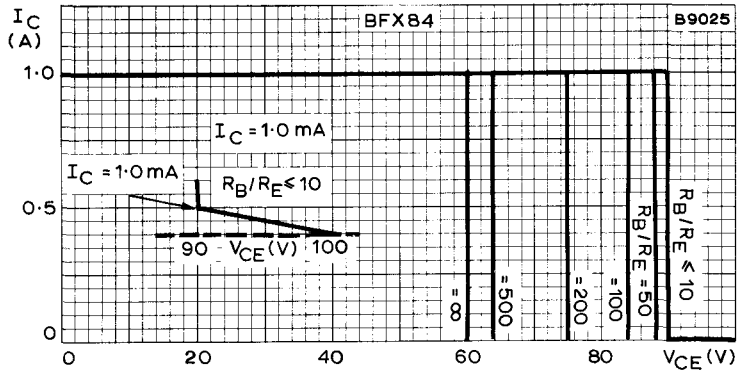
4. If devices are stored at temperatures above 100°C before incorporation into equipment, some deterioration of the external surface is likely to occur which may make soldering into the circuit difficult. Under these circumstances the leads should be retinned using a suitable activated flux.

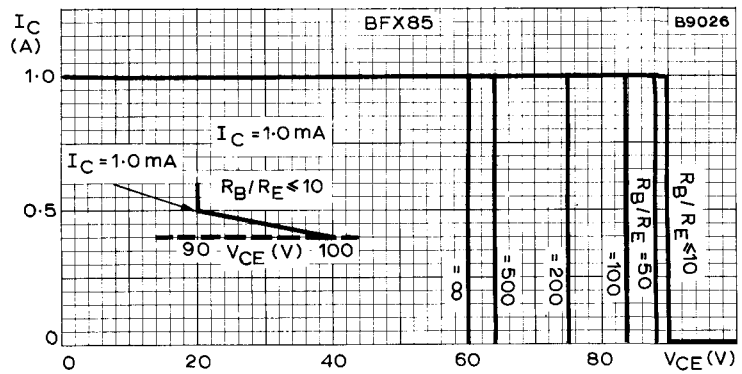


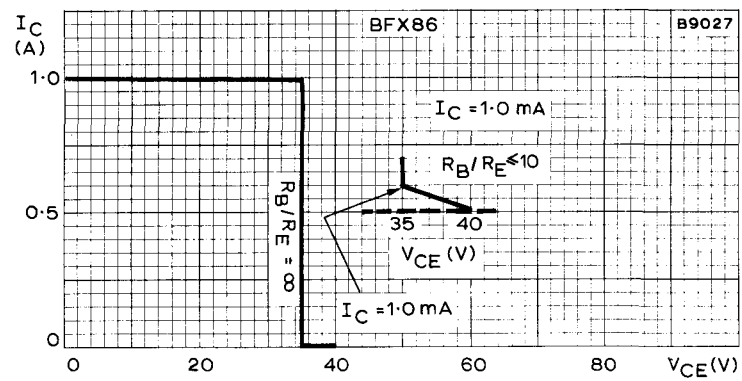
MAXIMUM TOTAL DISSIPATION PLOTTED AGAINST AMBIENT TEMPERATURE



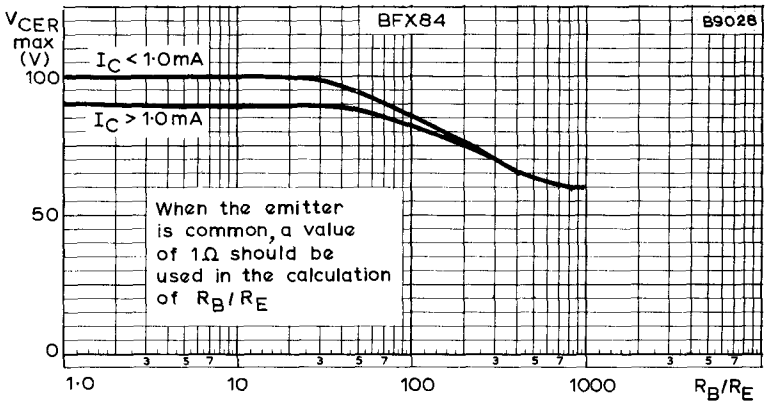
TRANSIENT THERMAL RESISTANCE FOR VARIOUS DUTY FACTORS PLOTTED AGAINST PULSE DURATION

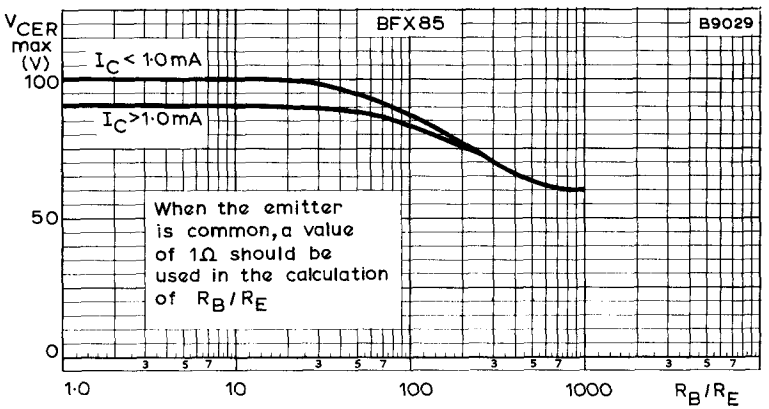


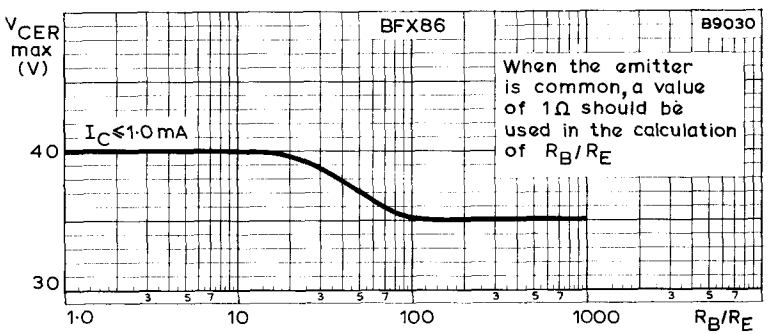




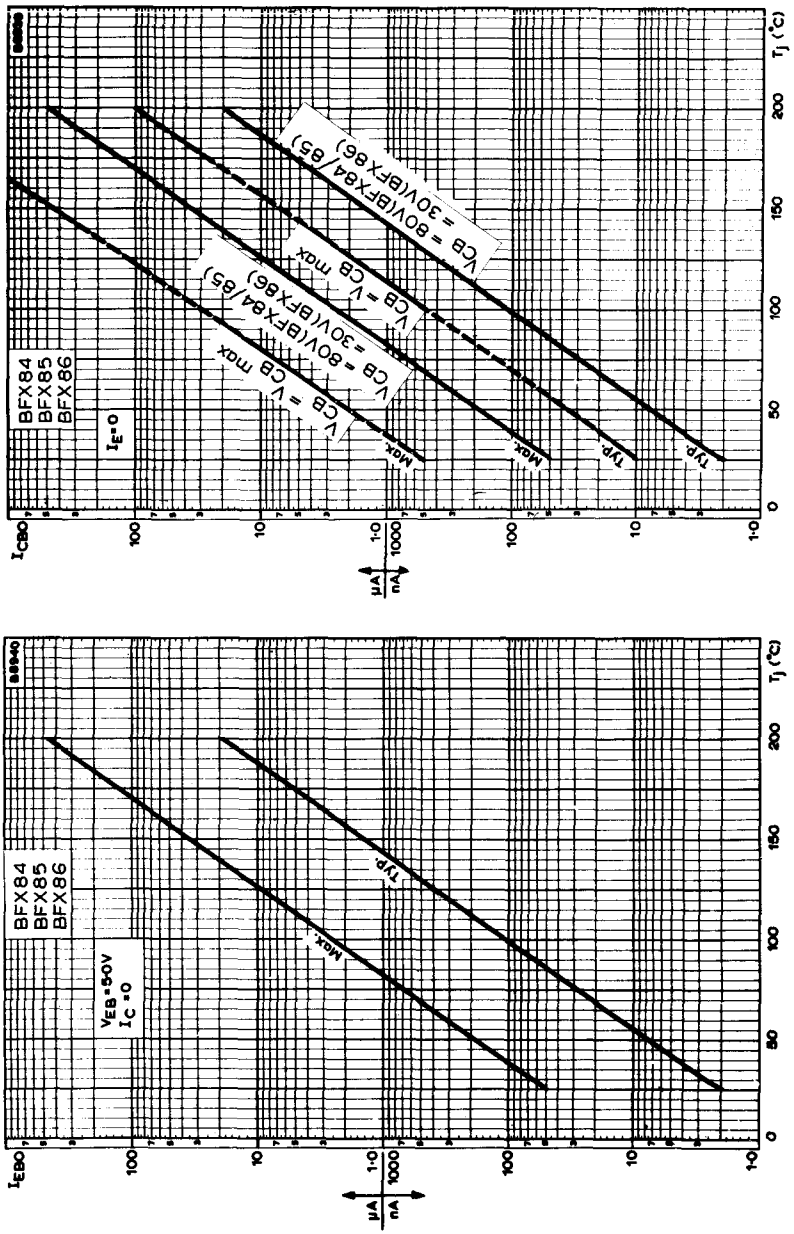
COLLECTOR CURRENT PLOTTED AGAINST MAXIMUM COLLECTOR-EMITTER VOLTAGE WITH R_B/R_E AS PARAMETER



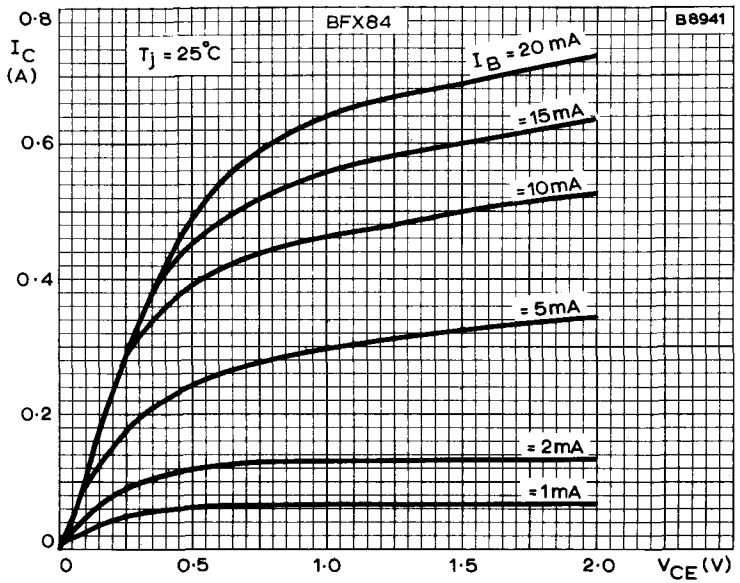


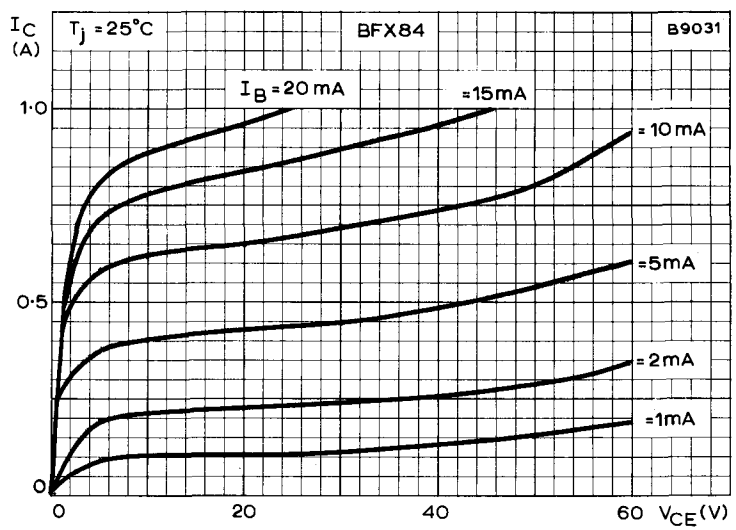


MAXIMUM COLLECTOR-EMITTER VOLTAGE PLOTTED AGAINST R_B/R_E RATIO

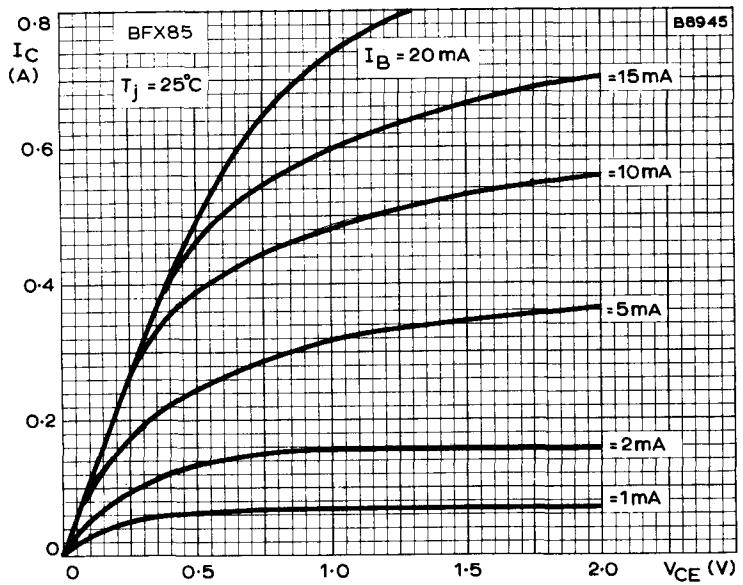


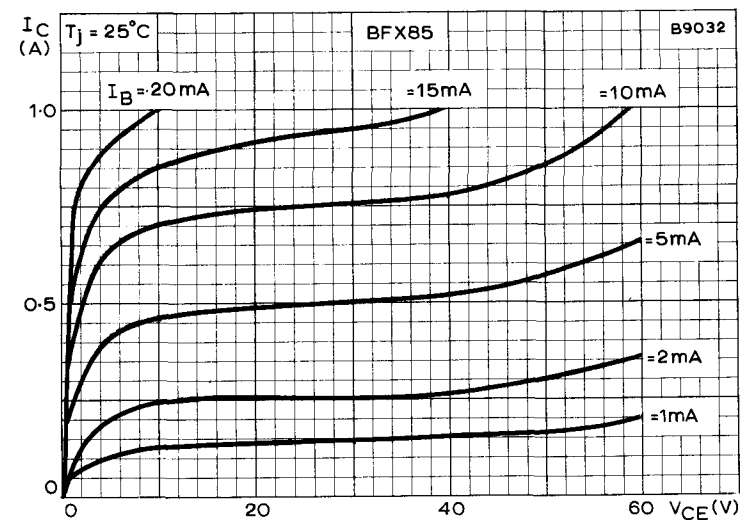
COLLECTOR AND EMITTER CUT-OFF CURRENTS PLOTTED AGAINST JUNCTION TEMPERATURE



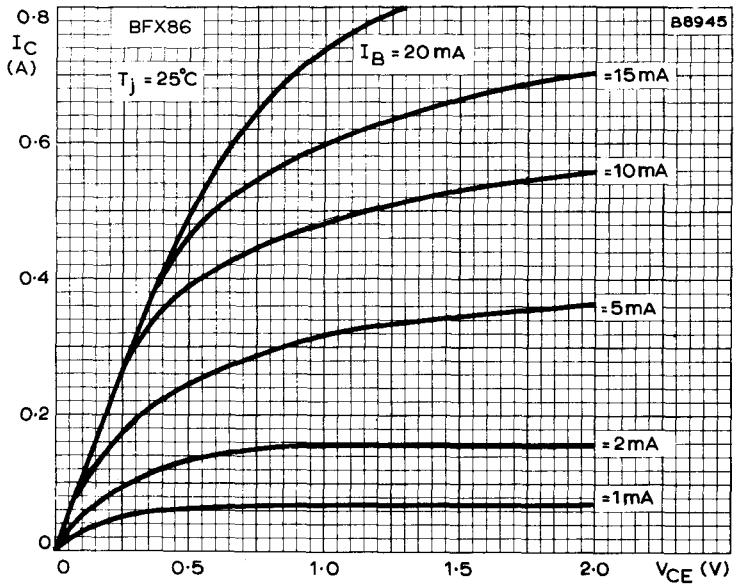


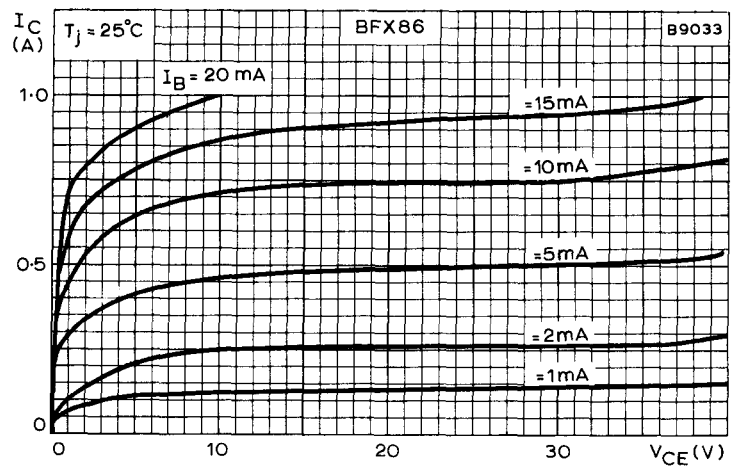
TYPICAL OUTPUT CHARACTERISTICS



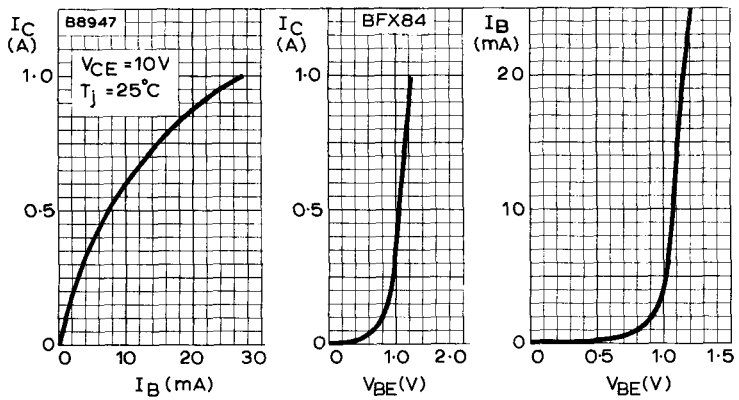


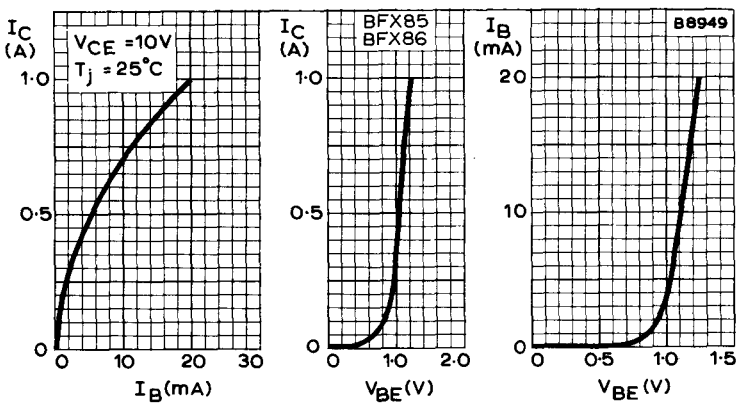
TYPICAL OUTPUT CHARACTERISTICS



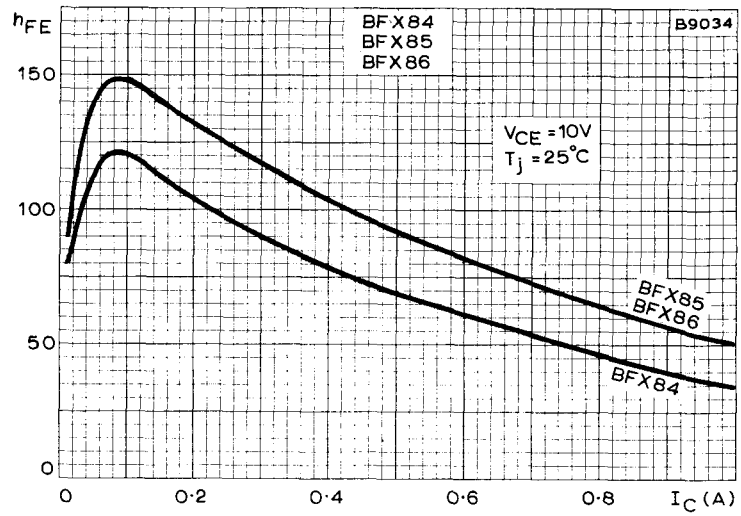


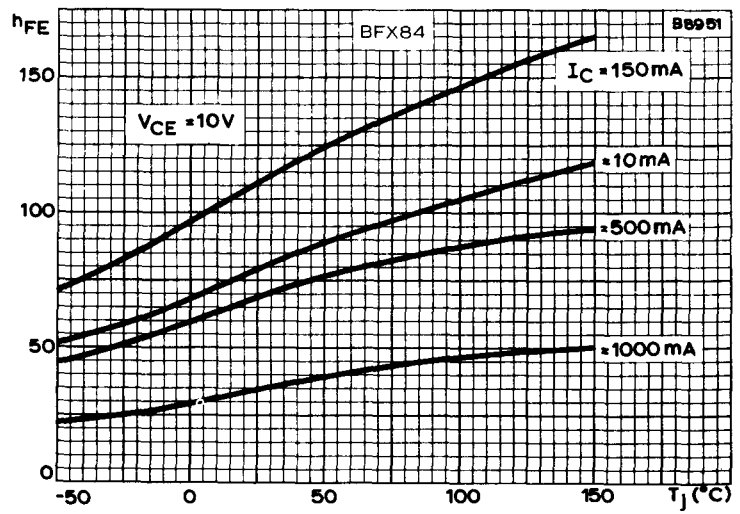
TYPICAL OUTPUT CHARACTERISTICS



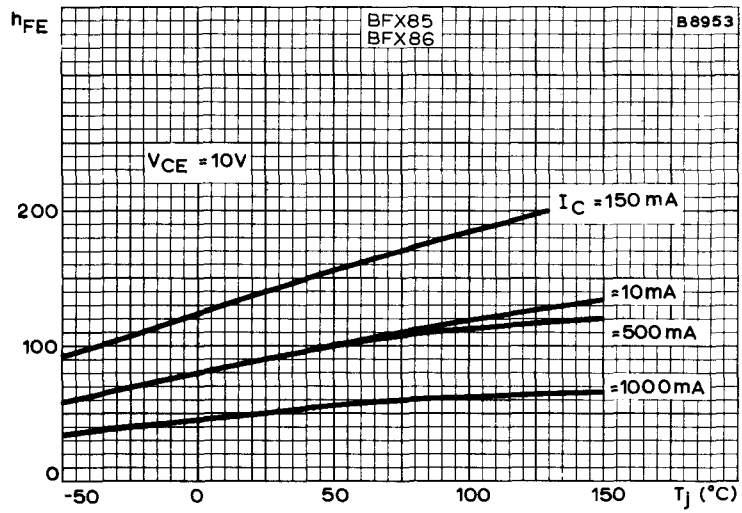


TYPICAL TRANSFER, MUTUAL AND INPUT CHARACTERISTICS

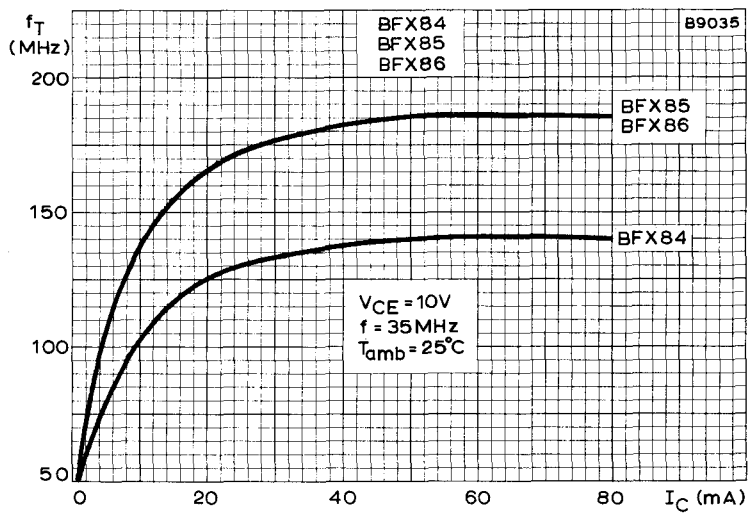




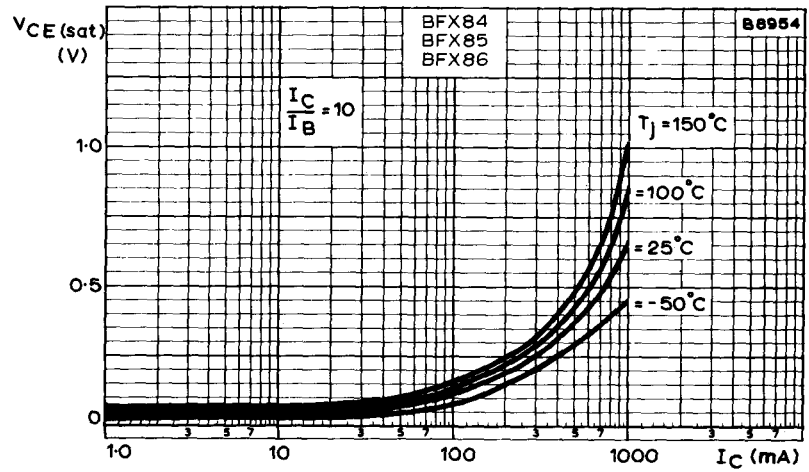
TYPICAL STATIC FORWARD CURRENT TRANSFER RATIO PLOTTED AGAINST COLLECTOR CURRENT AND JUNCTION TEMPERATURE

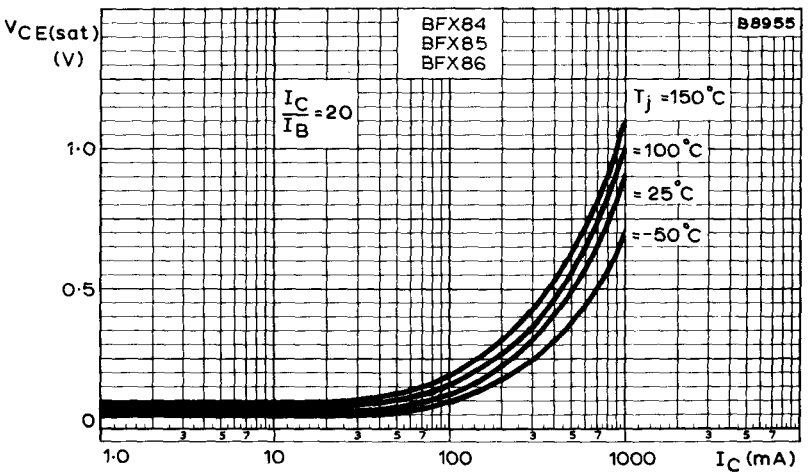


TYPICAL STATIC FORWARD CURRENT TRANSFER RATIO PLOTTED AGAINST JUNCTION TEMPERATURE

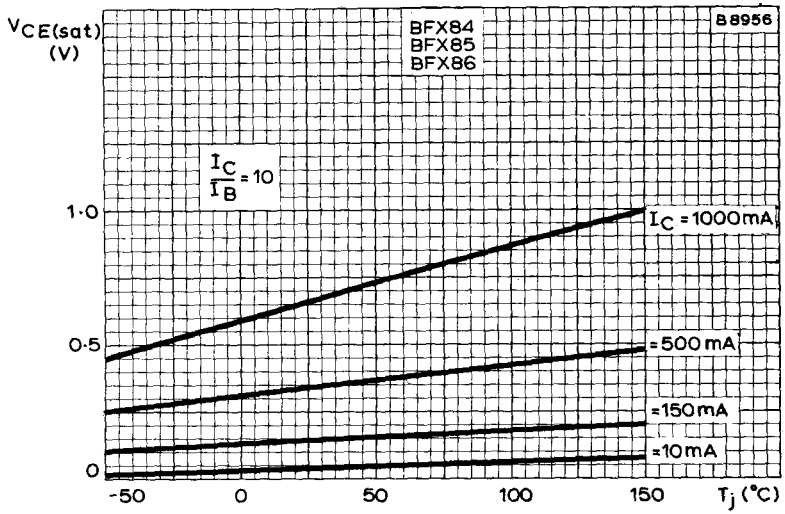


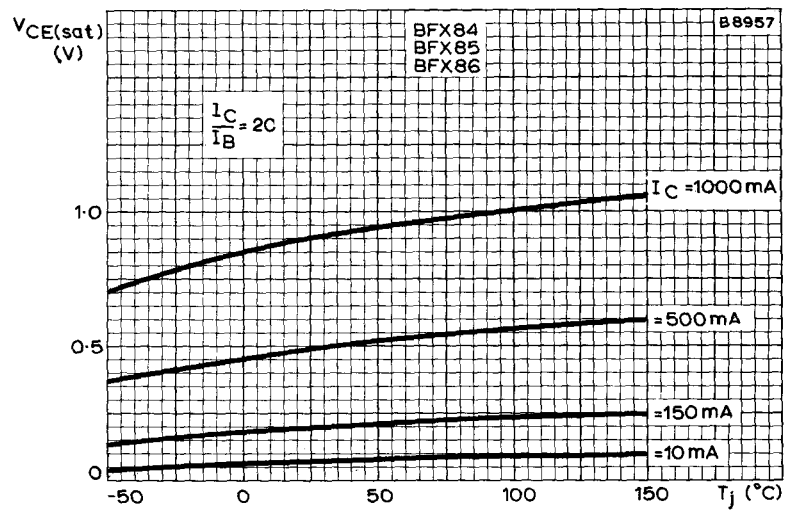
TYPICAL TRANSITION FREQUENCY PLOTTED AGAINST COLLECTOR CURRENT



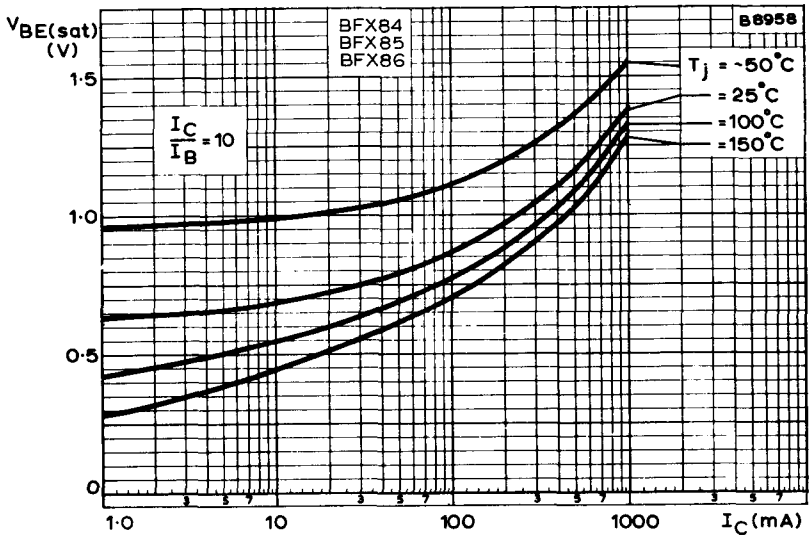


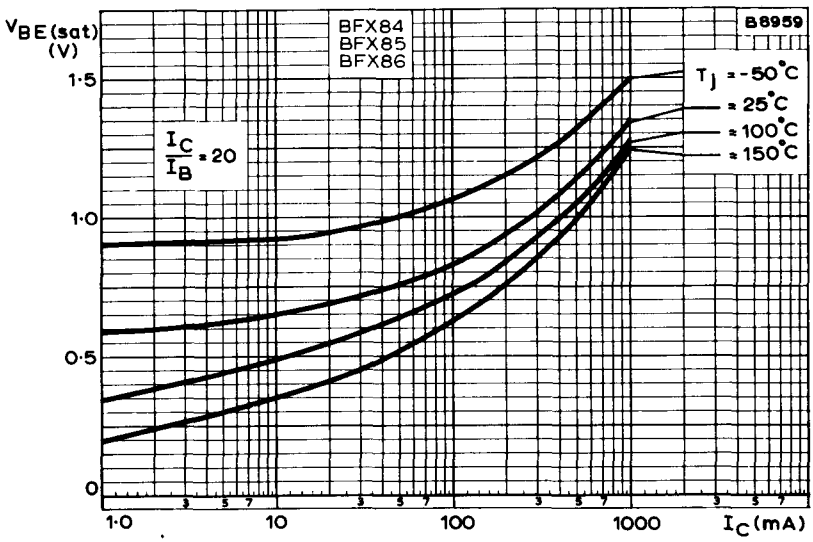
TYPICAL COLLECTOR-EMITTER SATURATION VOLTAGE
PLOTTED AGAINST COLLECTOR CURRENT



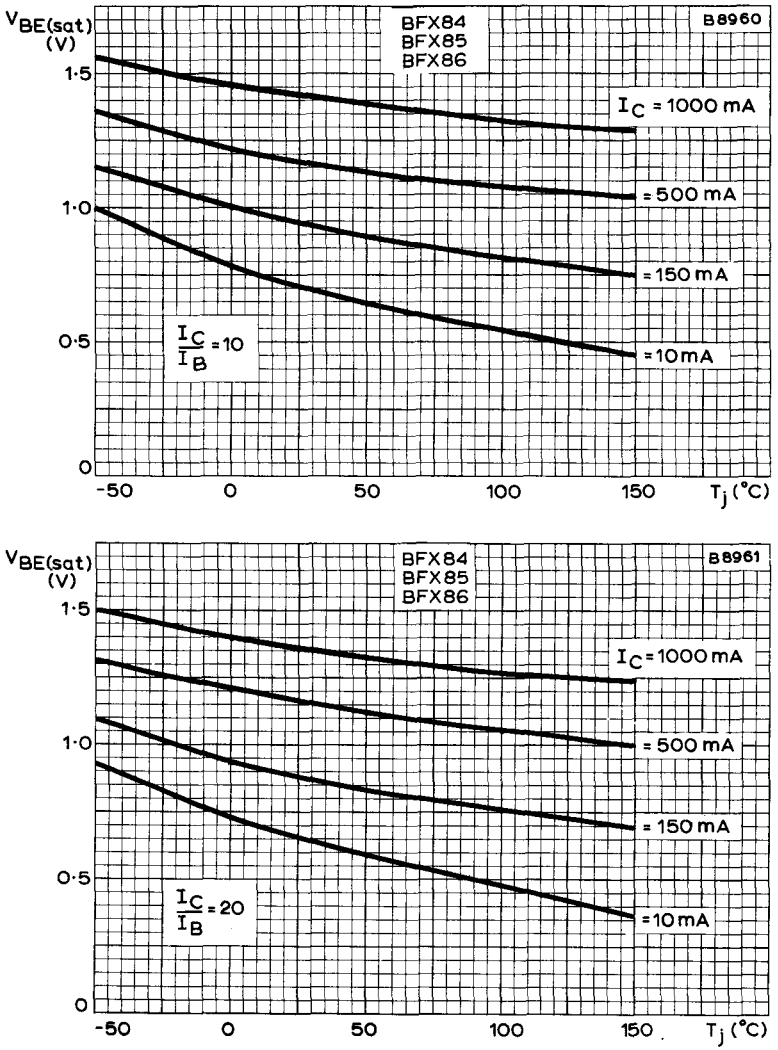


TYPICAL COLLECTOR-EMITTER SATURATION VOLTAGE
PLOTTED AGAINST JUNCTION TEMPERATURE

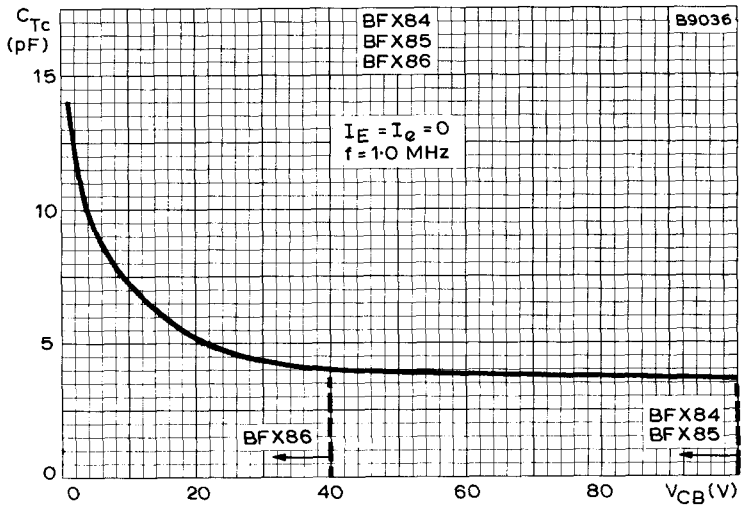




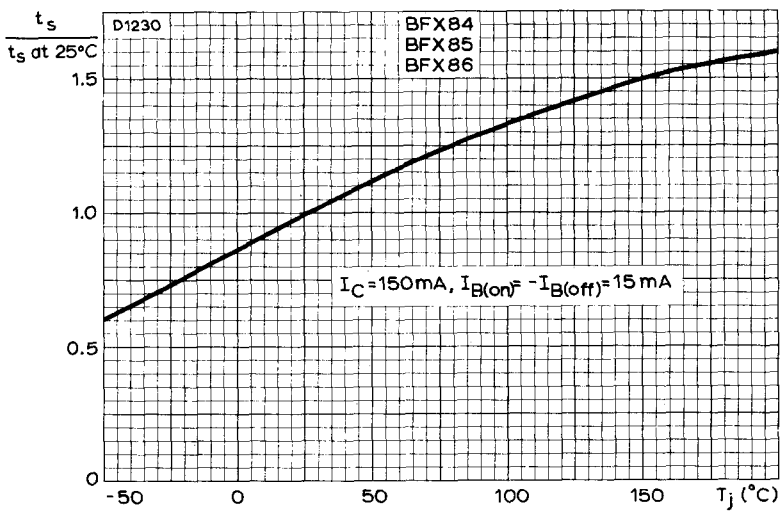
TYPICAL BASE-EMITTER SATURATION VOLTAGE
PLOTTED AGAINST COLLECTOR CURRENT



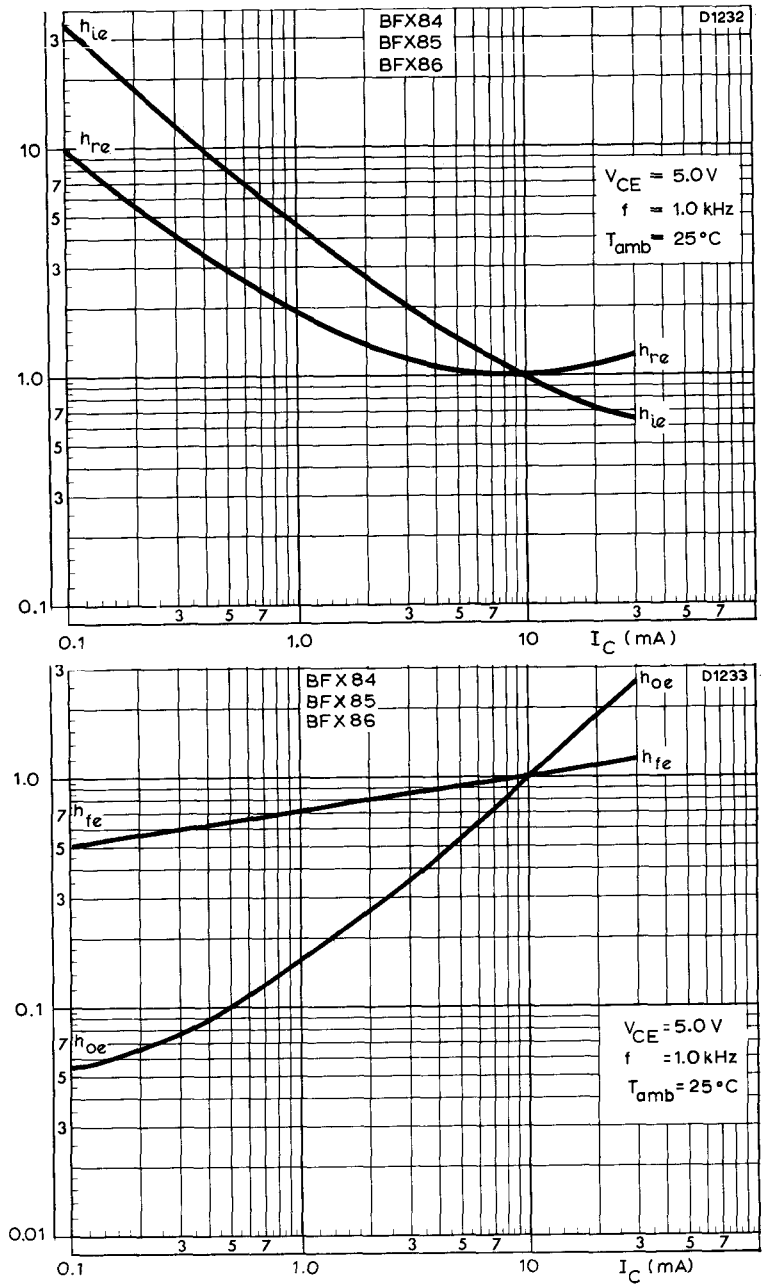
TYPICAL BASE-EMITTER SATURATION VOLTAGE
PLOTTED AGAINST JUNCTION TEMPERATURE



TYPICAL COLLECTOR CAPACITANCE PLOTTED AGAINST COLLECTOR-BASE VOLTAGE



TYPICAL STORAGE TIME NORMALISED AT 25°C



TYPICAL h-PARAMETERS NORMALISED AT I_C = 10mA

P-N-P SILICON PLANAR EPITAXIAL TRANSISTORS

BFX87
BFX88

For ratings, characteristics and mechanical details see BFX29 data sheet

N-P-N SILICON PLANAR EPITAXIAL TRANSISTOR

BFX89

N-P-N silicon planar epitaxial transistor designed for u.h.f. and v.h.f. applications. It has extremely good noise and intermodulation properties and a very high power gain and transition frequency. It is therefore particularly suitable for wideband aerial and distribution amplifiers.

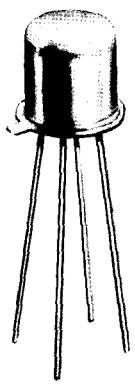
QUICK REFERENCE DATA

V_{CBOM} max. (peak)		30	V
V_{CEO} max.		15	V
I_{CM} max. (f > 1.0MHz)		50	mA
P_{tot} max. ($T_{amb} \leq 25^{o}C$)		200	mW
T_j max.		200	^{o}C
f_T typ. (I_C = 25mA, V_{CE} = 5V, f = 500MHz)		1.2	GHz
$-C_{re}$ typ. (I_C = 2mA, V_{CE} = 5V, f = 1MHz)		0.6	pF
N typ. (I_C = 2mA, V_{CE} = 10V, Z_S opt.)	f = 200MHz	3.3	dB
	f = 800MHz	7.0	dB
G_p typ. (I_C = 8mA, V_{CE} = 10V)	f = 200MHz	22	dB
	f = 800MHz	7.0	dB
P_o typ. (I_C = 8mA, V_{CE} = 10V, d_{im} = -30dB, v.s.w.r. at output < 2)	f = 200MHz	6.0	mW
	f = 800MHz	6.0	mW

OUTLINE AND DIMENSIONS

Conforms to J.E.D.E.C. TO-72
B.S. 3934 SO-12A/SB4-3

For details see page 6



Mullard

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{CBOM} max. (peak)	30	V
V_{CERM} max. (peak, $R_{BE} \leq 50\Omega$, $I_C = 10mA$)	30	V
V_{CEO} max. ($I_C = 10mA$)	15	V
V_{EBO} max.	2.5	V
I_C max. (d.c.)	25	mA
I_{CM} max. (peak, f > 1MHz)	50	mA
P_{tot} max. ($T_{amb} \leq 25^oC$)	200	mW

Temperature

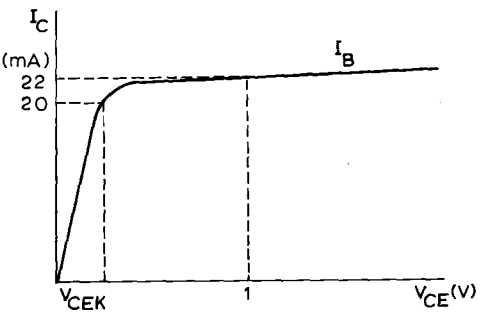
T_{stg} range	-65 to +200	^oC
T_j max.	200	^oC

THERMAL CHARACTERISTICS

$R_{th(j-amb)}$ in free air	0.88	degC/mW
$R_{th(j-case)}$	0.58	degC/mW

ELECTRICAL CHARACTERISTICS ($T_j = 25^oC$ unless otherwise stated)

		Min.	Typ.	Max.	
I_{CBO}	Collector cut-off current $I_E = 0$, $V_{CB} = 15V$	-	-	10	nA
V_{CEK}	Collector-emitter knee voltage $I_C = 20mA$, I_B = the value for $I_C = 22mA$ at $V_{CE} = 1V$	-	-	0.75	V



h_{FE}	Static forward current transfer ratio				
	$I_C = 2mA$, $V_{CE} = 1V$	25	-	150	
	$I_C = 25mA$, $V_{CE} = 1V$	20	-	125	

ELECTRICAL CHARACTERISTICS (cont'd)

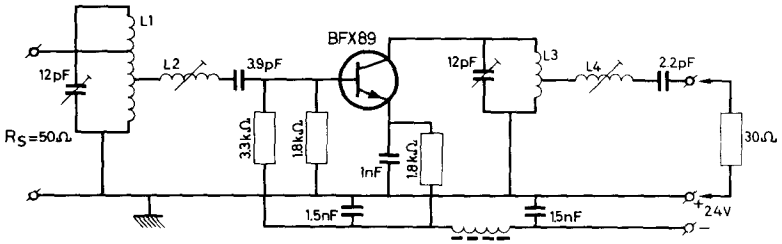
		Min.	Typ.	Max.	
f_T	*Transition frequency				
	$I_C = 2mA$, $V_{CE} = 5V$, $f = 500MHz$	-	1.0	-	GHz
	$I_C = 25mA$, $V_{CE} = 5V$, $f = 500MHz$	-	1.1	-	GHz
C_{tc}	**Collector capacitance				
	$I_E = I_e = 0$, $V_{CB} = 10V$, $f = 1MHz$	-	-	1.7	pF
$-C_{re}$	*Feedback capacitance				
	$I_C = 2mA$, $V_{CE} = 5V$, $f = 1MHz$	-	0.6	-	pF
N	*Noise figure				
	$I_C = 2mA$, $V_{CE} = 5V$,				
	$f = 200MHz$, $Z_S = opt.$	-	-	4.0	dB
	$f = 500MHz$, $R_S = 50\Omega$	-	-	6.5	dB
	$f = 800MHz$, $Z_S = opt.$	-	7.0	-	dB
G_p	*Power gain (not neutralised)				
	$I_C = 8mA$, $V_{CE} = 10V$, $f = 200MHz$	19	22	-	dB
	$f = 800MHz$	-	7.0	-	dB

*Fourth lead (case) grounded.
**Fourth lead (case) not connected.

Intermodulation characteristics

P_o	*Output power (see test circuits 1 and 2)				
	$I_C = 8mA$, $V_{CE} = 10V$, v.s.w.r. at output < 2,				
	$d_{im} = -30dB$				
	$f = 200MHz$, $f_p = 202MHz$, $f_q = 205MHz$,				
	$f_{(2q-p)} = 208MHz$ (channel 9)	-	6.0	-	mW
	$f = 800MHz$, $f_p = 798MHz$, $f_q = 802MHz$,				
	$f_{(2q-p)} = 806MHz$ (channel 62)	-	6.0	-	mW
d_{im}	Intermodulation distortion (see test circuit 3)				
	$I_C = 8mA$, $V_{CE} = 6V$, $R_L = 37.5\Omega$,				
	$V_o = 100mV$ at $f_p = 183MHz$				
	$V_o = 100mV$ at $f_q = 200MHz$				
	$f_{(2q-p)} = 217MHz$	-	-40	-	dB

TEST CIRCUIT 1 - OUTPUT POWER TEST CIRCUIT (f=200MHz)



L1 = 3 turns of 1.4mm silver plated copper wire, winding pitch 2.7mm, int. dia. 8mm, taps 1.5 and 0.5 turns from earth.
L2 = 5.5 turns of 1.4mm silver plated copper wire, winding pitch 2.2mm, int. dia. 8mm.
L3 = 3 turns of 1.4mm silver plated copper wire, winding pitch 3.3mm, int. dia. 8mm.
L4 = 5.5 turns of 1.4mm silver plated copper wire, winding pitch 2.2mm, int. dia. 11mm.

ADJUSTMENT OF TEST CIRCUIT

Technical considerations

Intermodulation distortion is caused by clipping in h.f. output current and voltage.
The maximum undistorted output power is attained when

a) Clipping in current and voltage is simultaneous; this occurs if

$$R_{load} = (V_{CE} - V_{cek})/I_C$$

Where V_{cek} is the high frequency knee voltage

b) The h.f. collector current is as low as possible; this occurs if

$$-C_{load} = +C_{oe}$$

Where C_{oe} is the output capacitance of the transistor with short-circuited input.

Experimentally obtained values of R_{load} and C_{load}, for maximum output power at an intermodulation factor of -30dB, are:

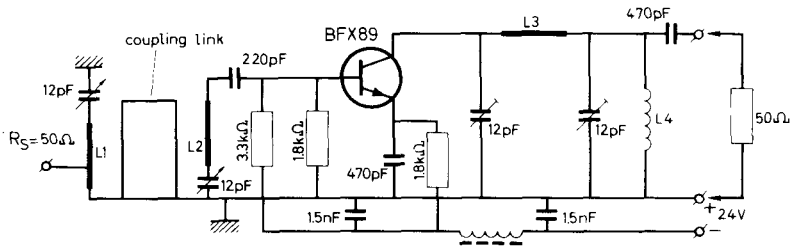
$$R_{load} = 1k\Omega,\ C_{load} = -1.8pF$$

Procedure

1. Remove the transistor and connect a dummy, consisting of a 220Ω resistor in parallel with a 5.6pF capacitor, between the collector and the emitter connections of the output circuit.
2. Tune and match the output circuit for zero reflection at 205MHz (i.e. v.s.w.r. = 1). After this adjustment no further change should be made in the output circuit.
3. Replace the dummy by the transistor. Tune and match the input circuit for maximum power gain and good bandpass curve. The v.s.w.r. of the output will then be ≤2 over most of the channel. Corrections can be made by tuning L2.

ELECTRICAL CHARACTERISTICS (cont'd)

TEST CIRCUIT 2 - OUTPUT POWER TEST CIRCUIT (f = 800MHz)



L1 = 24×6×0.5mm silver plated copper strip, input tap at 5mm from earth.
L2 = 15×6×0.5mm silver plated copper strip.
L3 = 20×8×0.5mm silver plated copper strip.
L4 = 4 turns of 0.5mm enamelled copper wire, winding pitch 1.5mm, int. dia. 4mm.
Coupling link = 42mm of 1mm silver plated copper wire.

ADJUSTMENT OF TEST CIRCUIT

At 800MHz a dummy cannot be used to adjust for optimum collector load, because at these frequencies the impedance transformations of the dummy are too high.
A small signal with a frequency of the midchannel 802MHz is fed to the input. The signal is increased until clipping occurs, that is until the output power no longer increases linearly with increasing input signal. Care should be taken not to allow the voltage swing to exceed the V_{CER} value as this may result in the destruction of the transistor by second breakdown.
The output circuit is then tuned to eliminate clipping.

The output power P_o is given by

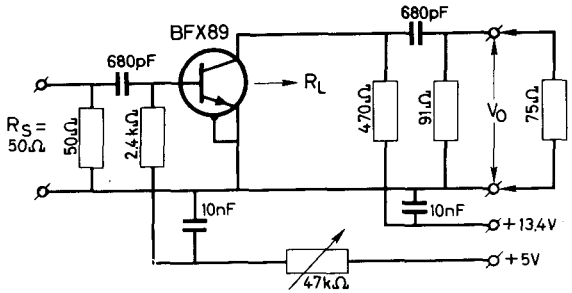
$$P_o = I_C(V_{CE} - V_{cek}) / 2 = 35mW$$

Where V_{cek} is the high frequency knee voltage

Keeping the input signal as small as possible at P_o = 35mW, the output circuit is adjusted for minimum intermodulation. The input circuit is then adjusted for maximum gain and good bandpass curve. The v.s.w.r. is found to be ≤2 over the whole channel.

ELECTRICAL CHARACTERISTICS (cont'd)

TEST CIRCUIT 3 - INTERMODULATION DISTORTION TEST CIRCUIT

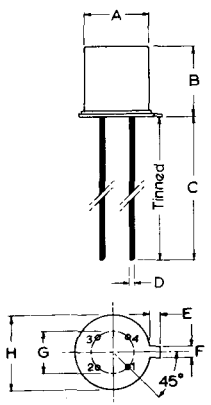


SOLDERING AND WIRING RECOMMENDATIONS

1. When using a soldering iron, transistors may be soldered directly into the circuit, but heat conducted to the junction should if possible be kept to a minimum by the use of a thermal shunt.
2. Transistors may be dip-soldered at a solder temperature of 245°C for a maximum soldering time of 5 seconds. The case temperature during soldering must not at any time exceed the maximum storage temperature. These recommendations apply to a transistor mounted flush on a board having punched-through holes, or spaced at least 1.5mm above a board having plated-through holes.
3. Care should be taken not to bend the leads nearer than 1.5mm from the seal.
4. If devices are stored at temperatures above 100°C before incorporation into equipment, some deterioration of the external surface is likely to occur which may make soldering into the circuit difficult. Under these circumstances the leads should be retinned using a suitable activated flux.

OUTLINE, DIMENSIONS AND CONNECTIONS

Conforms to J.E.D.E.C. TO-72

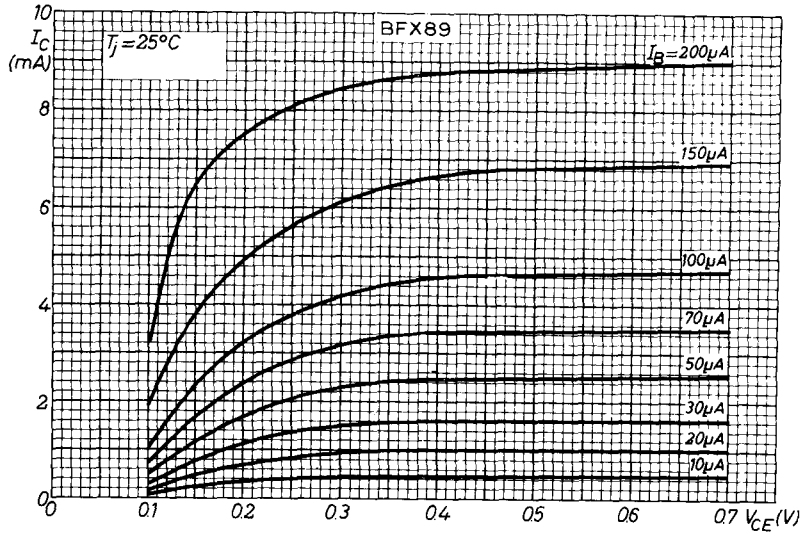


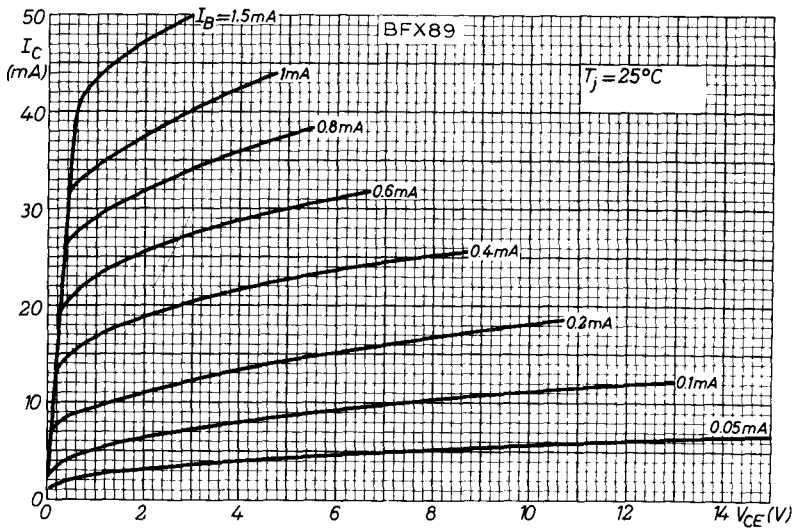
Viewed from underside

	Millimetres		
	Min.	Nom.	Max.
A	-	-	4.8
B	-	-	5.3
C	12.7	-	-
D	-	0.43	-
E	-	1.0	-
F	-	1.05	-
G	-	2.54	-
H	5.3	5.55	5.8

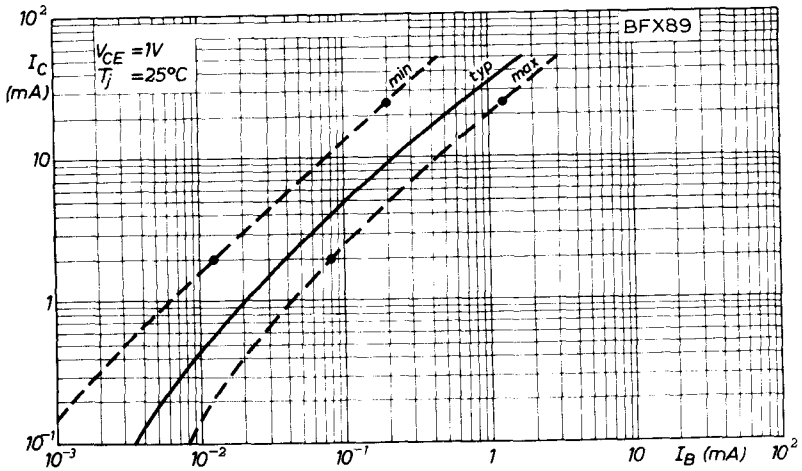
Connections

1. Emitter
2. Base
3. Collector
4. Shield connected to envelope

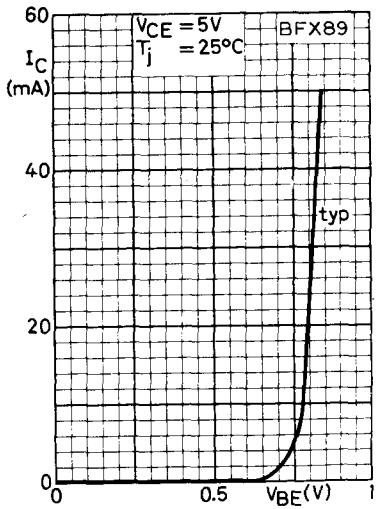




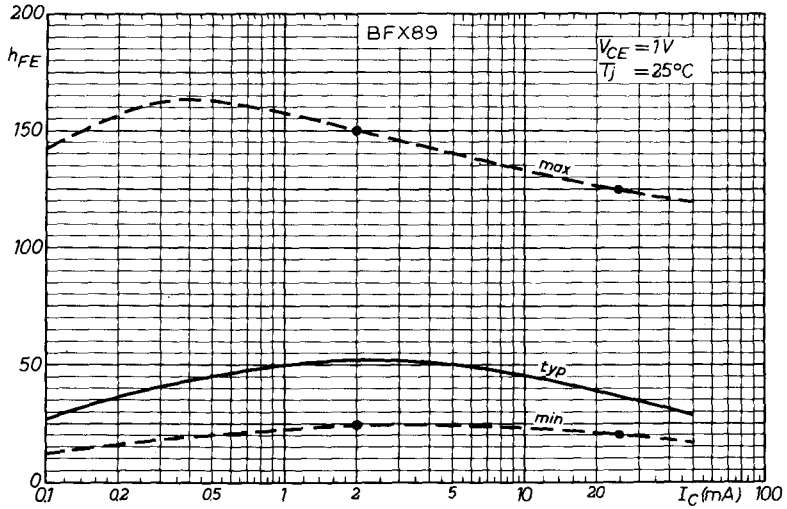
TYPICAL OUTPUT CHARACTERISTICS AT LOW AND HIGH COLLECTOR-EMITTER VOLTAGES



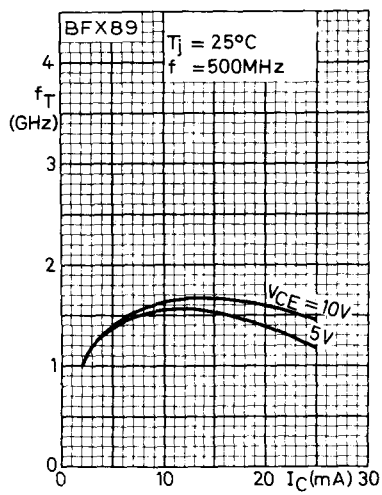
TRANSFER CHARACTERISTICS



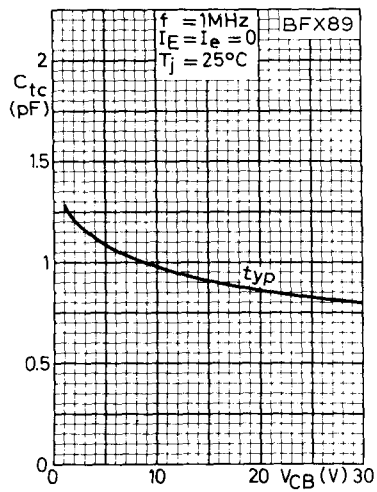
TYPICAL MUTUAL CHARACTERISTICS



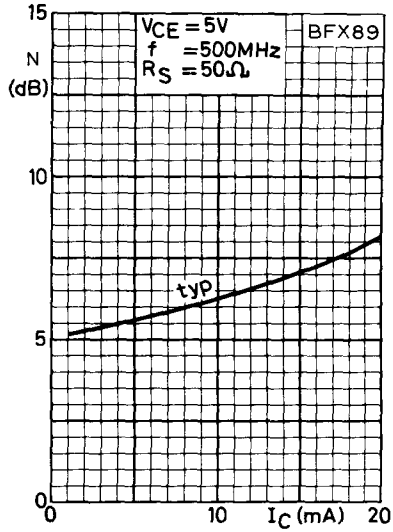
STATIC FORWARD CURRENT TRANSFER RATIO
PLOTTED AGAINST COLLECTOR CURRENT



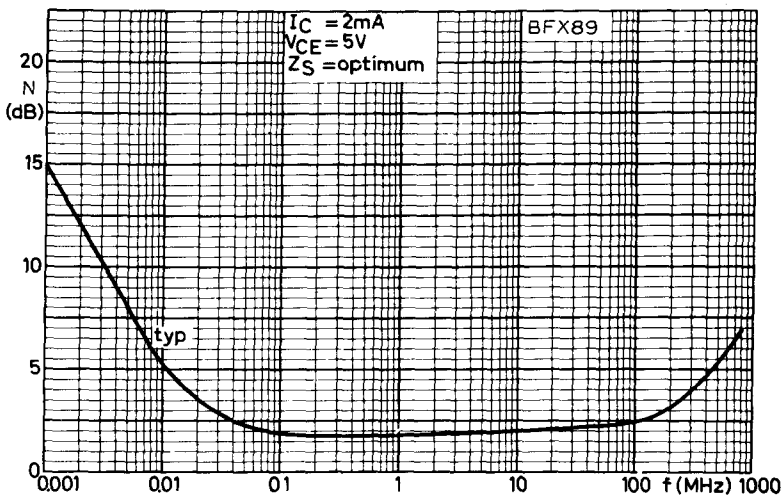
Typical transition frequency versus collector current



Typical collector capacitance versus collector-base voltage



TYPICAL NOISE FIGURE PLOTTED AGAINST COLLECTOR CURRENT



TYPICAL NOISE FIGURE PLOTTED AGAINST FREQUENCY

N-P-N SILICON PLANAR EPITAXIAL TRANSISTORS

BFY50
BFY51
BFY52

Also available to BS9365—F012

Silicon n-p-n planar epitaxial transistors for general purpose industrial applications. Encapsulated in TO-5 envelope with the collector connected to can.

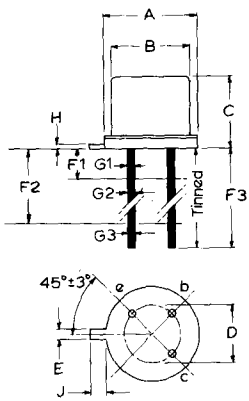
QUICK REFERENCE DATA

	BFY50	BFY51	BFY52	
V_{CBO} max.	80	60	40	V
V_{CEO} max.	35	30	20	V
I_{CM} max.	1.0	1.0	1.0	A
P_{tot} max. $T_{amb} \leq 25^{o}C$	800	800	800	mW
$T_{case} \leq 100^{o}C$	2.86	2.86	2.86	W
h_{FE} (I_C = 150mA, V_{CE} = 10V) min.	30	40	60	
typ.	112	123	142	
f_T min. (I_C = 50mA, V_{CE} = 10V, f = 35MHz, T_{amb} = 25°C)	50	50	50	MHz

Unless otherwise stated data is applicable to all types

OUTLINE AND DIMENSIONS

Conforms to B.S. 3934 SO-3/SB3-3A
J.E.D.E.C. TO-5



The collector is electrically connected to the envelope

	Millimetres		
	Min.	Nom.	Max.
A	9.10	-	9.40
B	8.20	-	8.50
C	6.10	-	6.60
D	-	5.08	-
E	0.71	-	0.86
F1	-	-	0.51
F2	12.7	-	-
F3	38.1	-	41.3
G1	-	-	1.01
G2	0.41	-	0.48
G3	-	-	0.53
H	-	0.4	-
J	0.74	-	1.0

ELECTRICAL CHARACTERISTICS (contd.)

		Min.	Typ.	Max.	
f_T	Transition frequency $I_C = 50mA$, $V_{CE} = 10V$, $f = 35MHz$, $T_{amb} = 25^oC$	60	140	-	MHz
Saturated switching times $I_C = 150mA$, $I_{B(on)} = -I_{B(off)} = 15mA$, $-V_{EE} = 10V$, $-V_{BE(off)} = 2.0V$					
t_d	Delay time	-	15	-	ns
t_r	Rise time	-	40	-	ns
t_{on}	Turn-on time	-	55	-	ns
t_s	Storage time	-	300	-	ns
t_f	Fall time	-	60	-	ns
t_{off}	Turn-off time	-	360	-	ns
h-parameters					
h_{fe}	$I_C = 1.0mA$, $V_{CE} = 5.0V$, $f = 1.0kHz$, $T_{amb} = 25^oC$	10	65	-	
h_{ie}	$I_C = 10mA$, $V_{CE} = 5.0V$, $f = 1.0kHz$, $T_{amb} = 25^oC$	-	250	750	Ω
h_{re}		-	0.85	5.0	$\times 10^{-4}$
h_{fe}		15	80	-	
h_{oe}		-	35	80	μmho

BFY51

ELECTRICAL CHARACTERISTICS ($T_j = 25^oC$ unless otherwise stated)

		Min.	Typ.	Max.	
I_{CBO}	Collector cut-off current				
	$V_{CB} = 60V$, $I_E = 0$	-	10	500	nA
	$V_{CB} = 60V$, $I_E = 0$, $T_j = 100^oC$	-	0.5	30	μA
	$V_{CB} = 40V$, $I_E = 0$	-	2.0	50	nA
	$V_{CB} = 40V$, $I_E = 0$, $T_j = 100^oC$	-	0.1	2.5	μA
I_{EBO}	Emitter cut-off current				
	$V_{EB} = 6.0V$, $I_C = 0$	-	10	500	nA
	$V_{EB} = 5.0V$, $I_C = 0$	-	2.0	50	nA
	$V_{EB} = 5.0V$, $I_C = 0$, $T_j = 100^oC$	-	0.1	2.5	μA
h_{FE}	Static forward current transfer ratio				
	$I_C = 10mA$, $V_{CE} = 10V$	30	85	-	
	$I_C = 150mA$, $V_{CE} = 10V$	40	123	-	
	$I_C = 500mA$, $V_{CE} = 10V$	25	79	-	
	$I_C = 1.0A$, $V_{CE} = 10V$	15	40	-	
$V_{CE(sat)}$	Collector-emitter saturation voltage				
	$I_C = 10mA$, $I_B = 1.0mA$	-	0.06	0.15	V
	$I_C = 150mA$, $I_B = 15mA$	-	0.15	0.35	V
	$I_C = 500mA$, $I_B = 50mA$	-	0.35	1.00	V
	$I_C = 1.0A$, $I_B = 100mA$	-	0.66	1.60	V
$V_{BE(sat)}$	Base-emitter saturation voltage				
	$I_C = 10mA$, $I_B = 1.0mA$	-	0.69	1.2	V
	$I_C = 150mA$, $I_B = 15mA$	-	0.92	1.3	V
	$I_C = 500mA$, $I_B = 50mA$	-	1.15	1.5	V
	$I_C = 1.0A$, $I_B = 100mA$	-	1.40	2.0	V
C_{Tc}	Collector capacitance $V_{CB} = 10V$, $I_E = I_e = 0$, $f = 1.0MHz$	-	7.0	12	pF

ELECTRICAL CHARACTERISTICS (contd.)

		Min.	Typ.	Max.	
f_T	Transition frequency $I_C = 50mA$, $V_{CE} = 10V$, $f = 35MHz$, $T_{amb} = 25^oC$	50	160	-	MHz
Saturated switching times $I_C = 150mA$, $I_{B(on)} = -I_{B(off)} = 15mA$, $-V_{EE} = 10V$, $-V_{BE(off)} = 2.0V$					
t_d	Delay time	-	15	-	ns
t_r	Rise time	-	40	-	ns
t_{on}	Turn-on time	-	55	-	ns
t_s	Storage time	-	300	-	ns
t_f	Fall time	-	60	-	ns
t_{off}	Turn-off time	-	360	-	ns
h-parameters					
h_{fe}	$I_C = 1.0mA$, $V_{CE} = 5.0V$, $f = 1.0kHz$, $T_{amb} = 25^oC$	20	65	-	
h_{ie}	$I_C = 10mA$, $V_{CE} = 5.0V$, $f = 1.0kHz$, $T_{amb} = 25^oC$	-	250	750	Ω
h_{re}		-	0.85	5.0	$\times 10^{-4}$
h_{fe}		25	80	-	
h_{oe}		-	35	80	μmho

BFY52

ELECTRICAL CHARACTERISTICS ($T_j = 25^oC$ unless otherwise stated)

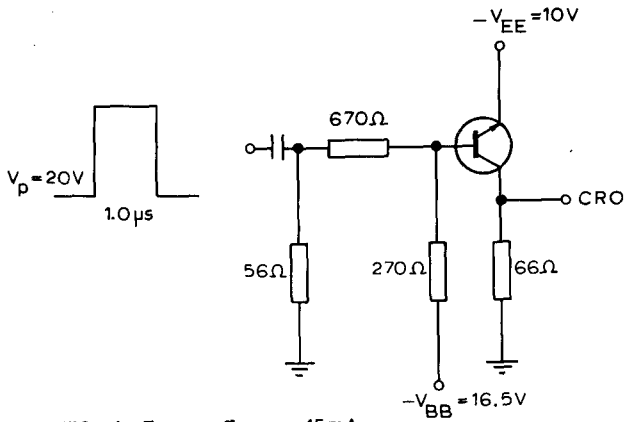
		Min.	Typ.	Max.	
I_{CBO}	Collector cut-off current				
	$V_{CB} = 40V$, $I_E = 0$	-	10	500	nA
	$V_{CB} = 40V$, $I_E = 0$, $T_j = 100^oC$	-	0.5	30	μA
	$V_{CB} = 30V$, $I_E = 0$	-	2.0	50	nA
	$V_{CB} = 30V$, $I_E = 0$, $T_j = 100^oC$	-	0.1	2.5	μA
I_{EBO}	Emitter cut-off current				
	$V_{EB} = 6.0V$, $I_C = 0$	-	10	500	nA
	$V_{EB} = 5.0V$, $I_C = 0$	-	2.0	50	nA
	$V_{EB} = 5.0V$, $I_C = 0$, $T_j = 100^oC$	-	0.1	2.5	μA
h_{FE}	Static forward current transfer ratio				
	$I_C = 10mA$, $V_{CE} = 10V$	30	90	-	
	$I_C = 150mA$, $V_{CE} = 10V$	60	142	-	
	$I_C = 500mA$, $V_{CE} = 10V$	30	90	-	
	$I_C = 1.0A$, $V_{CE} = 10V$	15	50	-	
$V_{CE(sat)}$	Collector-emitter saturation voltage				
	$I_C = 10mA$, $I_B = 1.0mA$	-	0.06	0.15	V
	$I_C = 150mA$, $I_B = 15mA$	-	0.15	0.35	V
	$I_C = 500mA$, $I_B = 50mA$	-	0.35	1.00	V
	$I_C = 1.0A$, $I_B = 100mA$	-	0.66	1.60	V
$V_{BE(sat)}$	Base-emitter saturation voltage				
	$I_C = 10mA$, $I_B = 1.0mA$	-	0.69	1.2	V
	$I_C = 150mA$, $I_B = 15mA$	-	0.92	1.3	V
	$I_C = 500mA$, $I_B = 50mA$	-	1.15	1.5	V
	$I_C = 1.0A$, $I_B = 100mA$	-	1.40	2.0	V
C_{Tc}	Collector capacitance $V_{CB} = 10V$, $I_E = I_e = 0$, $f = 1.0MHz$	-	7.0	12	pF

ELECTRICAL CHARACTERISTICS (contd.)

		Min.	Typ.	Max.	
f_T	Transition frequency $I_C = 50mA$, $V_{CE} = 10V$, $f = 35MHz$, $T_{amb} = 25^oC$	50	185	-	MHz
	Saturated switching times $I_C = 150mA$, $I_{B(on)} = -I_{B(off)} = 15mA$, $-V_{EE} = 10V$, $-V_{BE(off)} = 2.0V$				
t_d	Delay time	-	15	-	ns
t_r	Rise time	-	40	-	ns
t_{on}	Turn-on time	-	55	-	ns
t_s	Storage time	-	300	-	ns
t_f	Fall time	-	60	-	ns
t_{off}	Turn-off time	-	360	-	ns
	h-parameters				
h_{fe}	$I_C = 1.0mA$, $V_{CE} = 5.0V$, $f = 1.0kHz$, $T_{amb} = 25^oC$	20	65	-	
h_{ie}	$I_C = 10mA$, $V_{CE} = 5.0V$, $f = 1.0kHz$, $T_{amb} = 25^oC$	-	250	750	Ω
h_{re}		-	0.85	5.0	$\times 10^{-4}$
h_{fe}		25	80	-	
h_{oe}		-	35	80	μmho

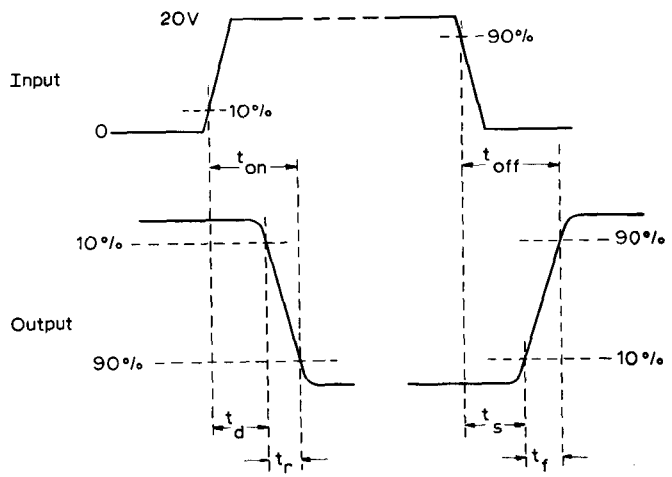
MEASUREMENT OF SATURATED SWITCHING TIMES

Test circuit



I_C = 150mA, $I_{B(on)} = -I_{B(off)}$ = 15mA
$-V_{BE(off)}$ = 2.0 V

Switching waveforms



OPERATING NOTES

1. Dissipation and heatsink considerations

a) Steady-state conditions

The maximum steady-state dissipation P_s is given by the relationship:

$$P_{s\ max.} = \frac{T_{j\ max.} - T_{amb}}{R_{th(j\text{-}amb)}}$$

Where $T_{j\ max.}$ is the maximum permissible operating junction temperature,
T_{amb} is the ambient temperature,
$R_{th(j\text{-}amb)}$ is the total thermal resistance between junction and ambient.

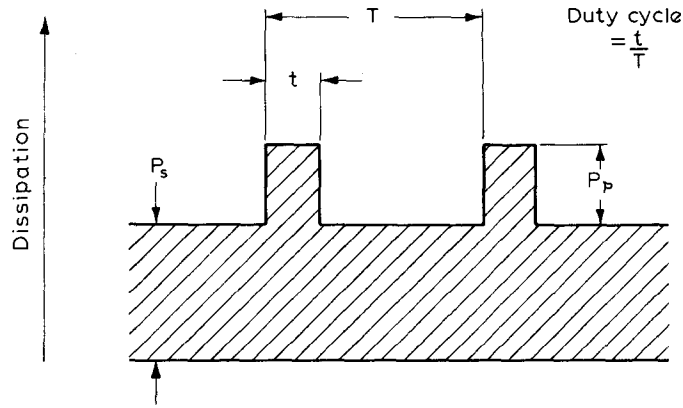
Page 13 gives the maximum allowable steady-state dissipation versus ambient temperature for the device mounted in free air and with infinite heatsink.

b) Pulse conditions (rectangular pulses)

The maximum pulse power P_p is given by the formula

$$P_p = \frac{(T_{j\ max.} - T_{amb}) - (P_s . R_{th(j\text{-}amb)})}{R_{th(t)} + d . R_{th(case\text{-}amb)}}$$

Where P_s is the steady-state dissipation excluding that in the pulses,
$R_{th(t)}$ is effective transient thermal resistance of the device between junction and case, and is a function of the pulse duration t, and duty cycle d,
d is the duty cycle, and is equal to the pulse duration t divided by the periodic time T,
$R_{th(case\text{-}amb)}$ is the total thermal resistance between case and ambient and is equal to the difference between $R_{th(j\text{-}amb)}$ and the thermal resistance from junction to case $R_{th(j\text{-}case)}$.



b) Pulse conditions (rectangular pulses) (cont'd)

Example

The following example shows how to calculate the maximum permissible peak dissipation of a BFY50 mounted in free air at a temperature not exceeding 65°C. The steady-state dissipation under the bottomed condition is 350mW, the pulse width is 1ms and the duty cycle is 0.2.

The transient thermal resistance $R_{th(t)} = 15.5$degC/W (page 13)

$$P_p \text{ max.} = \frac{(200-65) - (0.35\times220)}{15.5+0.2(220-35)}$$

$$= \frac{135-77}{15.5+37}$$

$$= 1.1\text{W}$$

The peak pulse dissipation of 1.1W is therefore allowed provided that the voltage and current ratings of the device are not exceeded.

c) Pulse conditions (other than rectangular)

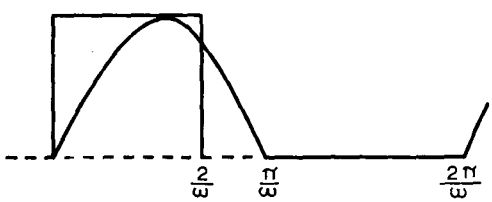
For sinusoidal and irregular shaped waveforms, the power pulse is converted to an equivalent rectangular pulse of the same average and peak values, and treated as in the previous section.

Example

The following example illustrates how to find the maximum permissible peak dissipation of a BFY52 operating in a class 'B' circuit at 1kHz. The device is mounted on a heatsink of thermal resistance equal to 50degC/W and at an ambient temperature not exceeding 100°C. Assuming that the waveform is sinusoidal for half period and zero for the other half.

Average of sinewave over half cycle = $2P_p/\pi$

Therefore equivalent rectangular pulse width of same amplitude and average value



B3559

$$t = \frac{2}{\omega}$$

$$= \frac{2}{2\pi\times10^3}$$

$$= 0.318\text{ms}$$

Duty cycle, $d = \frac{1}{\pi}$

c) Pulse conditions (other than rectangular) (cont'd)

$$\text{Duty cycle, } d = \frac{2}{\omega} \Big/ \frac{2\pi}{\omega} = \frac{1}{\pi} = 0.318$$

From page 13

$$R_{th(t)} = 6.8\text{degC/W } (d=0)$$

$$R_{th(s)} = 35\text{degC/W}$$

$$R_{th(t)} \text{ at } d=0.318 = (35-6.8) \times 0.318+6.8$$

$$= 15.8\text{degC/W}$$

$$P_p \text{ max.} = \frac{(200 - 100) - 0}{15.8+0.318\times50}$$

$$= \frac{100}{31.7} = 3.15\text{W}$$

A peak power of 3.15W is therefore permissible provided that the voltage and current ratings of the device are not exceeded.

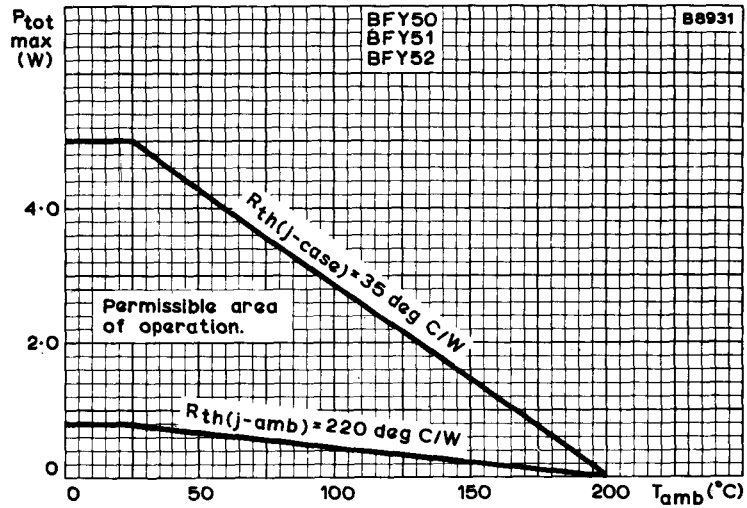
SOLDERING AND WIRING RECOMMENDATIONS

1. When using a soldering iron, transistors may be soldered directly into the circuit, but heat conducted to the junction should if possible be kept to a minimum by the use of a thermal shunt.

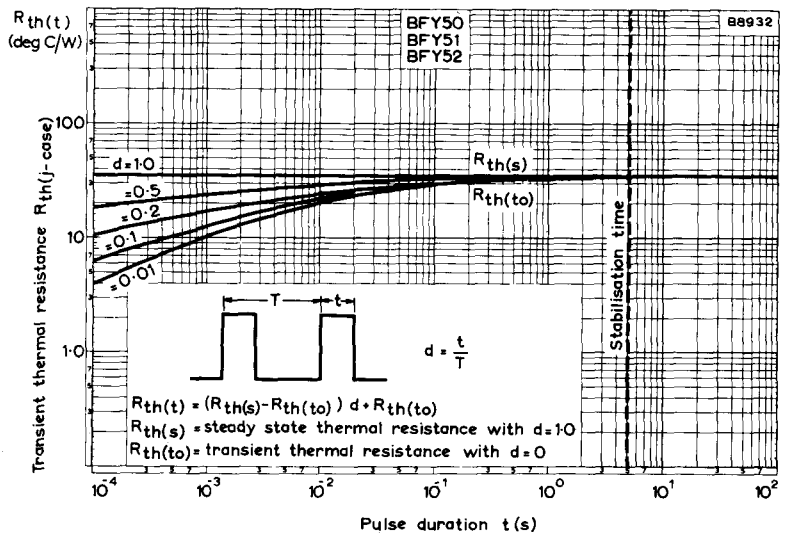
2. Transistors may be dip-soldered at a solder temperature of 245°C for a maximum soldering time of 5 seconds. The case temperature during soldering must not at any time exceed the maximum storage temperature. These recommendations apply to a transistor mounted flush on a board having punched-through holes, or spaced at least 1.5mm above a board having plated-through holes.

3. Care should be taken not to bend the leads nearer than 1.5mm from the seal.

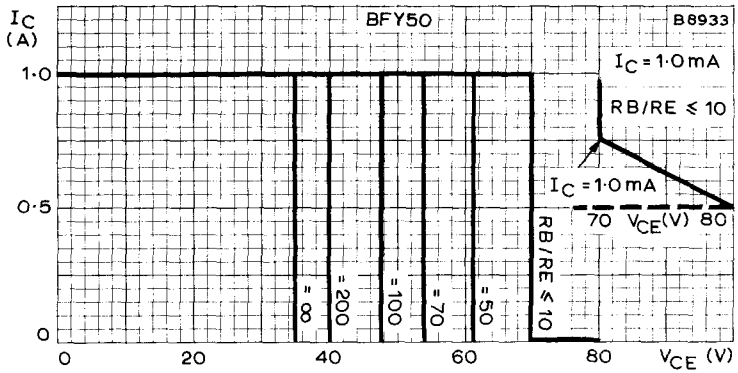
4. If devices are stored at temperatures above 100°C before incorporation into equipment, some deterioration of the external surface is likely to occur which may make soldering into the circuit difficult. Under these circumstances the leads should be retinned using a suitable activated flux.

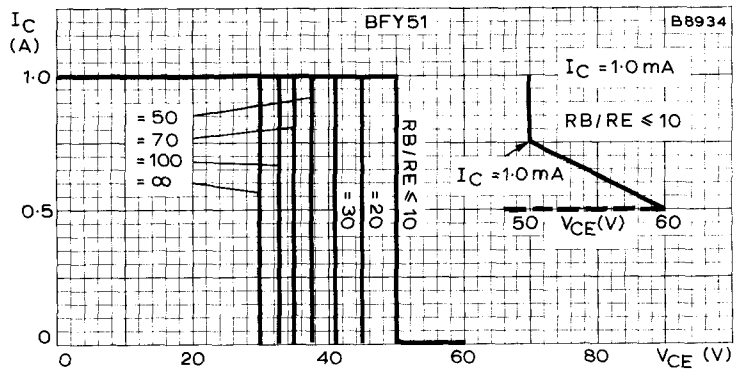


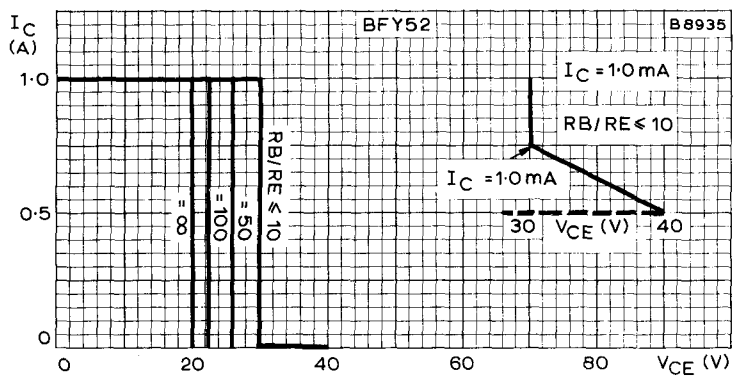
MAXIMUM TOTAL DISSIPATION PLOTTED AGAINST AMBIENT TEMPERATURE



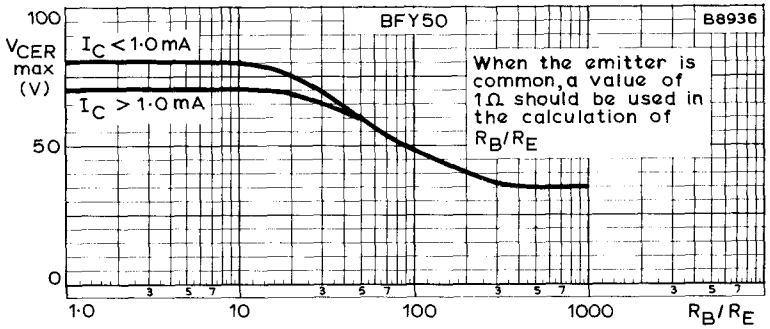
TRANSIENT THERMAL RESISTANCE FOR VARIOUS DUTY FACTORS PLOTTED AGAINST PULSE DURATION

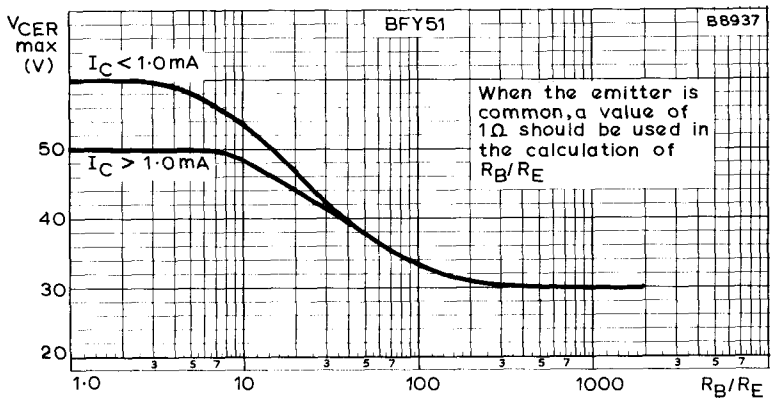


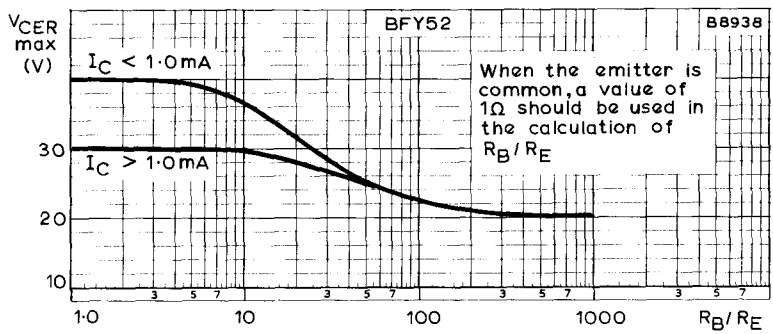




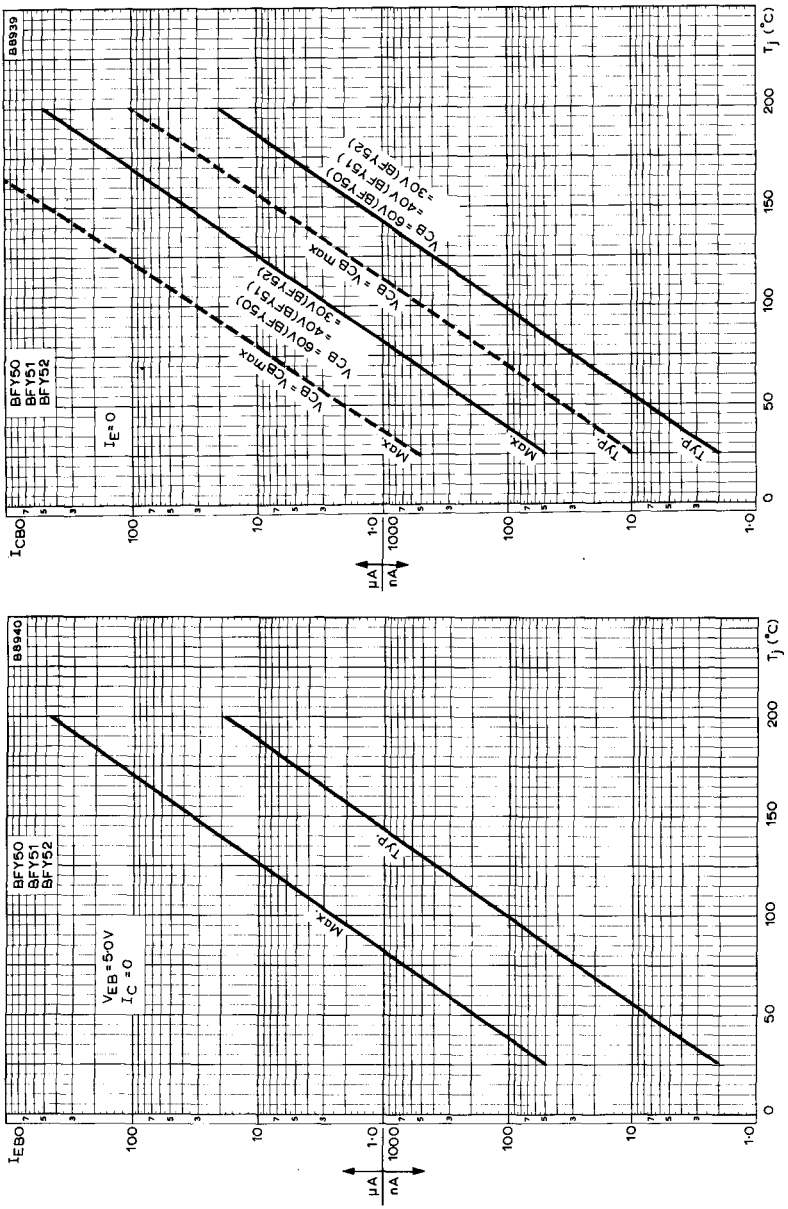
COLLECTOR CURRENT PLOTTED AGAINST MAXIMUM COLLECTOR-EMITTER VOLTAGE WITH R_B/R_E AS PARAMETER



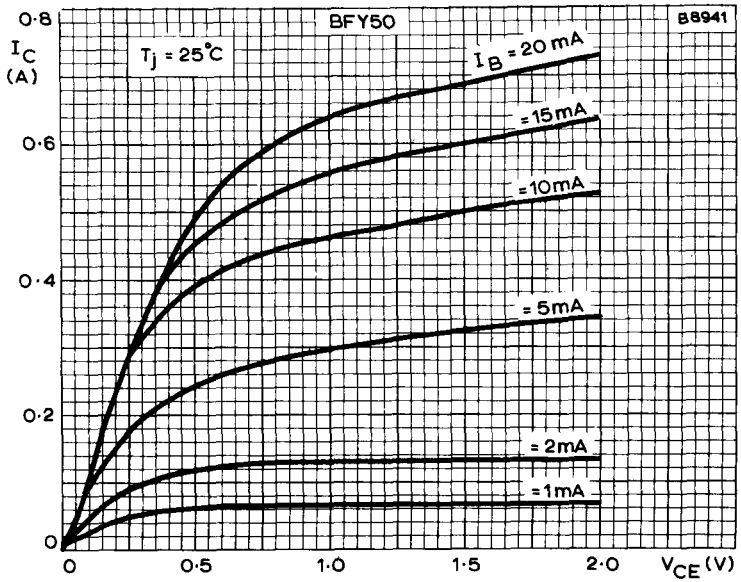


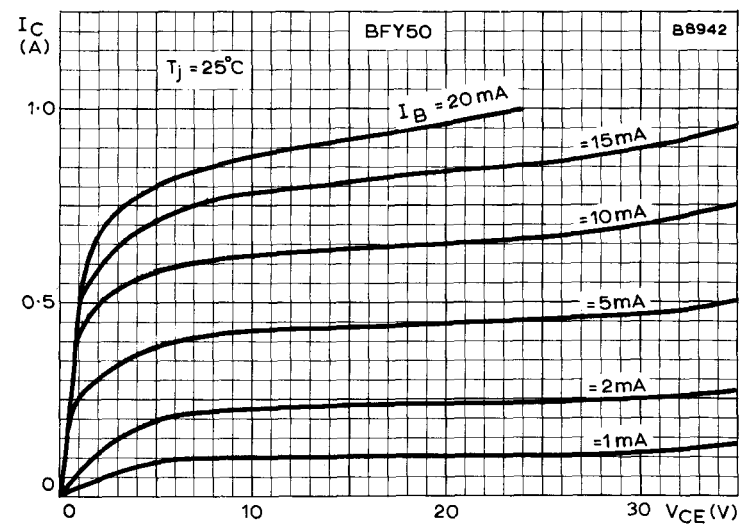


MAXIMUM COLLECTOR-EMITTER VOLTAGE PLOTTED AGAINST R_B/R_E RATIO

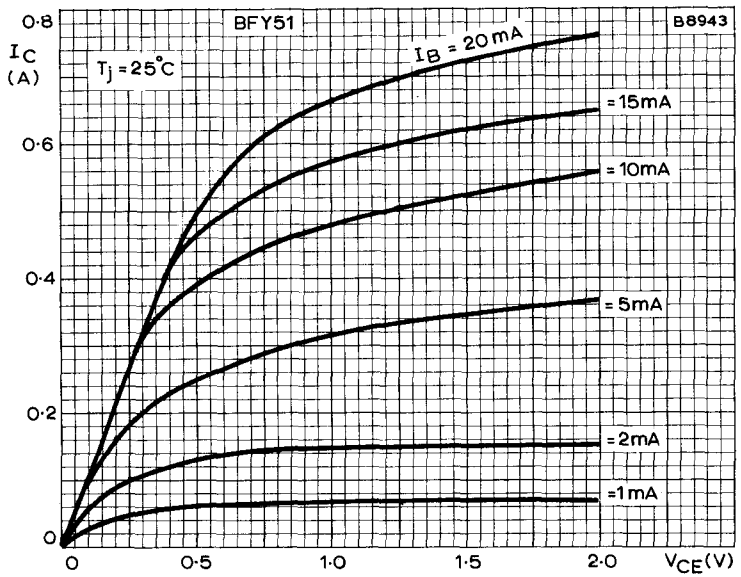


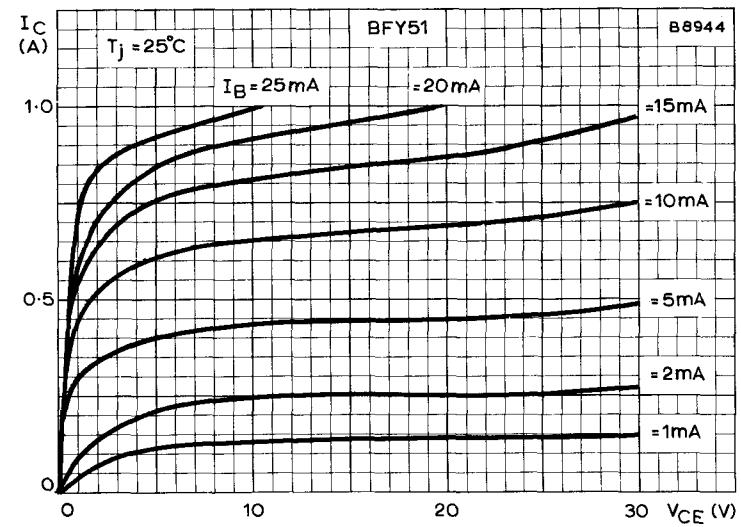
COLLECTOR AND EMITTER CUT-OFF CURRENTS PLOTTED AGAINST JUNCTION TEMPERATURE



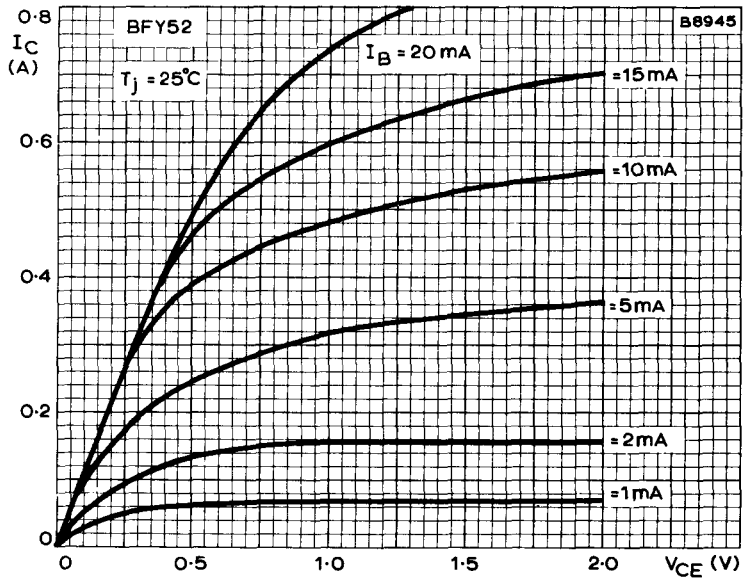


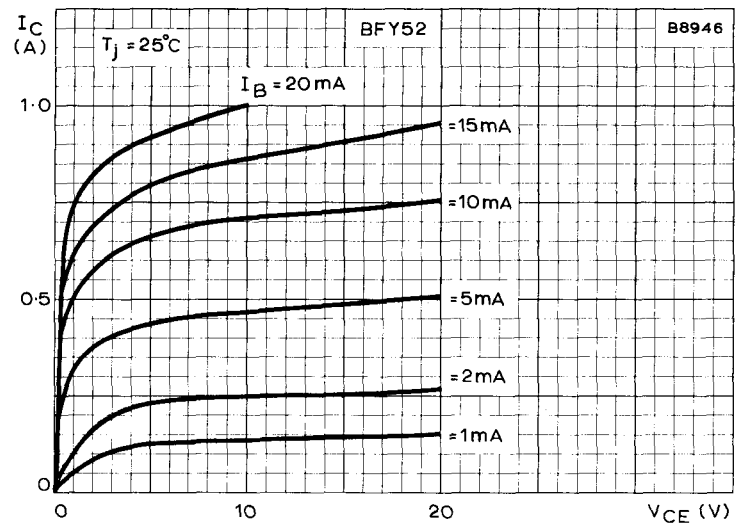
TYPICAL OUTPUT CHARACTERISTICS



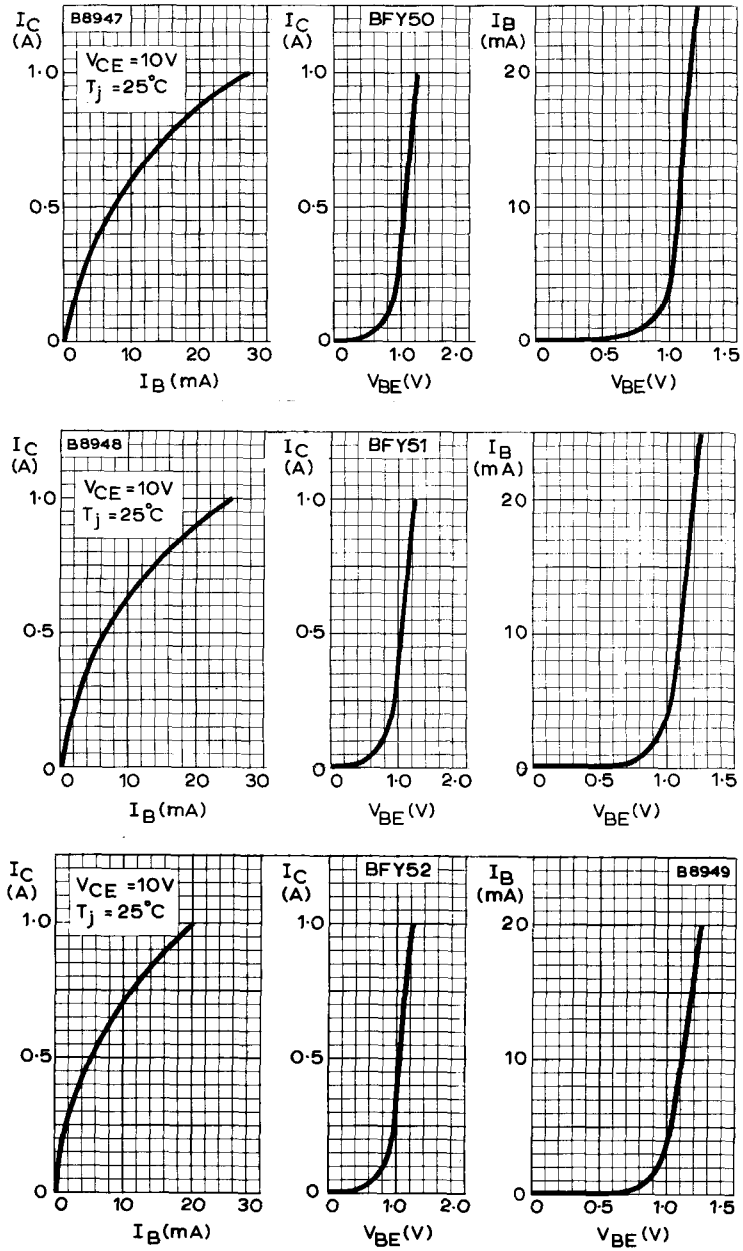


TYPICAL OUTPUT CHARACTERISTICS

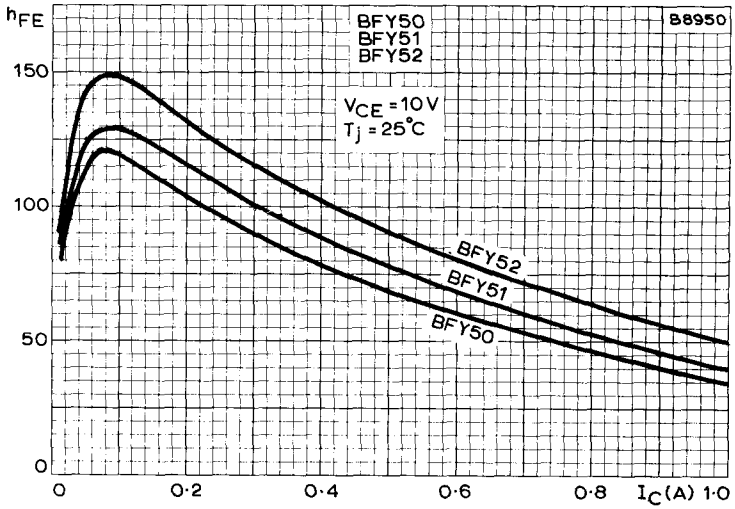


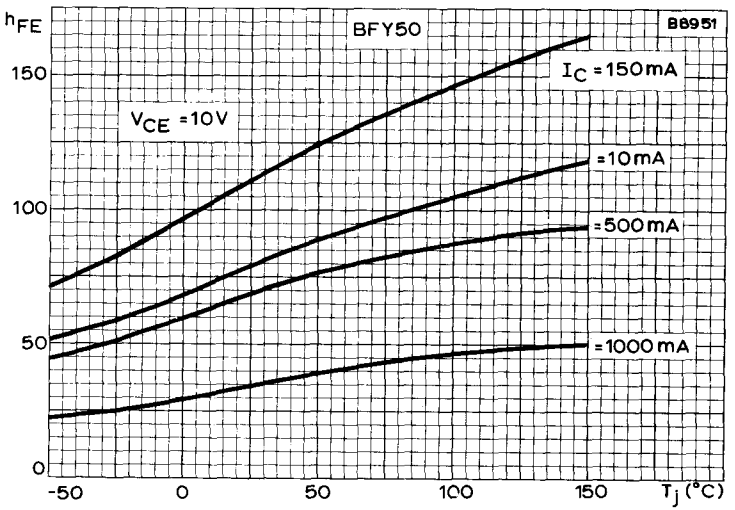


TYPICAL OUTPUT CHARACTERISTICS

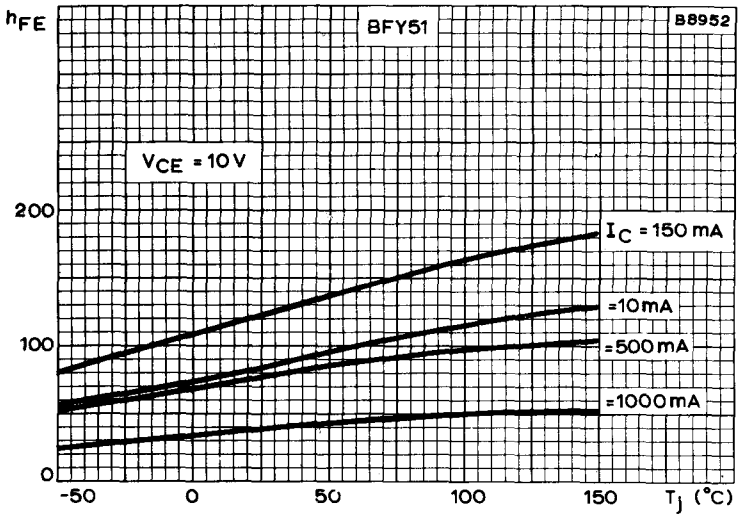


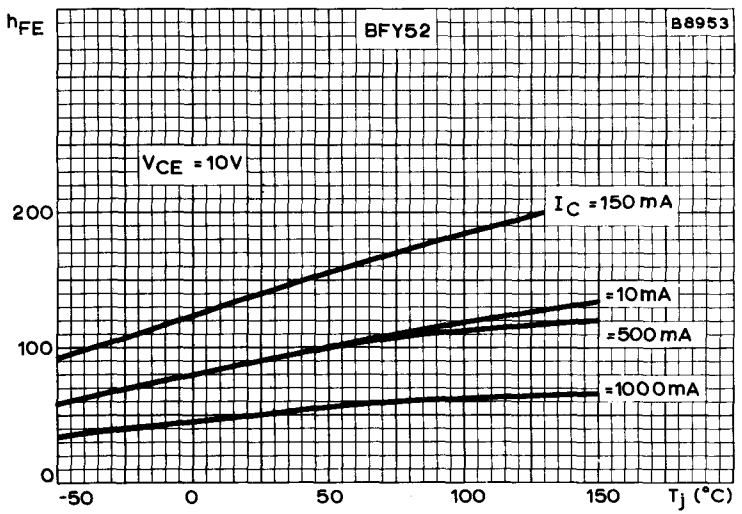
TYPICAL TRANSFER, MUTUAL AND INPUT CHARACTERISTICS



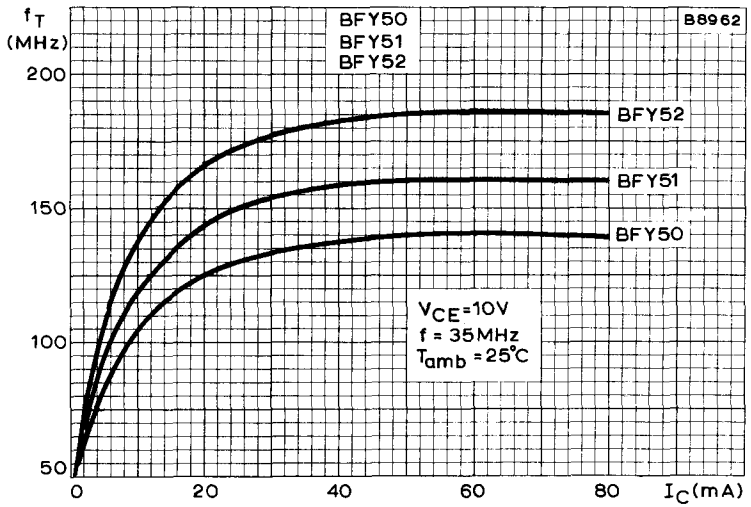


TYPICAL STATIC FORWARD CURRENT TRANSFER RATIO PLOTTED AGAINST COLLECTOR CURRENT AND JUNCTION TEMPERATURE

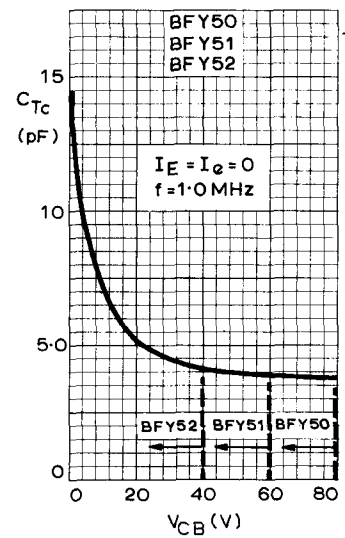




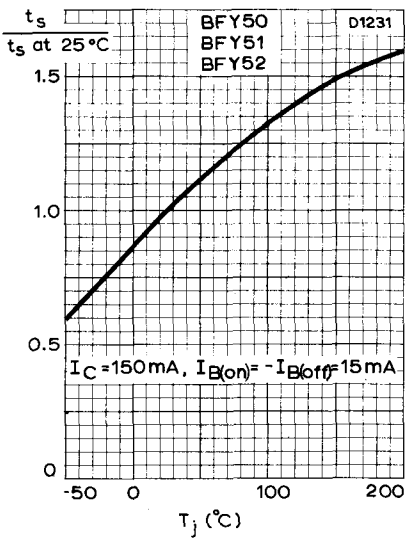
TYPICAL STATIC FORWARD CURRENT TRANSFER RATIO PLOTTED AGAINST JUNCTION TEMPERATURE



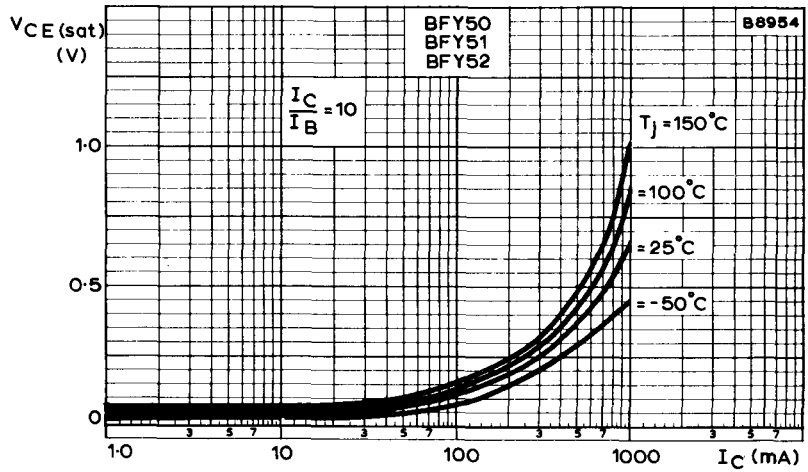
TYPICAL TRANSITION FREQUENCY PLOTTED AGAINST COLLECTOR CURRENT

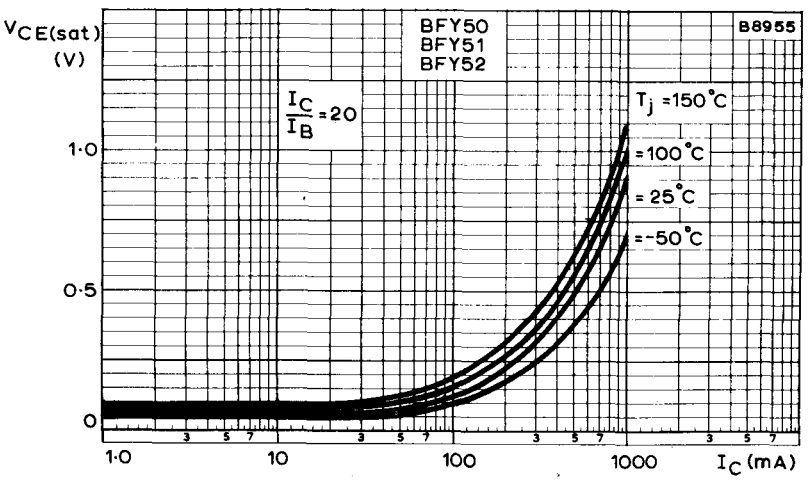


Typical collector capacitance versus collector-base voltage

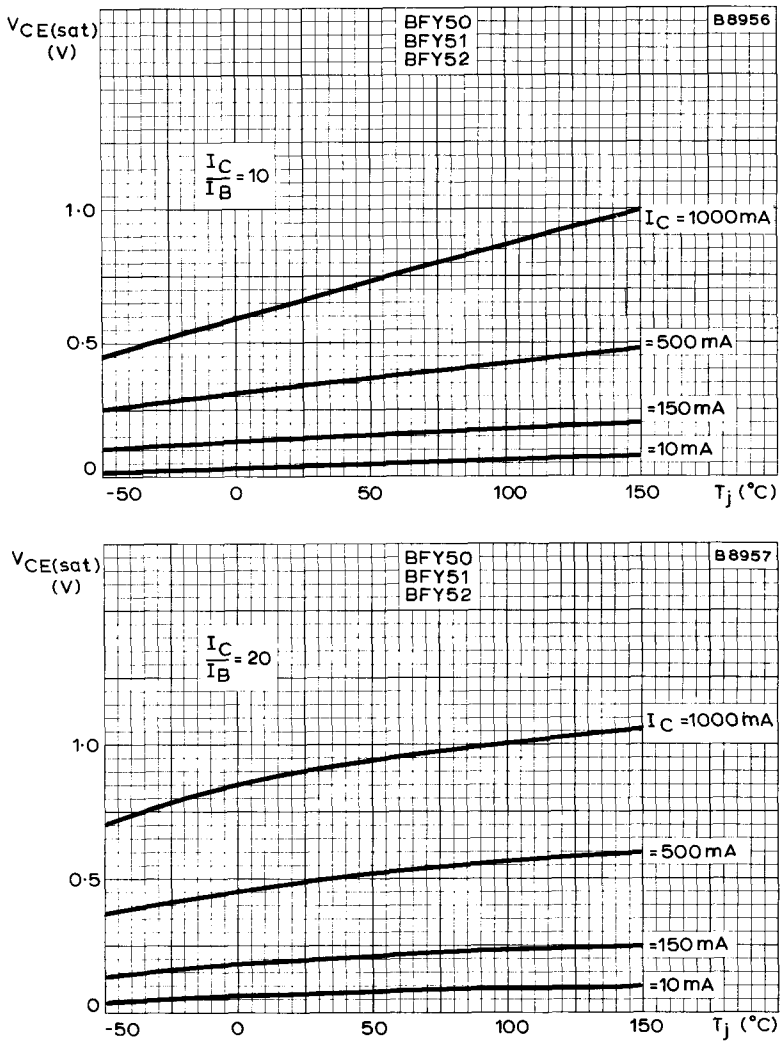


Typical storage time normalised at 25°C

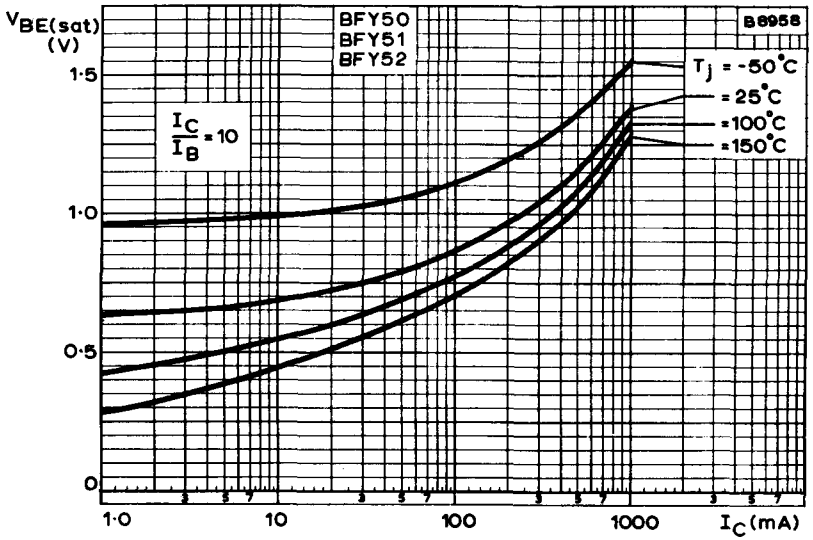


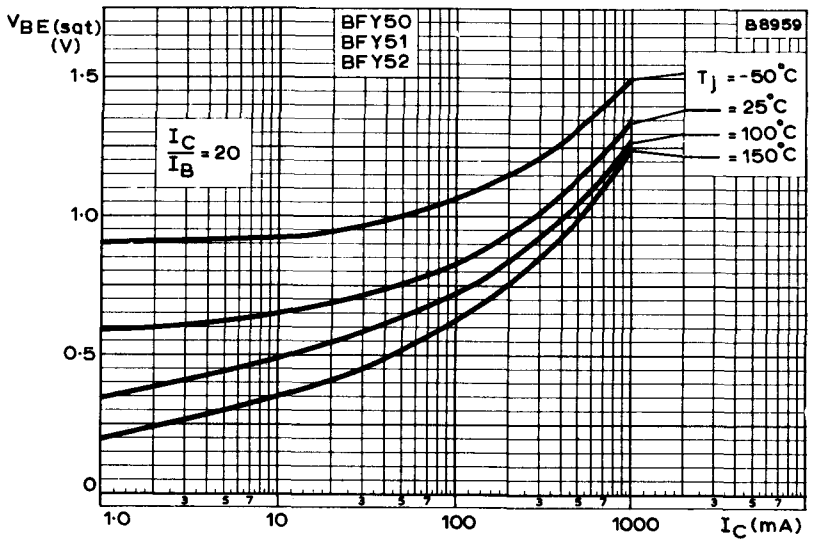


TYPICAL COLLECTOR-EMITTER SATURATION VOLTAGE
PLOTTED AGAINST COLLECTOR CURRENT

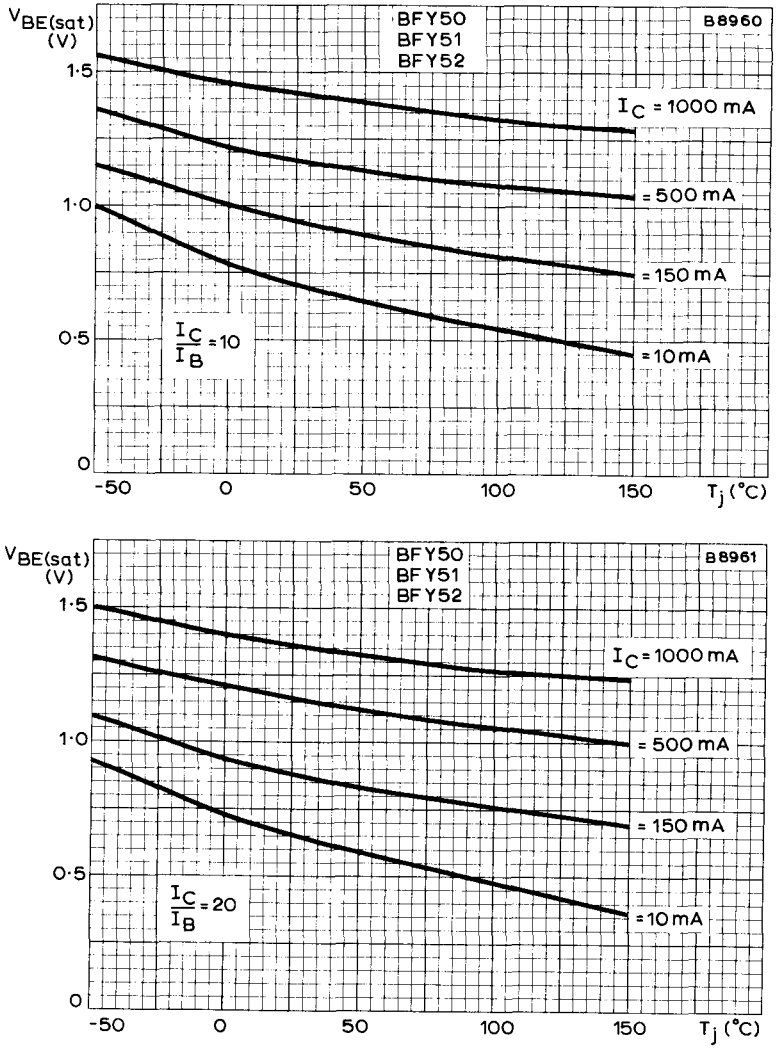


TYPICAL COLLECTOR-EMITTER SATURATION VOLTAGE
PLOTTED AGAINST JUNCTION TEMPERATURE

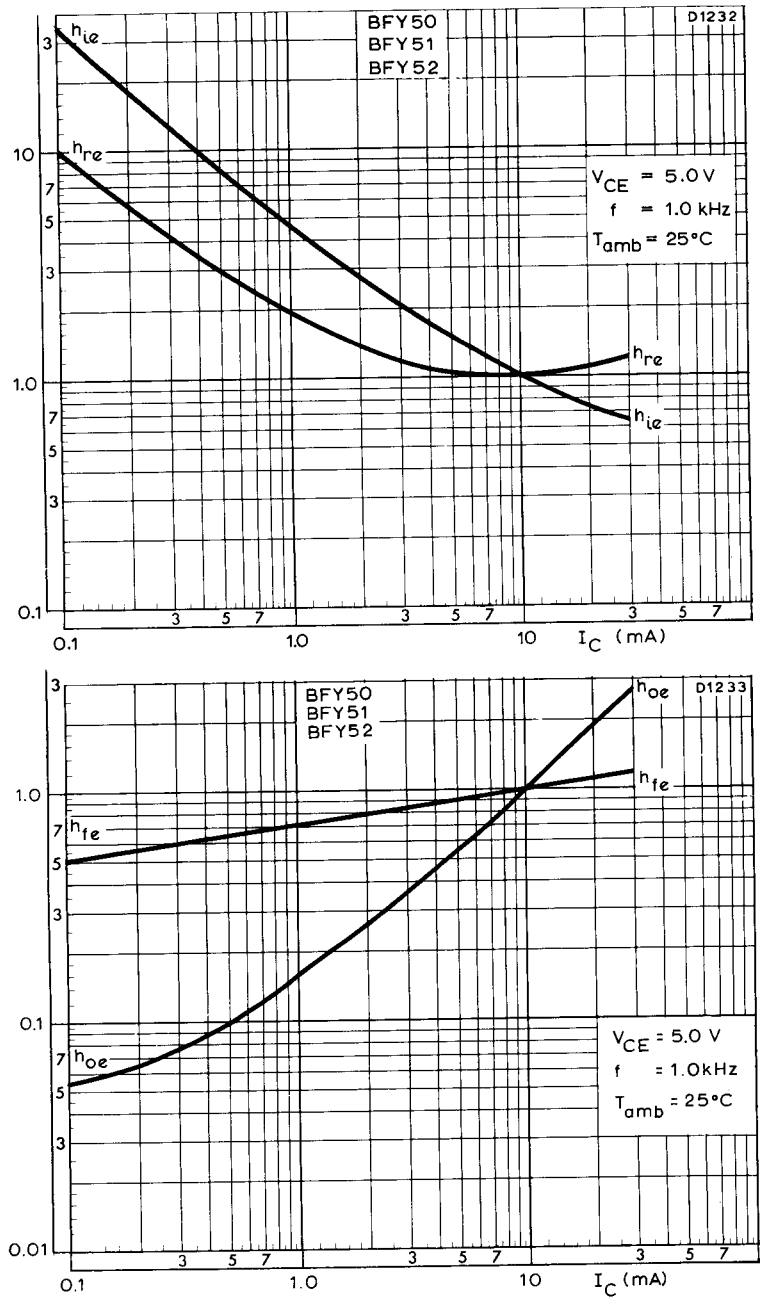




TYPICAL BASE-EMITTER SATURATION VOLTAGE
PLOTTED AGAINST COLLECTOR CURRENT



TYPICAL BASE-EMITTER SATURATION VOLTAGE
PLOTTED AGAINST JUNCTION TEMPERATURE



TYPICAL h-PARAMETERS NORMALISED AT I_C = 10mA

N-P-N SILICON PLANAR EPITAXIAL TRANSISTOR

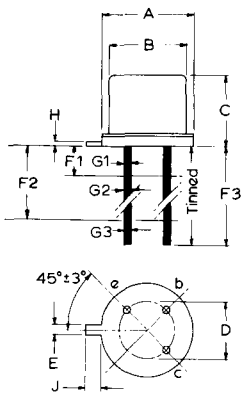
BFY53

Silicon n-p-n planar epitaxial transistor for general purpose industrial applications. Encapsulated in TO-5 envelope with the collector connected to can.

QUICK REFERENCE DATA			
V_{CBO} max.		40	V
V_{CEO} max.		20	V
I_{CM} max.		1.0	A
P_{tot} max.	($T_{amb} \leq 25^{o}C$)	800	mW
	($T_{case} \leq 25^{o}C$)	5.0	W
h_{FE} ($I_C = 150mA$, $V_{CE} = 10V$)	min.	30	
	typ.	75	
f_T min. ($I_C = 50mA$, $V_{CE} = 10V$, $f = 35MHz$, $T_{amb} = 25^{o}C$)		50	MHz

OUTLINE AND DIMENSIONS

Conforms to BS3934 SO-3/SB3-3A
J.E.D.E.C. TO-5



Collector connected to can

	Millimetres		
	Min.	Nom.	Max.
A	9.1	-	9.4
B	8.2	-	8.5
C	6.1	-	6.6
D	-	5.08	-
E	0.71	-	0.86
F1	-	-	0.51
F2	12.7	-	-
F3	38.1	-	41.3
G1	-	-	1.01
G2	0.41	-	0.48
G3	-	-	0.53
H	0.3	-	0.8
J	0.74	-	1.0

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{CBO} max.	40	V
V_{CE} max. (cut-off, $I_C \leq 1mA$)	40	V
V_{CEO} max.	20	V
V_{EBO} max.	6.0	V
I_C max.	1.0	A
I_{CM} max.	1.0	A
$-I_E$ max.	1.0	A
$-I_{EM}$ max.	1.0	A
I_B max.	100	mA
$\pm I_{BM}$ max.	100	mA
P_{tot} max. ($T_{amb} \leq 25^oC$)	800	mW
($T_{case} \leq 25^oC$)	5.0	W

Temperature

T_{stg} range	-65 to +200	^oC
T_j max.	200	^oC

THERMAL CHARACTERISTICS

$R_{th(j-amb)}$	220	degC/W
$R_{th(j-case)}$	35	degC/W

ELECTRICAL CHARACTERISTICS ($T_j = 25^oC$ unless otherwise stated)

		Min.	Typ.	Max.	
I_{CBO}	Collector cut-off current				
	$V_{CB}=40V$, $I_E=0$	-	10	500	nA
	$V_{CB}=40V$, $I_E=0$, $T_j=100^oC$	-	0.5	30	μA
	$V_{CB}=30V$, $I_E=0$	-	2.0	50	nA
	$V_{CB}=30V$, $I_E=0$, $T_j=100^oC$	-	0.1	2.5	μA
I_{EBO}	Emitter cut-off current				
	$V_{EB}=6.0V$, $I_C=0$	-	10	500	nA
	$V_{EB}=5.0V$, $I_C=0$	-	2.0	50	nA
	$V_{EB}=5.0V$, $I_C=0$, $T_j=100^oC$	-	0.1	2.5	μA

ELECTRICAL CHARACTERISTICS (contd.)

		Min.	Typ.	Max.	
h_{FE}	Static forward current transfer ratio				
	$I_C = 10mA$, $V_{CE} = 10V$	20	55	-	
	$I_C = 150mA$, $V_{CE} = 10V$	30	75	-	
	$I_C = 500mA$, $V_{CE} = 10V$	18	50	-	
	$I_C = 1.0A$, $V_{CE} = 10V$	10	35	-	
$V_{CE(sat)}$	Collector-emitter saturation voltage				
	$I_C = 10mA$, $I_B = 1.0mA$	-	0.06	0.15	V
	$I_C = 150mA$, $I_B = 15mA$	-	0.15	0.35	V
	$I_C = 500mA$, $I_B = 50mA$	-	0.35	1.00	V
	$I_C = 1.0A$, $I_B = 100mA$	-	0.66	2.00	V
$V_{BE(sat)}$	Base-emitter saturation voltage				
	$I_C = 10mA$, $I_B = 1.0mA$	-	0.69	1.2	V
	$I_C = 150mA$, $I_B = 15mA$	-	0.92	1.3	V
	$I_C = 500mA$, $I_B = 50mA$	-	1.15	1.5	V
	$I_C = 1.0A$, $I_B = 100mA$	-	1.40	2.0	V
C_{Tc}	Collector capacitance $V_{CB} = 10V$, $I_E = I_e = 0$, $f = 1.0MHz$	-	7.0	12	pF
f_T	Transition frequency $I_C = 50mA$, $V_{CE} = 10V$, $f = 35MHz$, $T_{amb} = 25^oC$	50	140	-	MHz
h_{fe}	Small signal forward current transfer ratio $I_C = 1.0mA$, $V_{CE} = 5.0V$, $f = 1.0kHz$, $T_{amb} = 25^oC$	10	70	-	

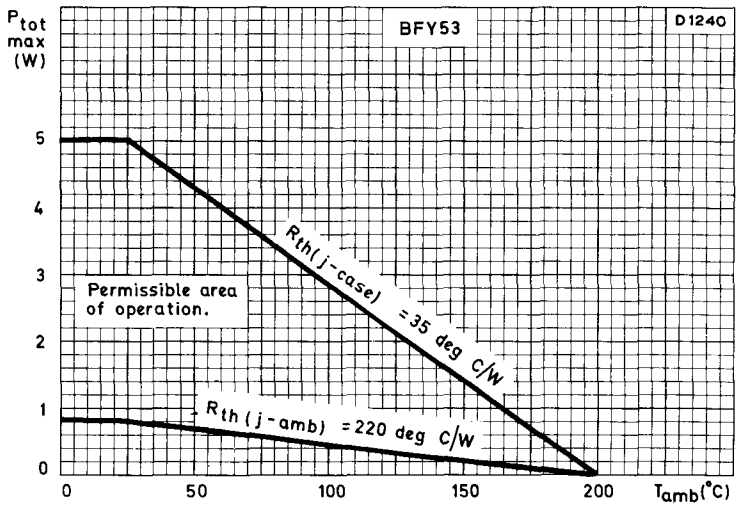
SOLDERING AND WIRING RECOMMENDATIONS

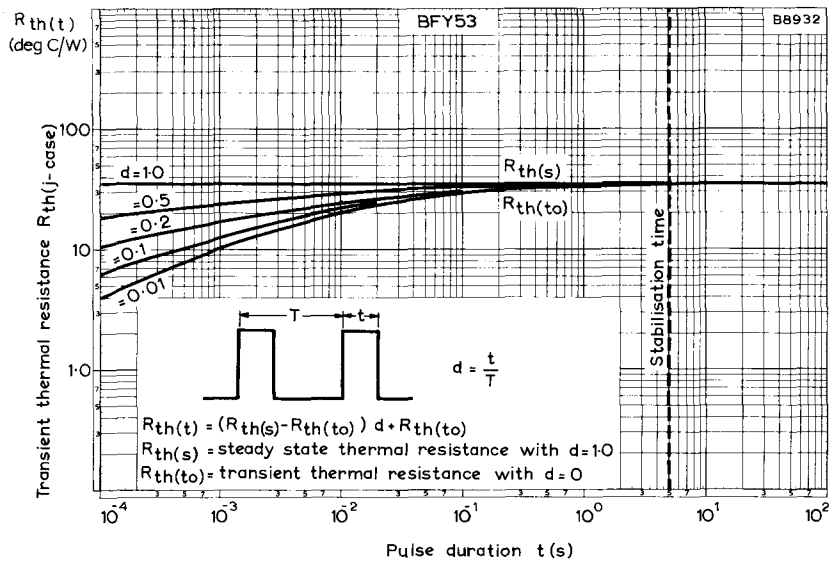
1. When using a soldering iron, transistors may be soldered directly into the circuit, but heat conducted to the junction should if possible be kept to a minimum by the use of a thermal shunt.

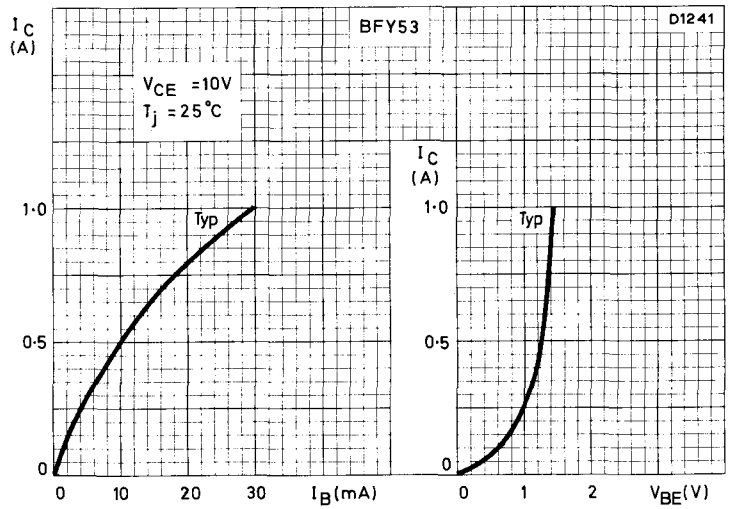
2. Transistors may be dip-soldered at a solder temperature of 245°C for a maximum soldering time of 5 seconds. The case temperature during soldering must not at any time exceed the maximum storage temperature. These recommendations apply to a transistor mounted flush on a board having punched-through holes, or spaced at least 1.5mm above a board having plated-through holes.

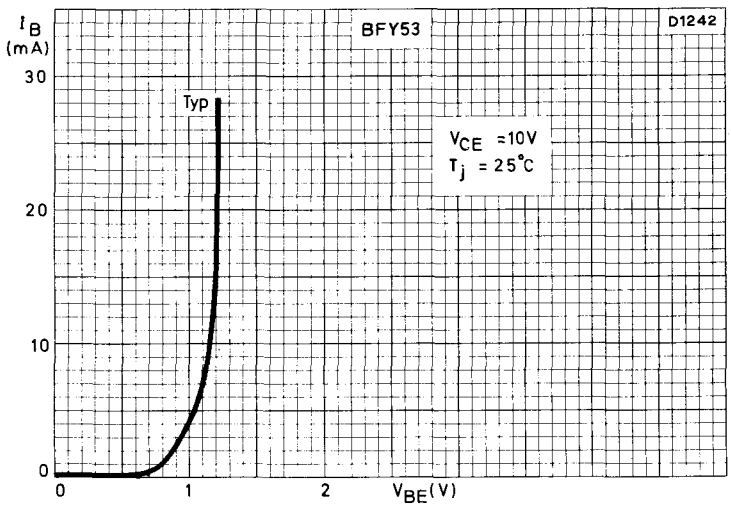
3. Care should be taken not to bend the leads nearer than 1.5mm from the seal.

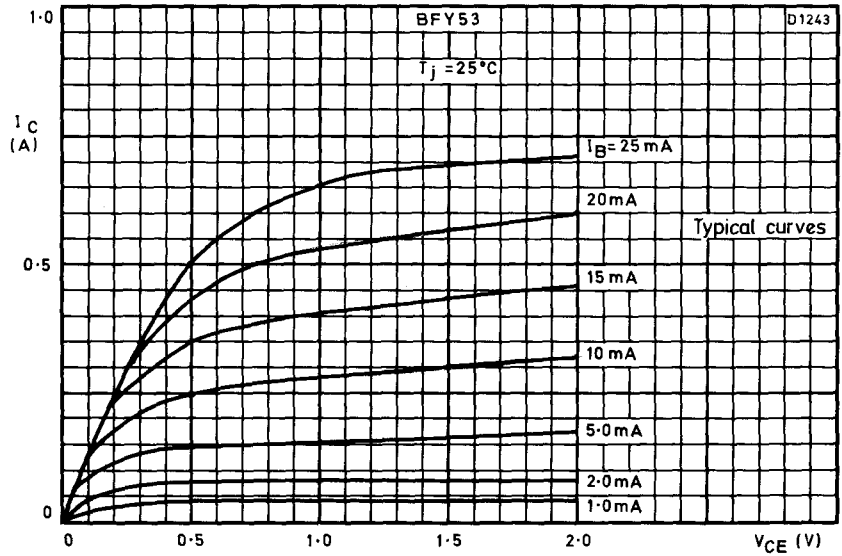
4. If devices are stored at temperatures above 100°C before incorporation into equipment, some deterioration of the external surface is likely to occur which may make soldering into the circuit difficult. Under these circumstances the leads should be retinned using a suitable activated flux.

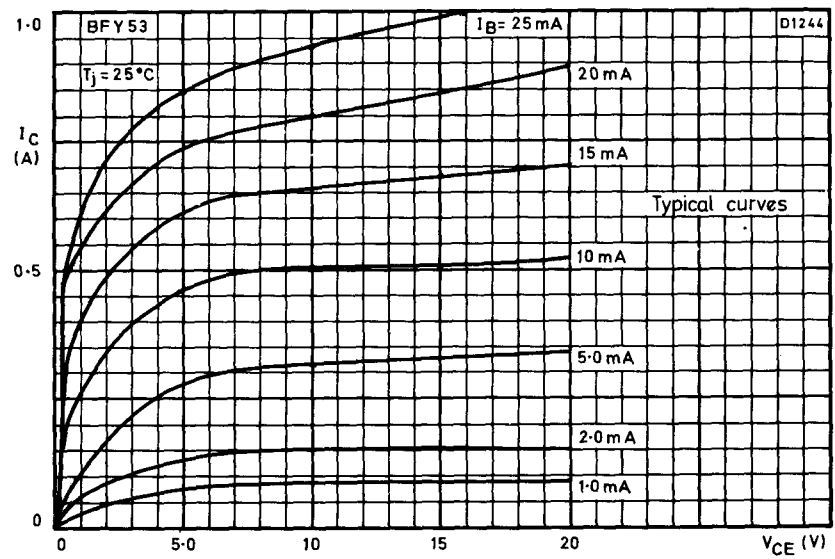

BFY53
D1240
P_{tot} max (W)
5
4
3
2
1
0
Permissible area of operation.
$R_{th(j-case)}$ = 35 deg C/W
$R_{th(j-amb)}$ = 220 deg C/W
0
50
100
150
200
T_{amb}(°C)

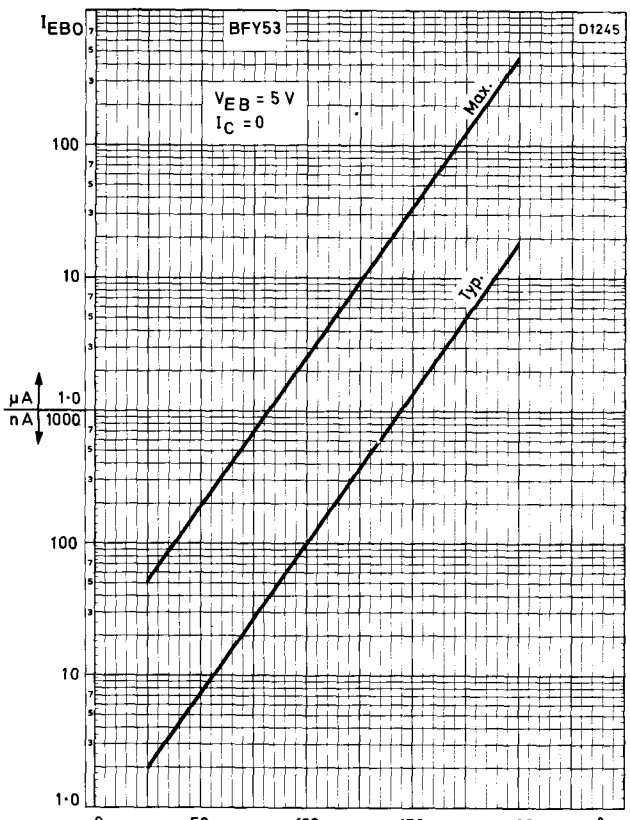

$R_{th(t)}$ (deg C/W)
BFY53
B8932
Transient thermal resistance $R_{th(j-case)}$
100
10
1·0
d=1·0
=0·5
=0·2
=0·1
=0·01
$R_{th(s)}$
$R_{th(to)}$
Stabilisation time
T
t
$d = \frac{t}{T}$
$R_{th(t)} = (R_{th(s)} - R_{th(to)})\ d + R_{th(to)}$
$R_{th(s)}$ = steady state thermal resistance with d=1·0
$R_{th(to)}$ = transient thermal resistance with d = 0
10^{-4}
10^{-3}
10^{-2}
10^{-1}
10^{0}
10^{1}
10^{2}
Pulse duration t (s)

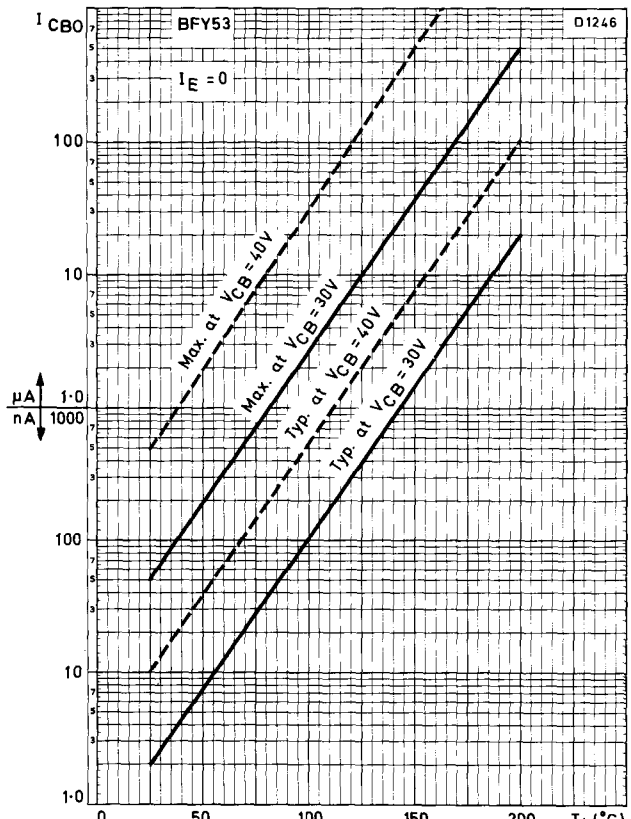

BFY53
D1241
I_C (A)
V_{CE} =10V
T_j = 25°C
Typ
1·0
0·5
0
0
10
20
30
I_B(mA)
I_C (A)
1·0
0·5
0
Typ
0
1
2
V_{BE}(V)

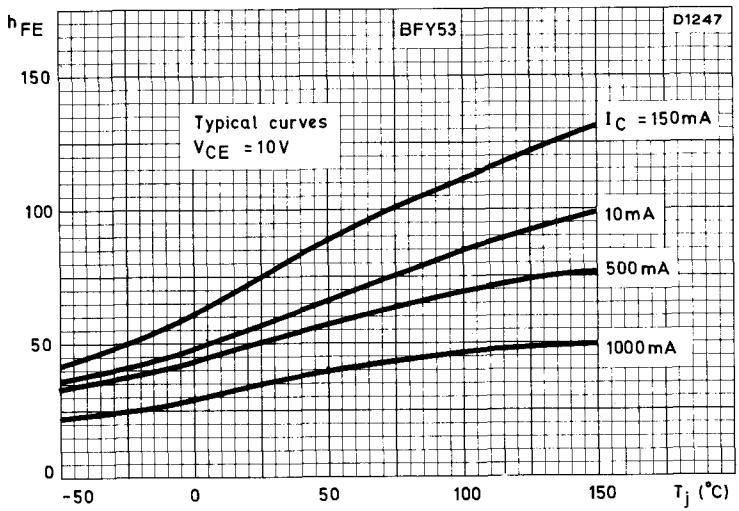

BFY53
D1242
I_B (mA)
30
20
10
0
Typ
V_{CE} =10V
T_j = 25°C
0
1
2
V_{BE}(V)

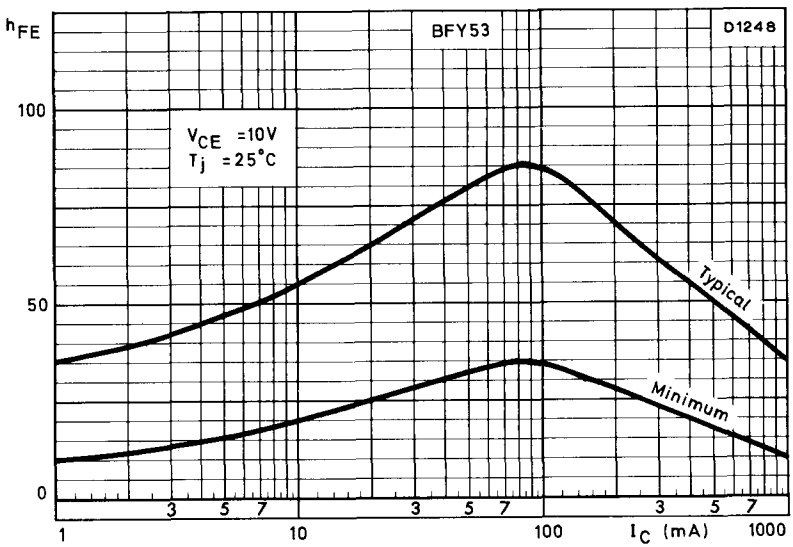

BFY53
D1243
T_j = 25°C
I_C (A)
1·0
0·5
0
I_B = 25 mA
20 mA
15 mA
10 mA
5·0 mA
2·0 mA
1·0 mA
Typical curves
0
0·5
1·0
1·5
2·0
V_{CE} (V)

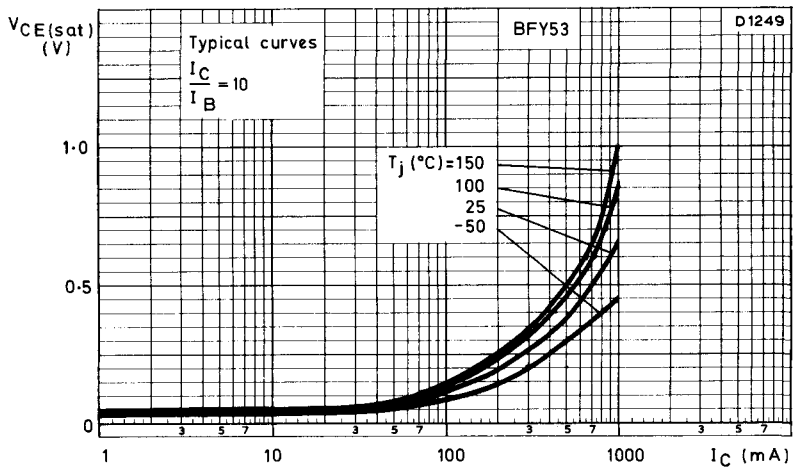

BFY53
D1244
T_j = 25°C
I_B = 25 mA
I_C (A)
1·0
0·5
0
20 mA
15 mA
10 mA
5·0 mA
2·0 mA
1·0 mA
Typical curves
0
5·0
10
15
20
V_{CE} (V)

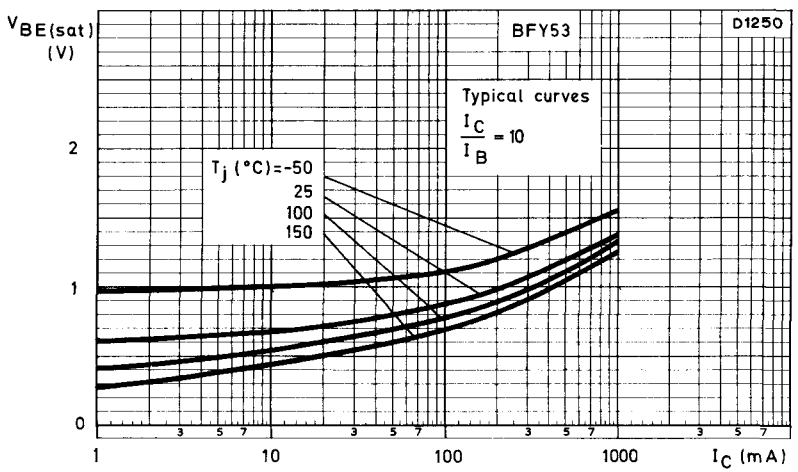

BFY53
D1245
I_{EBO}
V_{EB} = 5 V
I_C = 0
Max.
Typ.
μA 1·0
nA 1000
100
10
1·0
0
50
100
150
200
T_j (°C)

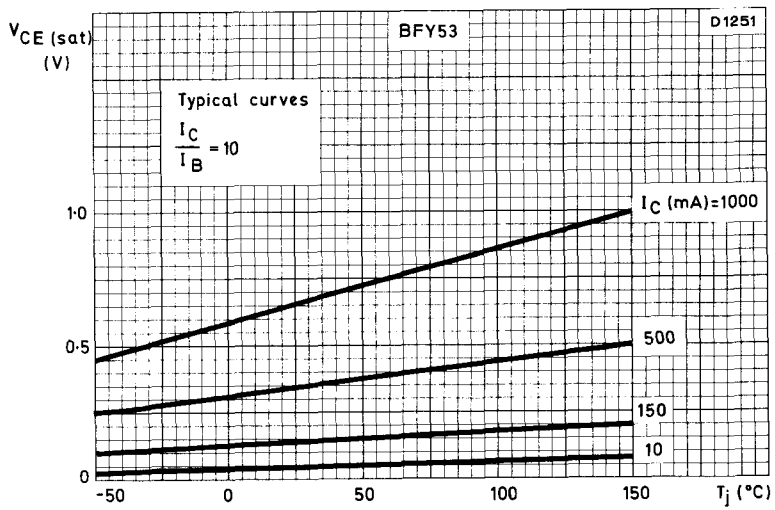

BFY53
D1246
I_{CBO}
I_E = 0
Max. at V_{CB} = 40V
Max. at V_{CB} = 30V
Typ. at V_{CB} = 40V
Typ. at V_{CB} = 30V
μA 1·0
nA 1000
100
10
1·0
0
50
100
150
200
T_j (°C)

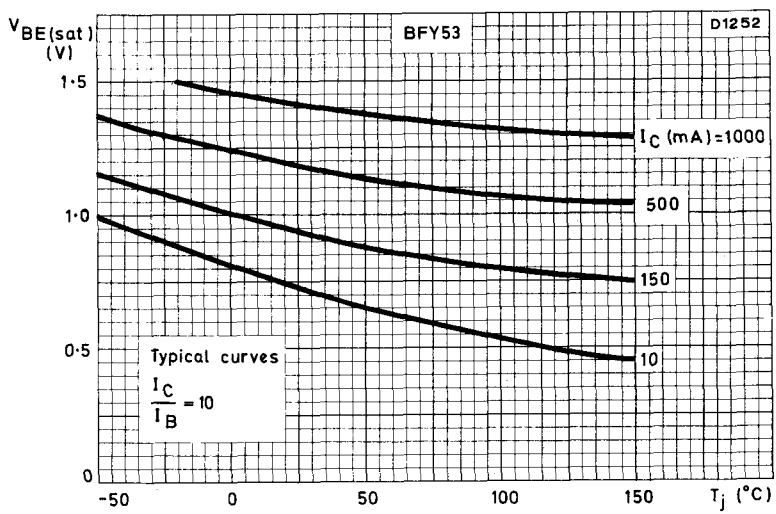

hFE
BFY53
D1247
150
100
50
0
Typical curves
VCE = 10V
IC = 150mA
10mA
500mA
1000mA
-50
0
50
100
150
Tj (°C)

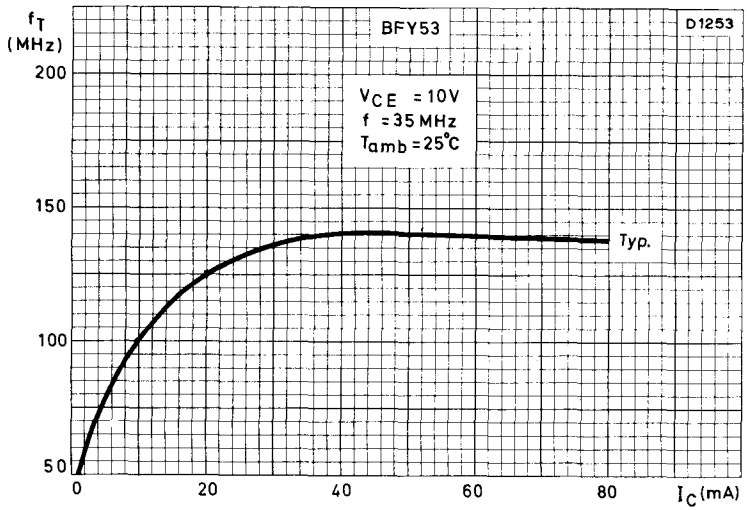

hFE
BFY53
D1248
100
50
0
VCE = 10V
Tj = 25°C
Typical
Minimum
1
3
5
7
10
3
5
7
100
3
5
7
1000
IC (mA)

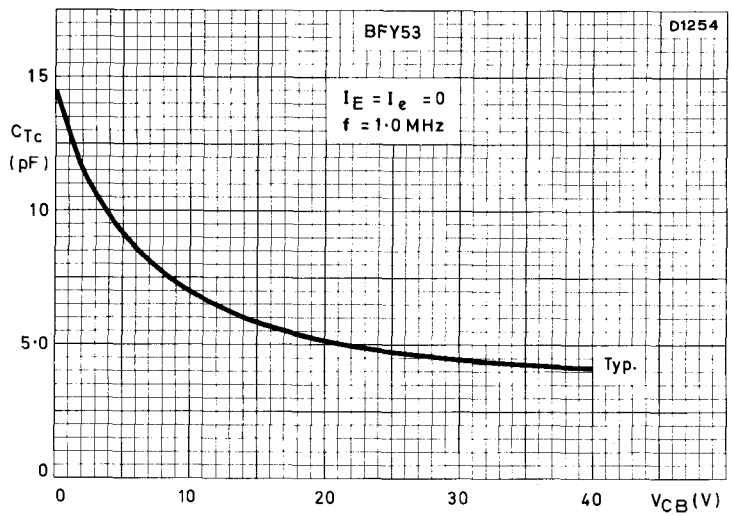

$V_{CE(sat)}$ (V)
Typical curves
$\frac{I_C}{I_B} = 10$
BFY53
D1249
T_j (°C)=150
100
25
-50
1·0
0·5
0
1
10
100
1000
I_C (mA)


$V_{BE(sat)}$ (V)
BFY53
D1250
Typical curves
$\frac{I_C}{I_B} = 10$
T_j (°C)=-50
25
100
150
2
1
0
1
10
100
1000
I_C (mA)


BFY53
D1251
$V_{CE(sat)}$ (V)
Typical curves
$\frac{I_C}{I_B} = 10$
I_C (mA)=1000
500
150
10
1·0
0·5
0
-50
0
50
100
150
T_j (°C)


BFY53
D1252
$V_{BE(sat)}$ (V)
Typical curves
$\frac{I_C}{I_B} = 10$
I_C (mA)=1000
500
150
10
1·5
1·0
0·5
0
-50
0
50
100
150
T_j (°C)


BFY53
D1253
V_{CE} = 10V
f = 35 MHz
T_{amb} = 25°C
Typ.
f_T (MHz)
200
150
100
50
0
20
40
60
80
I_C (mA)


BFY53
D1254
$I_E = I_e$ = 0
f = 1·0 MHz
Typ.
C_{Tc} (pF)
15
10
5·0
0
0
10
20
30
40
V_{CB} (V)

SILICON PLANAR EPITAXIAL N-P-N TRANSISTOR

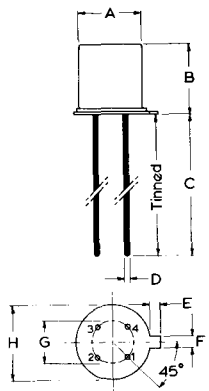
BFY90

N-P-N silicon planar epitaxial transistor featuring low noise, low intermodulation distortion and a high transition frequency. Intended for military and industrial applications.

QUICK REFERENCE DATA		
V_{CBO} max.	30	V
V_{CEO} max.	15	V
I_{CM} max.	50	mA
P_{tot} max. ($T_{amb}=25^{o}C$)	200	mW
T_j max.	200	^{o}C
f_T min. $I_C=2.0mA$, $V_{CE}=5.0V$	1.0	Gc/s
$I_C=25mA$, $V_{CE}=5.0V$	1.3	Gc/s
$-c_{re}$ max. $I_C=2.0mA$, $f=1.0Mc/s$	0.8	pF
Max. noise figure, $I_C=2.0mA$, $f=500Mc/s$	5.0	dB

OUTLINE AND DIMENSIONS

Conforming to B.S.3934 SO-12A/SB4-3
J.E.D.E.C. TO-72



	Millimetres		
	Min.	Nom.	Max.
A	-	-	4.8
B	-	-	5.33
C	12.7	-	-
D	-	-	0.48
E	-	-	1.17
F	-	-	1.16
G	-	2.54	-
H	-	-	5.83

Viewed from underside

Connections: 1. Emitter 3. Collector
2. Base 4. Shield connected to envelope

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{CBO} max. ($I_E = 0$)	30	V
V_{CEO} max. ($I_B = 0$, $I_C = 10mA$)	15	V
V_{EBO} max. ($I_C = 0$)	2.5	V
I_{CM} max.	50	mA
$I_{C(AV)}$ max. (averaged over any 100μs period)	25	mA
P_{tot} max. ($T_{amb} = 25^oC$)	200	mW

Temperature

T_{stg} max.	200	^oC
T_{stg} min.	-65	^oC
T_j max.	200	^oC

THERMAL CHARACTERISTICS

$\Theta_{j\text{-amb}}$ (in free air)	0.88	deg C/mW
$\Theta_{j\text{-case}}$	0.58	deg C/mW

ELECTRICAL CHARACTERISTICS ($T_j = 25^oC$ unless otherwise specified)

		Min.	Typ.	Max.	
	Collector cut-off current				
I_{CBO}	$V_{CB} = 15V$, $I_E = 0$	-	-	10*	nA
I_{CES}	$V_{CE} = 15V$, $V_{BE} = 0$	-	-	10	μA
I_B	Base current				
	$-I_E = 2.0mA$, $V_{CB} = 0$	13.2*	-	77*	μA
	$-I_E = 25mA$, $V_{CB} = 0$	200*	-	1200*	μA
h_{FE}	Static forward current transfer ratio				
	$I_C = 2.0mA$, $V_{CE} = 1.0V$	25	-	150	
	$I_C = 25mA$, $V_{CE} = 1.0V$	20	-	125	
f_T	Transition frequency†				
	$I_C = 2.0mA$, $V_{CE} = 5.0V$	1.0	-	-	Gc/s
	$I_C = 25mA$, $V_{CE} = 5.0V$	1.3	-	-	Gc/s
c_{tc}	Collector capacitance**				
	$V_{CB} = 10V$, $I_E = I_e = 0$, $f = 1.0Mc/s$	-	-	1.5	pF
c_{te}	Emitter capacitance				
	$V_{EB} = 0.5V$, $I_C = I_c = 0$, $f = 1.0Mc/s$	-	-	2.0	pF

		Min.	Typ.	Max.	
$V_{CEO(sust)}$	Collector-emitter sustaining voltage				
	$I_C = 10mA$, $I_B = 0$	15	-	-	V
$-c_{re}$	Feedback capacitance				
	$I_C = 2.0mA$, $V_{CE} = 5.0V$, $f = 1.0Mc/s$	-	-	0.8	pF
$r_{bb'}c_{b'c}$	Feedback time constant†				
	$-I_E = 2.0mA$, $V_{CB} = 5.0V$, $f = 10.7Mc/s$	2.0	-	12	ps
NF	Noise figure†, $I_C = 2.0mA$, $V_{CE} = 5.0V$				
	$f = 100kc/s$, optimum R_s	-	-	4.0	dB
	$f = 200Mc/s$, optimum Z_s	-	-	3.5	dB
	$f = 500Mc/s$, $R_s = 50\Omega$	-	-	5.0	dB
d_{im}	Intermodulation distortion (See fig. 1)				
	$I_C = 14mA$, $V_{CE} = 6.0V$, $f = 217Mc/s$				
	$V_o = 100mV$, $R_L = 37.5\Omega$				
	$f_1 = 183Mc/s$, $f_2 = 200Mc/s$	-	-53	-	dB
P_o	Output power‡ (See fig. 2)				
	$I_C = 22.5mA$, $V_{CE} = 13.5V$, $P_i = 25mW$				
	$f = 500Mc/s$, $T_{case} = 25^oC$	175	-	-	mW

*These are the characteristics which are recommended for acceptance testing purposes.

†Shield lead grounded.

**Shield lead not connected

‡Care must be taken to reduce steady state current when no h.f. signal is applied.

Small signal y-parameters

$I_C = 2.0mA$, $V_{CE} = 5.0V$, f = 500Mc/s

		Min.	Typ.	Max.	
g_{ie}	Input conductance	-	16	-	mmho
c_{ie}	Input capacitance	-	3.75	-	pF
$\|y_{re}\|$	Feedback admittance	-	1.55	-	mmho
ϕ_{re}	Phase angle of y_{re}	-	258	-	deg
$\|y_{fe}\|$	Forward transfer admittance	-	45	-	mmho
ϕ_{fe}	Phase angle of y_{fe}	-	285	-	deg
g_{oe}	Output conductance	-	0.19	-	mmho
c_{oe}	Output capacitance	-	1.9	-	pF
G_{UM}	Max. unilateralised power gain $10 \log \frac{\|y_{fe}\|^2}{4 g_{ie} g_{oe}}$ $I_C = 2.0mA$, $V_{CE} = 5.0V$, f = 500Mc/s	-	22	-	dB

INTERMODULATION DISTORTION TEST CIRCUIT

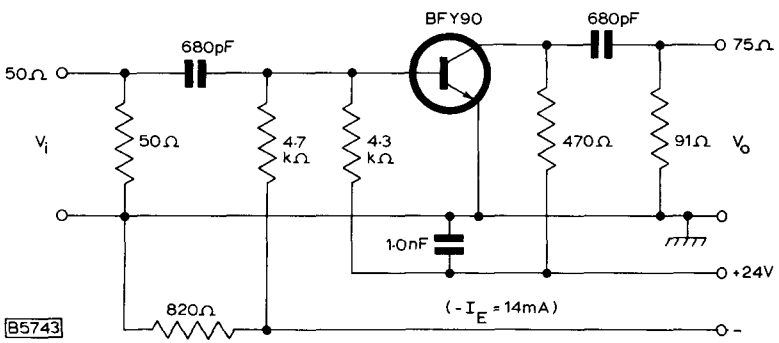


Fig. 1.

CIRCUIT FOR MEASUREMENT OF THE OUTPUT POWER

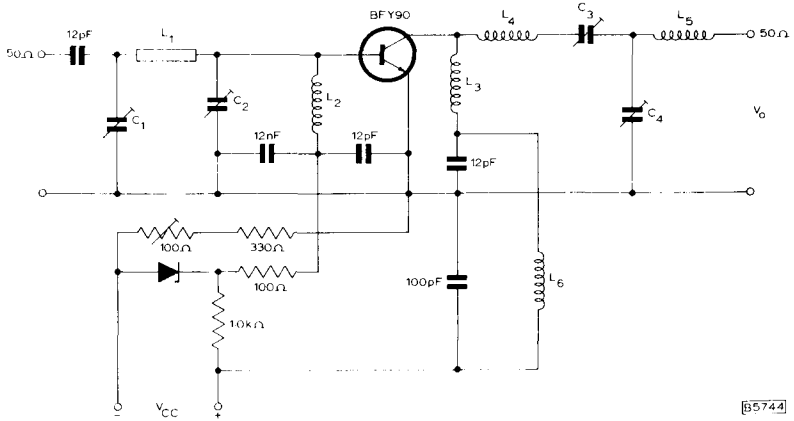


Fig. 2.

C_1 = 16pF air-gap trimmer

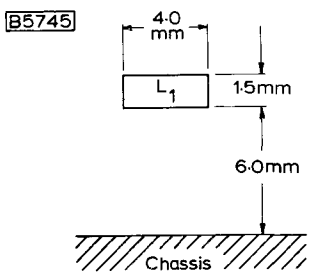
C_2, C_3, C_4 = 6pF ceramic trimmer

L_1 = copper strip 20 × 4 × 1.5mm

L_2, L_6 = 10 turns of 0.7mm en. copper wire, dia = 4mm

L_3 = 1 turn of 1mm copper wire, dia = 8mm

L_4, L_5 = 1 turn of 1mm copper wire dia = 7mm



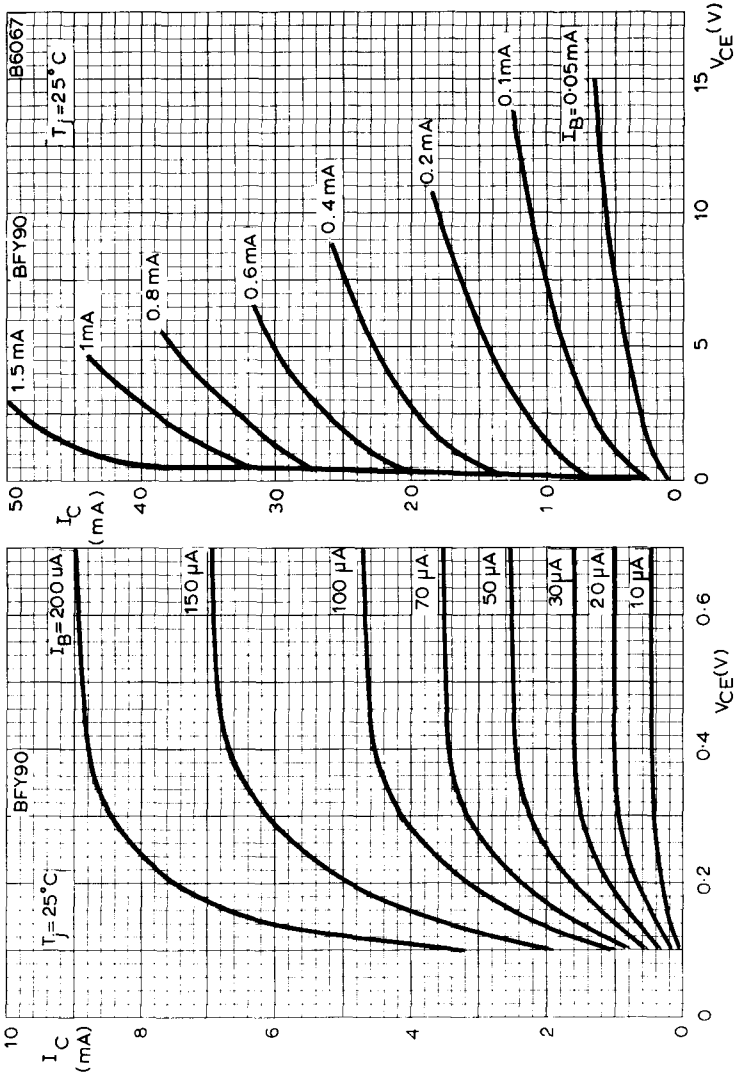
SOLDERING AND WIRING RECOMMENDATIONS

1. When using a soldering iron, transistors may be soldered directly into the circuit, but heat conducted to the junction should if possible be kept to a minimum by the use of a thermal shunt.

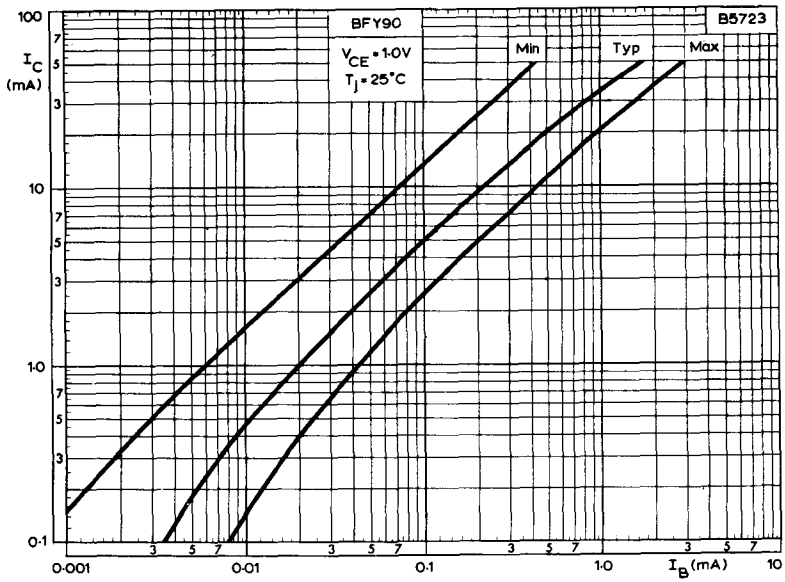
2. Transistors may be dip-soldered at a solder temperature of 245°C for a maximum soldering time of 5 seconds. The case temperature during dip-soldering must not at any time exceed the maximum storage temperature. These recommendations apply to a transistor mounted flush on a board having punched-through holes, or spaced at least 1.5mm above a board having plated-through holes.

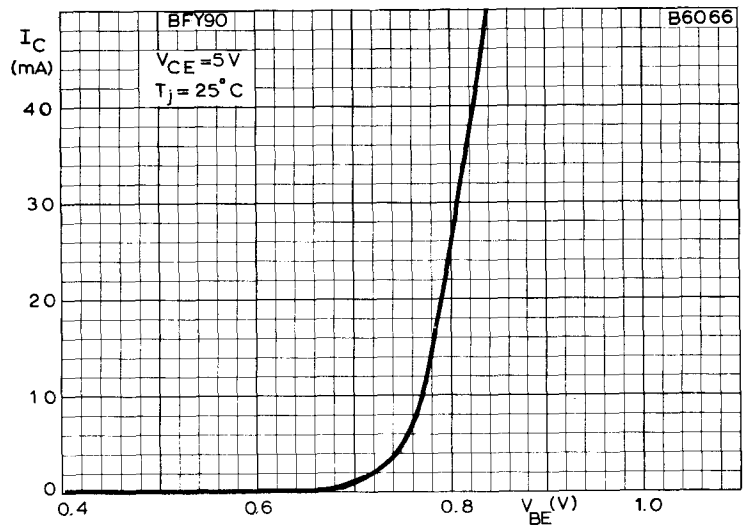
3. Care should be taken not to bend the leads nearer than 1.5mm from the seal.

4. If devices are stored above 100°C before incorporation into equipment, some deterioration of the external surface is likely to occur which may make soldering into the circuit difficult. Under these circumstances the leads should be retinned using a suitable activated flux.

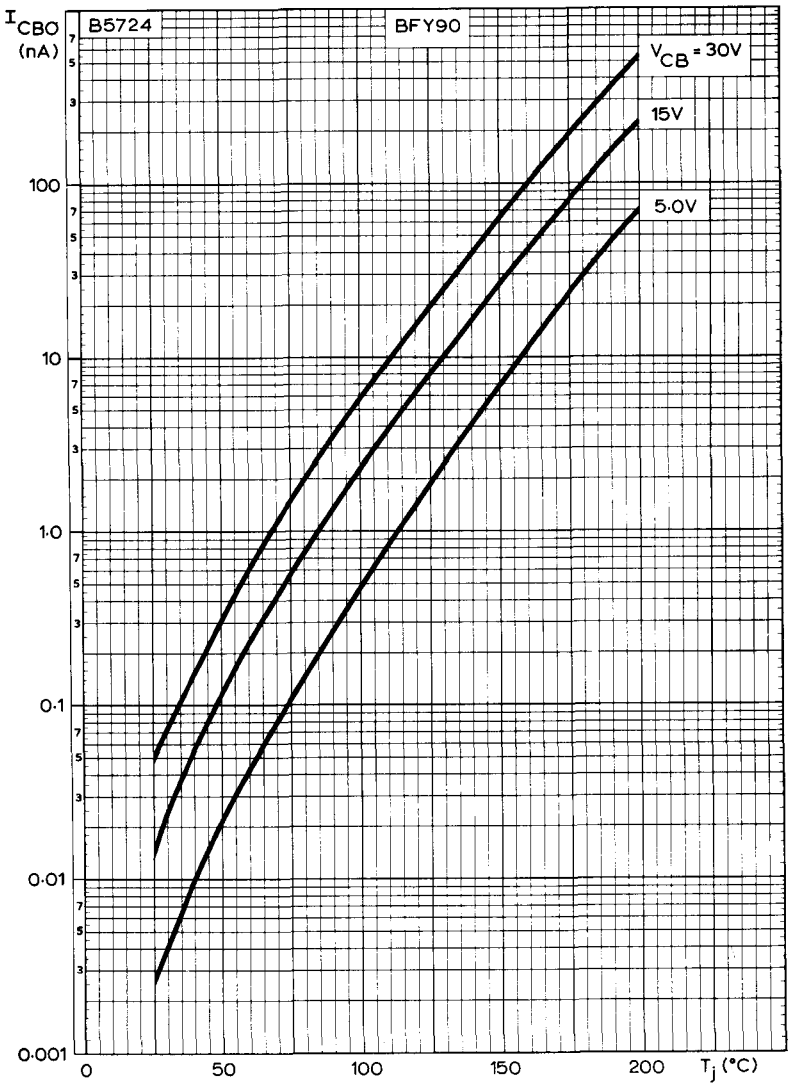


TYPICAL OUTPUT CHARACTERISTICS

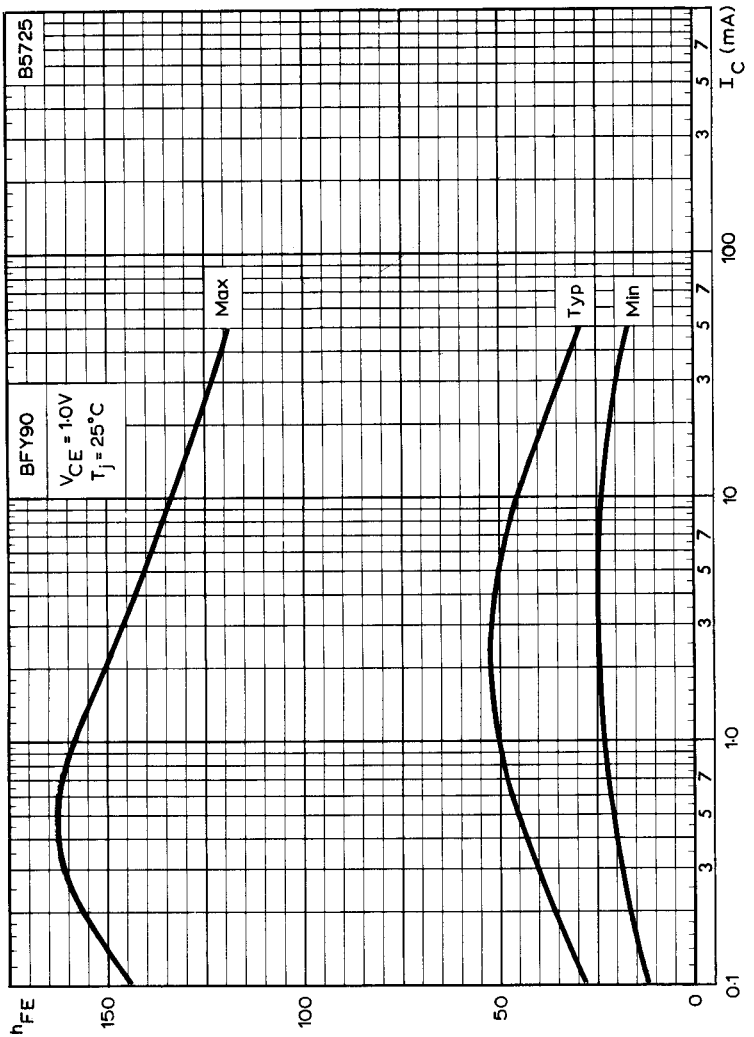




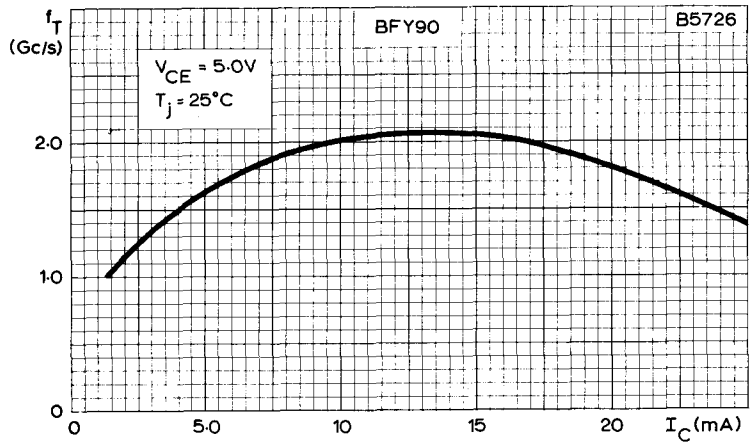
TRANSFER CHARACTERISTICS
TYPICAL INPUT CHARACTERISTIC

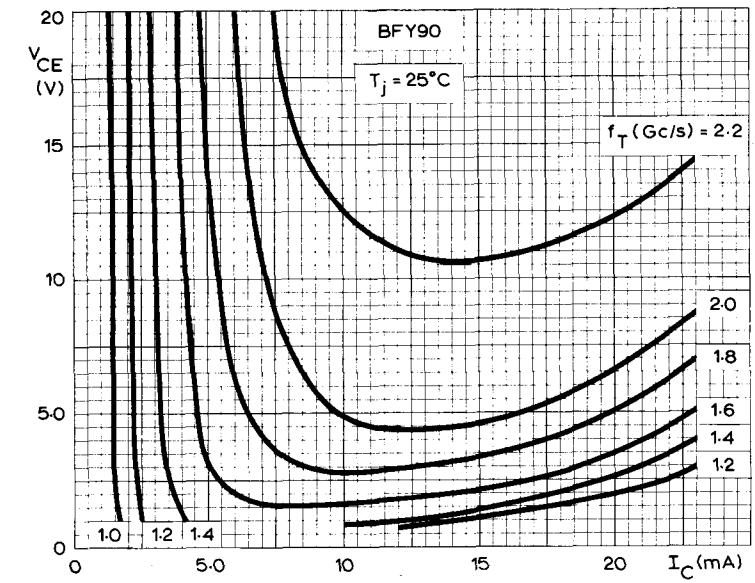


TYPICAL VARIATION OF COLLECTOR CUT-OFF CURRENT
WITH JUNCTION TEMPERATURE



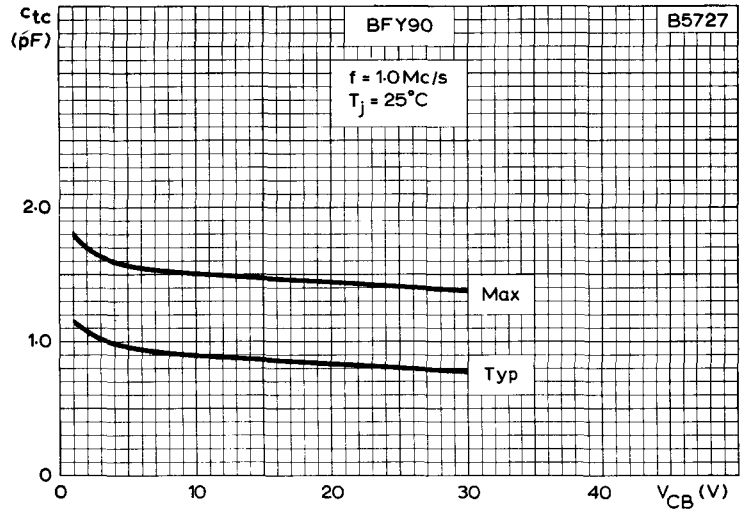
STATIC FORWARD CURRENT TRANSFER RATIO
PLOTTED AGAINST COLLECTOR CURRENT

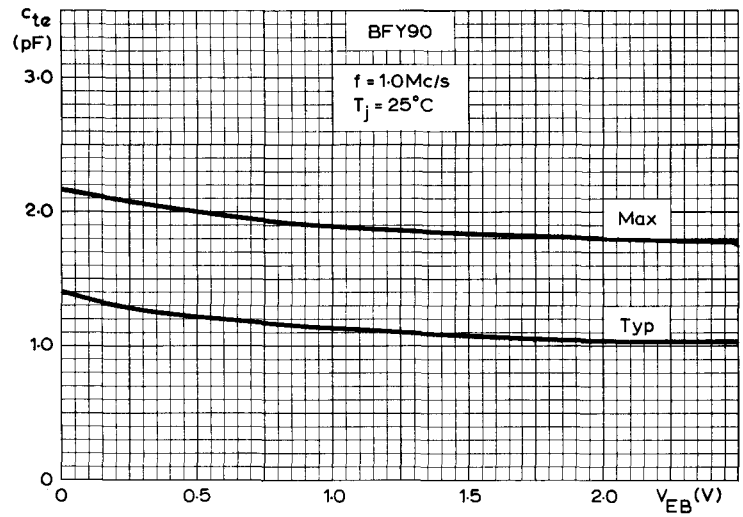




TYPICAL TRANSITION FREQUENCY PLOTTED AGAINST COLLECTOR CURRENT

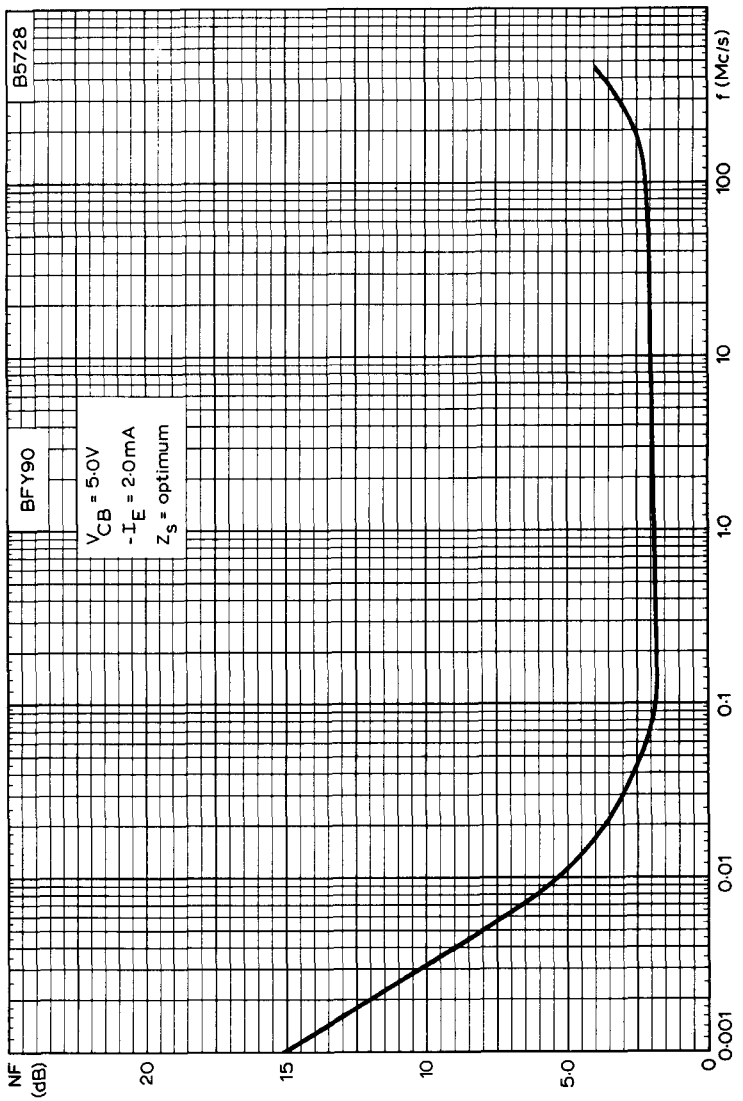
CONTOURS OF CONSTANT TRANSITION FREQUENCY



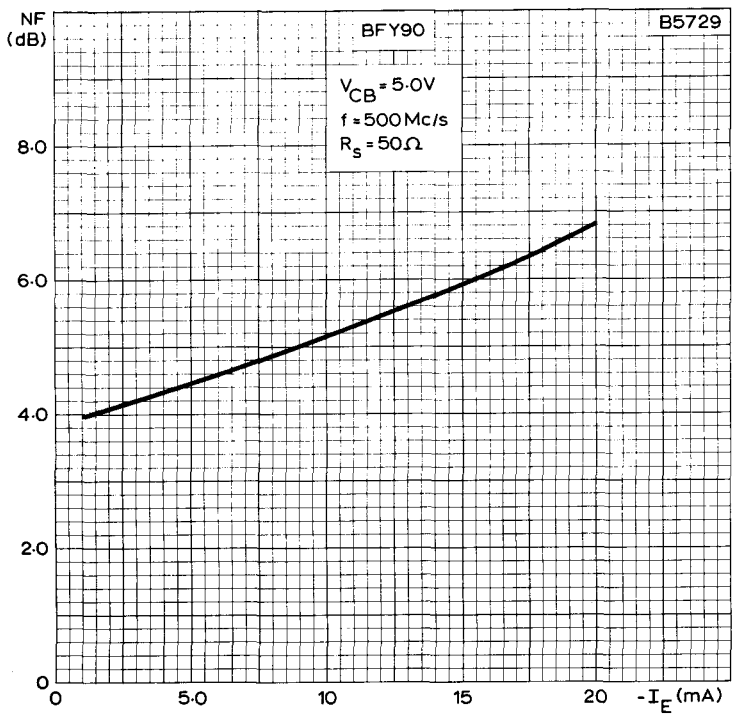


COLLECTOR CAPACITANCE PLOTTED AGAINST COLLECTOR-BASE VOLTAGE

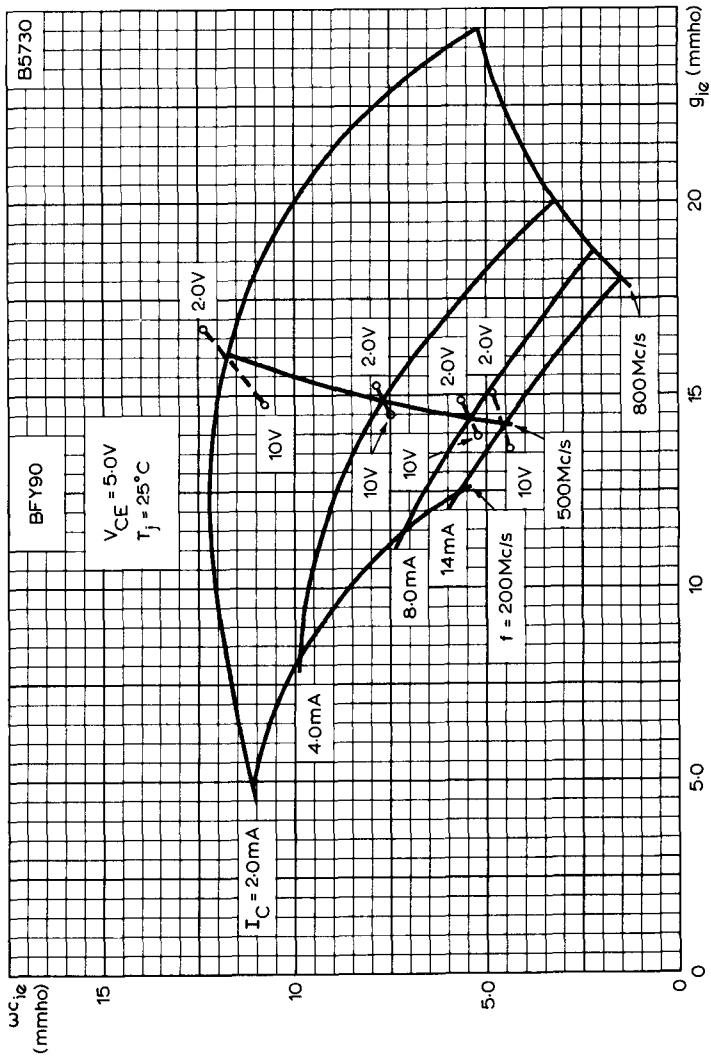
EMITTER CAPACITANCE PLOTTED AGAINST EMITTER-BASE VOLTAGE



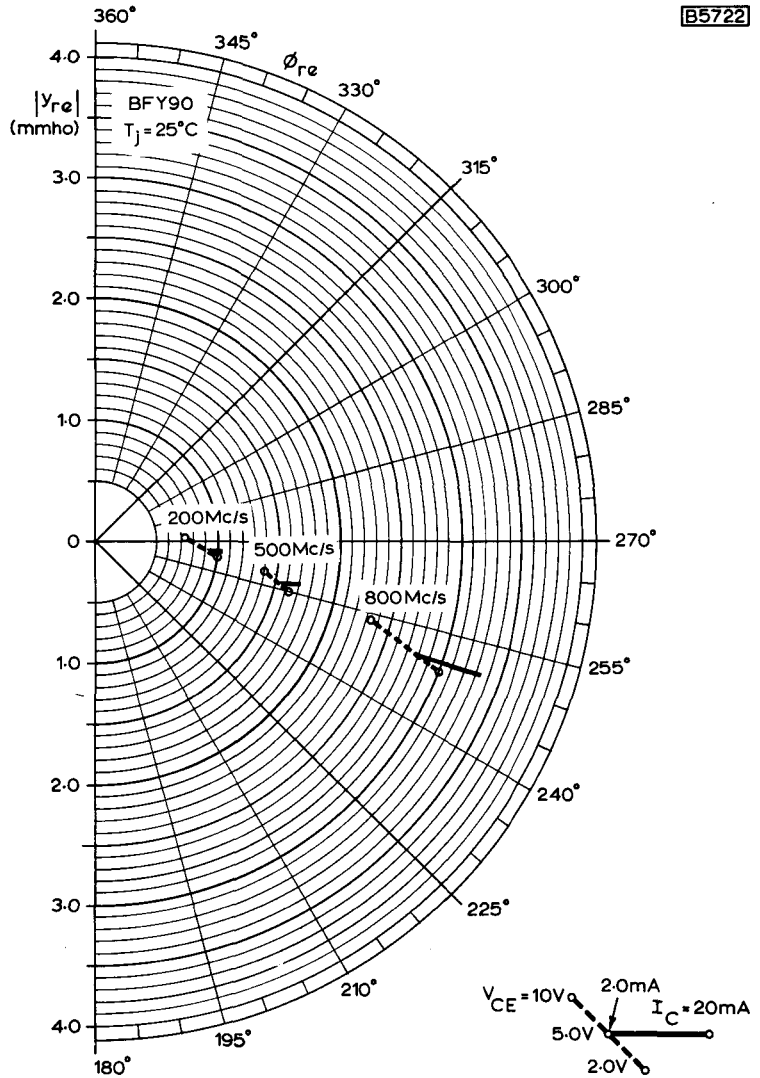
TYPICAL NOISE FIGURE PLOTTED AGAINST FREQUENCY



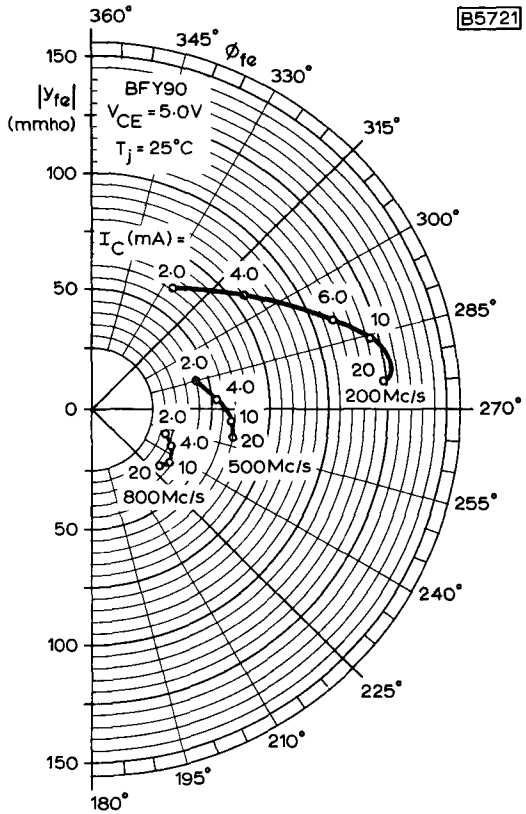
TYPICAL NOISE FIGURE PLOTTED AGAINST EMITTER CURRENT



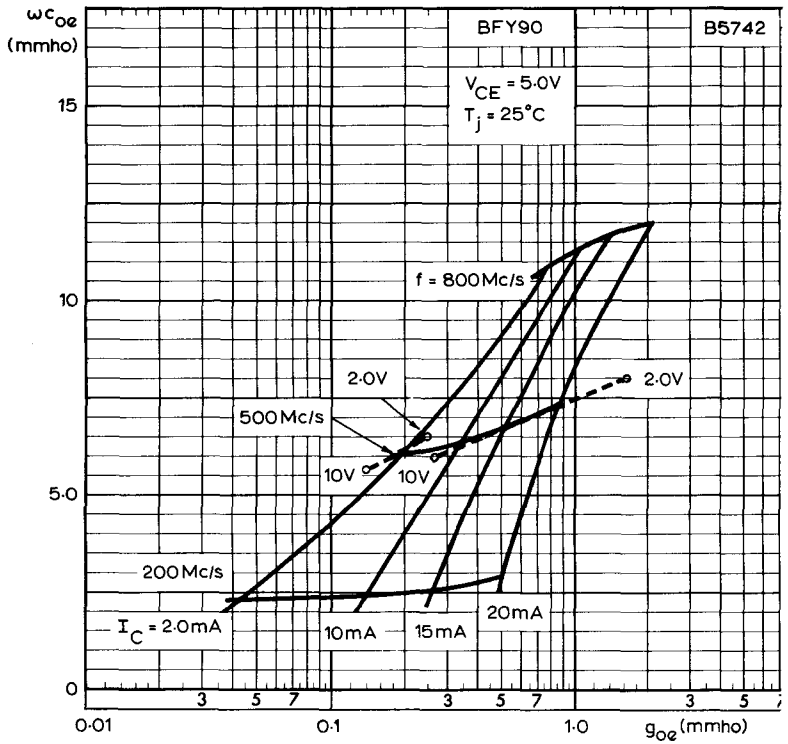
TYPICAL INPUT ADMITTANCE PLOTTED AGAINST
COLLECTOR CURRENT AND FREQUENCY



TYPICAL FEEDBACK ADMITTANCE PLOTTED AGAINST COLLECTOR CURRENT AND FREQUENCY



TYPICAL FORWARD TRANSFER ADMITTANCE PLOTTED AGAINST COLLECTOR CURRENT AND FREQUENCY



TYPICAL OUTPUT ADMITTANCE PLOTTED AGAINST COLLECTOR CURRENT AND FREQUENCY

U.H.F. POWER AMPLIFIER MODULES

BGY22
BGY22A

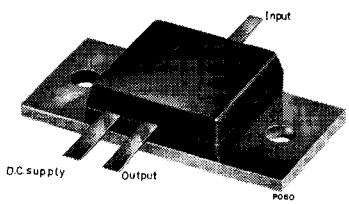
TENTATIVE DATA

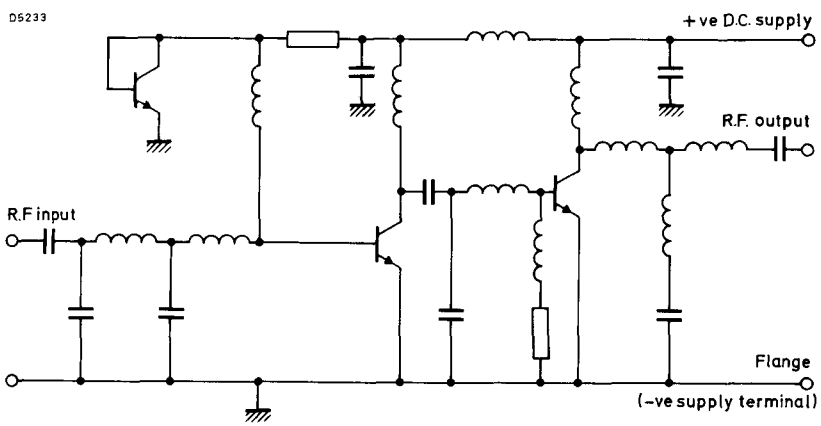
Broadband u.h.f. amplifier modules primarily designed for mobile applications operating directly from 12V vehicle electrical systems. The modules will produce 2.5W output into a 50Ω load over the bands 380-512MHz (BGY22), and 420-480MHz (BGY22A).

QUICK REFERENCE DATA

Type	Mode	Freq. range (MHz)	V_{CC} (V)	P_D (mW)	P_L (W)	η (%)	Matched input and output Z (Ω)
BGY22	f.m.	380-512	13.5	50	2.5 min.	40 min.	50
BGY22	f.m.	380-512	13.5	50	2.9 typ.	50 typ.	50
BGY22A	f.m.	420-480	12.5	50	2.5 min.	40 min.	50

Mechanical details on page 10.



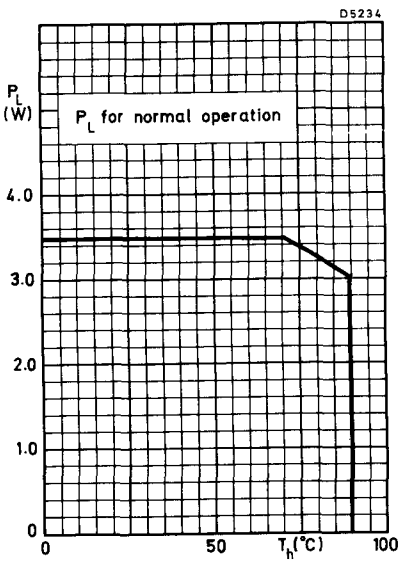


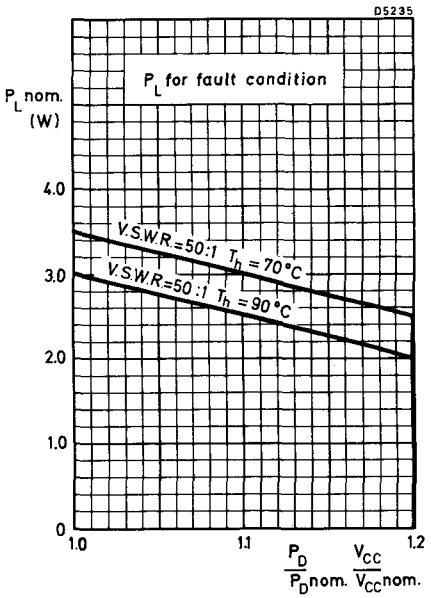
RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{CC}	max.	D.C. voltage - supply terminal to flange	18	V
V_{in}	max.	D.C. voltage - input terminal to flange	±25	V
V_{out}	max.	D.C. voltage - output terminal to flange	±25	V
I_{in}	max.	D.C. supply terminal current	800	mA
P_D	max.	V_{CC} = 13.5V, Z_L = 50Ω	150	mW





Where $P_{L\ nom}$ = P_L at V_{CC} = 13.5V, Z_L = 50Ω (BGY22),
and $P_{L\ nom}$ = P_L at V_{CC} = 12.5V, Z_L = 50Ω (BGY22A).

OPERATING CHARACTERISTICS (At $T_h = 25^oC$ unless otherwise stated)

Reference planes at RF input and output terminals are 1mm from the plastic encapsulation.

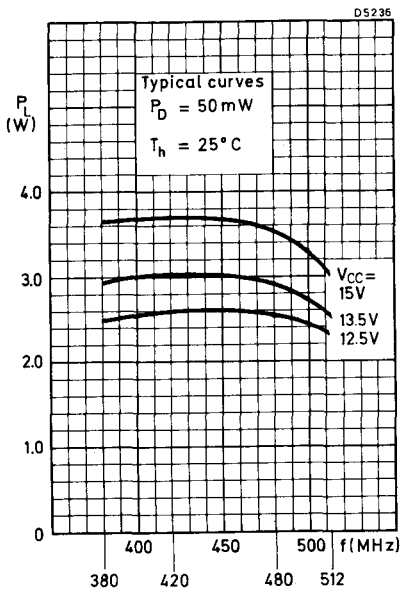
Frequency range 380 - 512MHz, V_{CC} = 13.5V (BGY22)

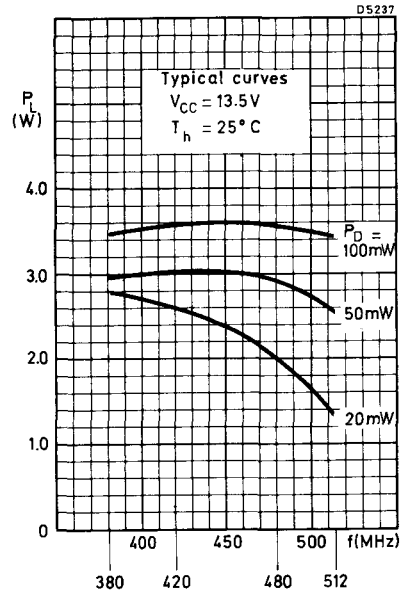
Frequency range 420 - 480MHz, V_{CC} = 12.5V (BGY22A)

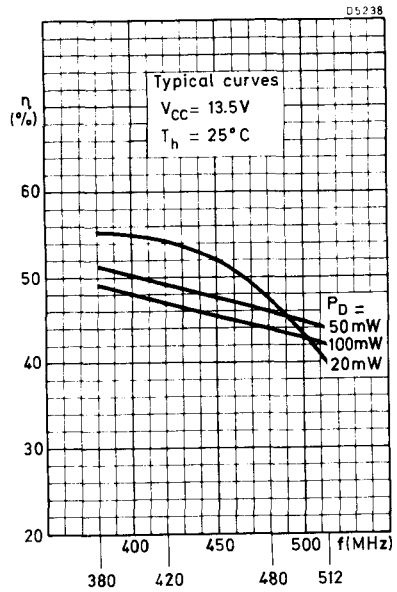
		Min.	Typ.	Max.	
I_Q	Quiescent current				
	$P_D = 0$	4.0	-	12	mA
P_L	Load power				
	P_D = 50mW	2.5	-	3.5	W
η	Efficiency				
	P_D = 50mW	40	-	-	%
I_{in}	Module current				
	P_D = 50mW	-	475	-	mA
	Harmonic content				
	P_D = 50mW	Any harmonic is at least 20dB down relative to carrier			
	Input V.S.W.R. with respect to 50Ω				
	P_D = 50mW	-	-	2:1	
	Temperature coefficient of P_L				
	P_D = 50mW, T_h = 25 to 70°C	-	-10	-	mW/°C
	Stability				
	V_{CC} = 10.5 to 15V, P_D = 10mW to 100mW				
	T_h = -40 to +90°C				
	Output load V.S.W.R. ≤3:1, all phases	No instabilities			
	Output load V.S.W.R. ≤10:1, all phases	No appreciable instabilities			

THERMAL CHARACTERISTICS

T_{stg} range	-40 to +100	°C
T_h range	-40 to +90	°C


D5236
Typical curves
P_D = 50 mW
T_h = 25°C
P_L (W)
4.0
3.0
2.0
1.0
0
V_{CC} = 15V
13.5V
12.5V
400
450
500
f(MHz)
380
420
480
512


D5237
Typical curves
V_{CC} = 13.5V
T_h = 25°C
P_L (W)
4.0
3.0
2.0
1.0
0
P_D = 100mW
50mW
20mW
400
450
500
f(MHz)
380
420
480
512


D5238
Typical curves
V_{CC} = 13.5V
T_h = 25°C
η (%)
60
50
40
30
20
P_D = 50mW
100mW
20mW
400
450
500
f(MHz)
380
420
480
512

APPLICATION INFORMATION

R. F. performance in c. w. operation, $T_h = 25^oC$.

Drive source and Load Impedance = 50Ω.

Type	Freq. range (MHz)	V_{CC} (V)	P_D (mW)	P_L (W)	η (%)
BGY22	380-512	15	50	3.5 typ.	47 typ.
BGY22	380-512	13.5	50	2.5 min.	40 min.
BGY22	380-512	13.5	50	2.9 typ.	47 typ.
BGY22	380-512	12.5	50	2.5 typ.	47 typ.
BGY22A	420-480	12.5	50	2.5 min.	40 min.

The modules are designed to withstand full load mismatch under the following conditions.

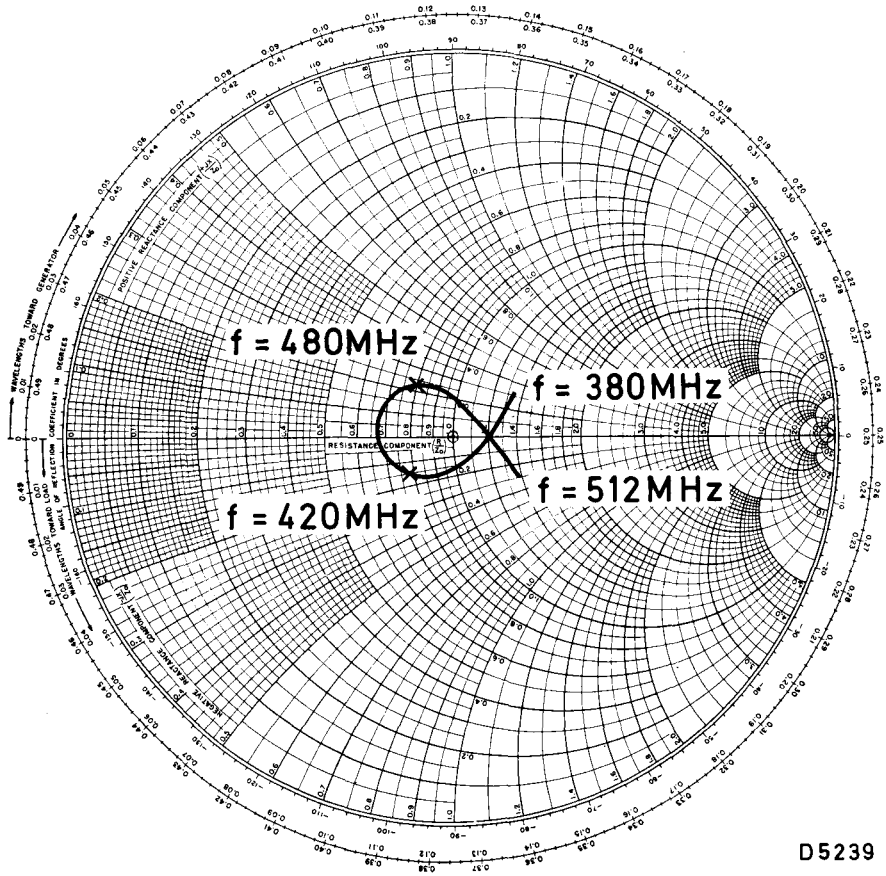
$P_D = P_D$ nom + 20%, $T_h = 70^oC$,

$V_{CC} = 16.5V$ (BGY22)

$V_{CC} = 15.0V$ (BGY22A)

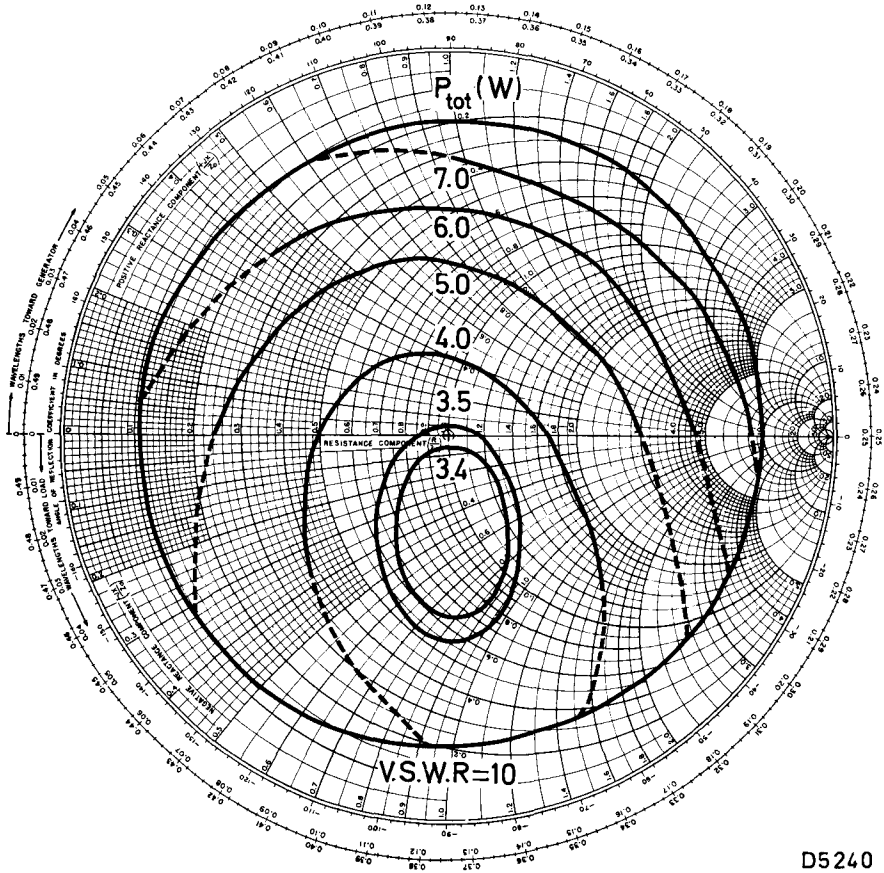
V.S.W.R. = 50: 1 at any phase

where P_D nom = P_D for 2.5W module output under nominal conditions.



TYPICAL VARIATION OF INPUT IMPEDANCE WITH FREQUENCY

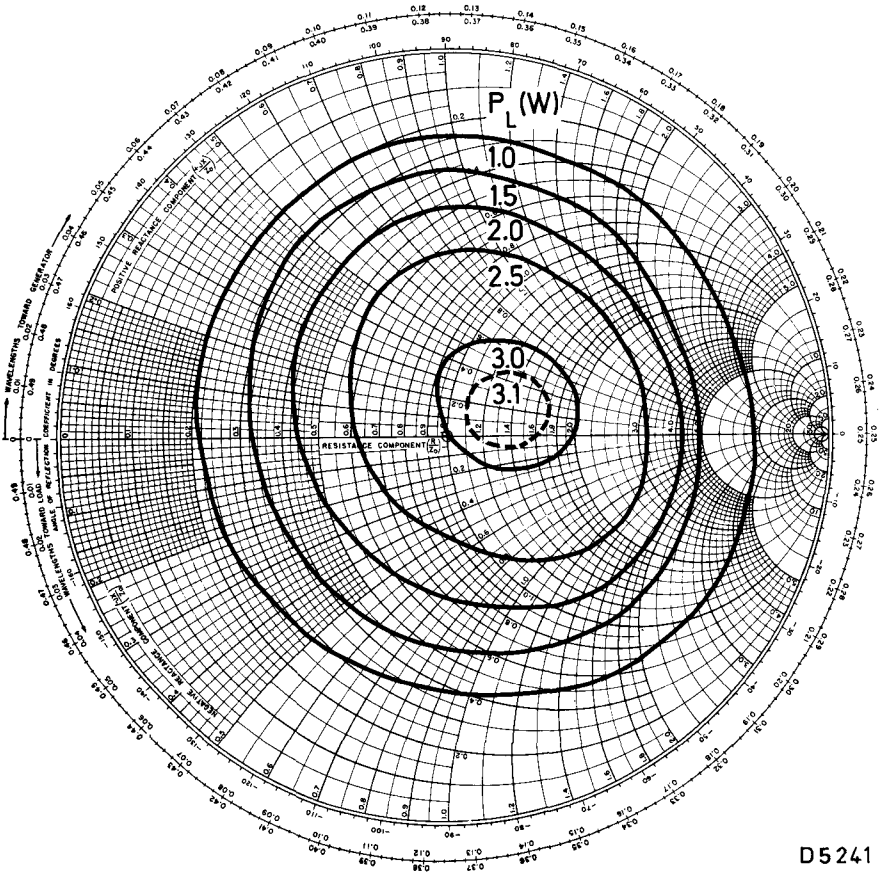
APPLICATION INFORMATION (Cont'd)



TYPICAL VARIATION OF POWER DISSIPATION WITH LOAD IMPEDANCE

f = 470MHz

V_{CC} = 13.5V



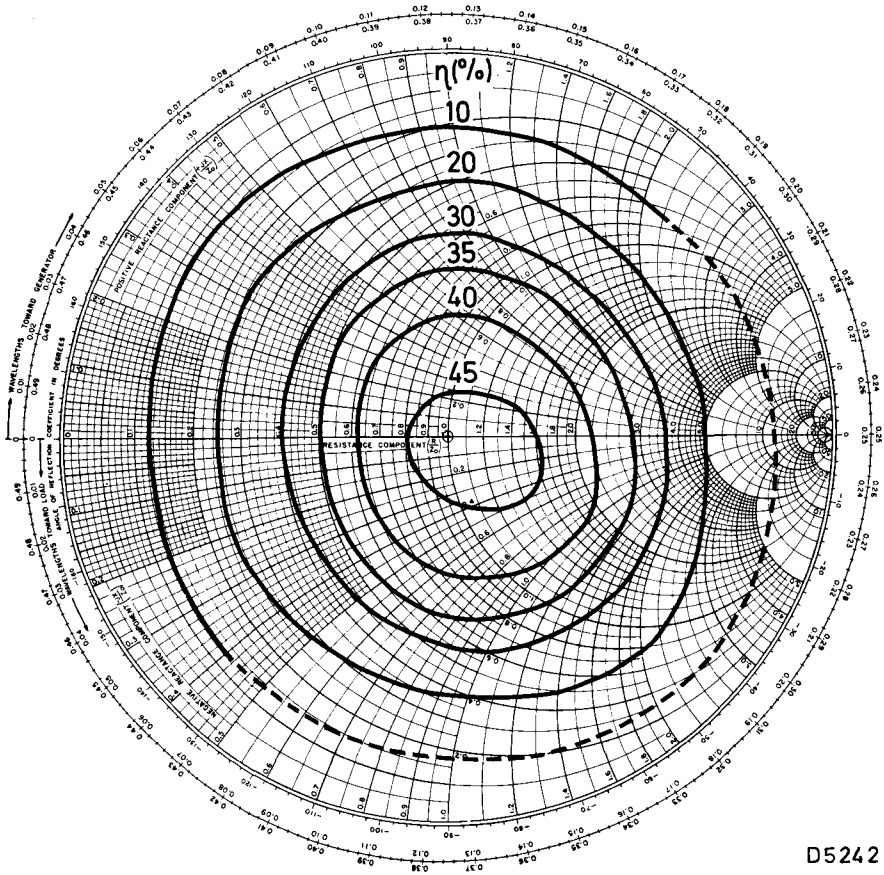
TYPICAL VARIATION OF LOAD POWER WITH LOAD IMPEDANCE

P_D = 50mW

f = 470MHz

V_{CC} = 13.5V

APPLICATION INFORMATION (Cont'd)



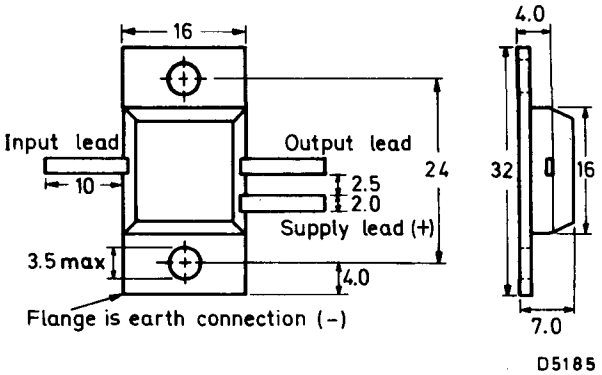
TYPICAL VARIATION OF EFFICIENCY WITH LOAD IMPEDANCE

P_D = 50mW

f = 470MHz

V_{CC} = 13.5V

OUTLINE AND DIMENSIONS



All dimensions in millimetres

MOUNTING

To ensure good thermal contact between mountingbase and heatsink, burrs or thickening at the edges of the heatsink holes should be removed and the package bolted down onto a flat surface.

Devices may be soldered directly into a circuit with a soldering iron at a maximum iron temperature of 245°C for 10 seconds at least 1mm from the plastic.

CAUTION

This device incorporates Beryllium Oxide, the dust of which is toxic. The device is entirely safe provided that it is not dismantled.

Care should be taken to ensure that all those who may handle, use or dispose of this device are aware of its nature and of the necessary safety precautions. In particular, it should never be thrown out with general industrial or domestic waste.

DISPOSAL SERVICE

Devices requiring disposal may be returned to the Mullard Service Department. They must be separately and securely packed and clearly identified. If any are damaged or broken they MUST NOT be sent through the post. In this case, advice is available from:

THE SERVICE DEPARTMENT
MULLARD LIMITED
P.O. BOX 142
NEW ROAD
MITCHAM
SURREY, CR4 4SR

U.H.F. POWER AMPLIFIER MODULES

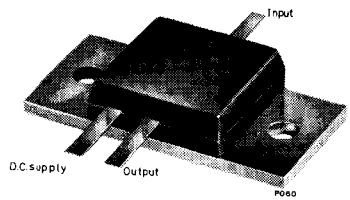
BGY23
BGY23A

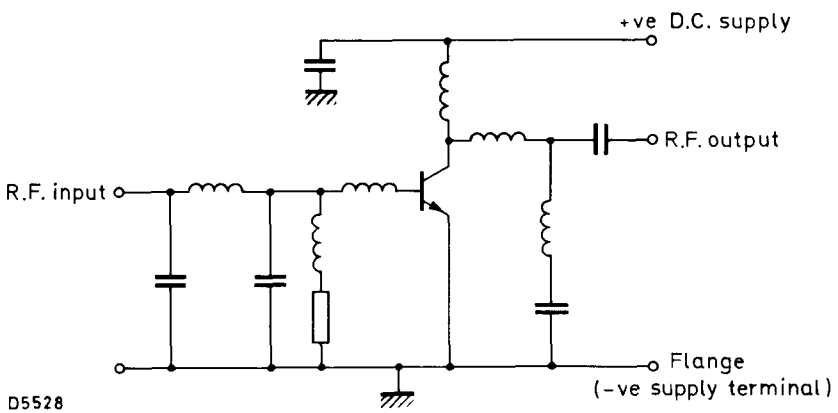
TENTATIVE DATA

Broadband u.h.f. amplifier modules primarily designed for mobile applications operating directly from 12V vehicle systems. The modules are suitable for driving directly from the BGY22 and BGY22A respectively, and when so driven will produce 7W output into a 50Ω load over the band 380-480MHz (BGY23), and 7W over the band 420-480MHz (BGY23A).

QUICK REFERENCE DATA							
Type	Mode	Freq. range (MHz)	V_{CC} (V)	P_D (W)	P_L (W)	η (%)	Matched input and output Z (Ω)
BGY23	f.m.	380-480	13.5	2.5	7.0 min.	60 min.	50
BGY23	f.m.	380-480	13.5	2.5	8.3 typ.	71 typ.	50
BGY23	f.m.	480-512	13.5	2.5	7.5 typ.	69 typ.	50
BGY23A	f.m.	420-480	12.5	2.5	7.0 min.	60 min.	50

Mechanical details on page 10



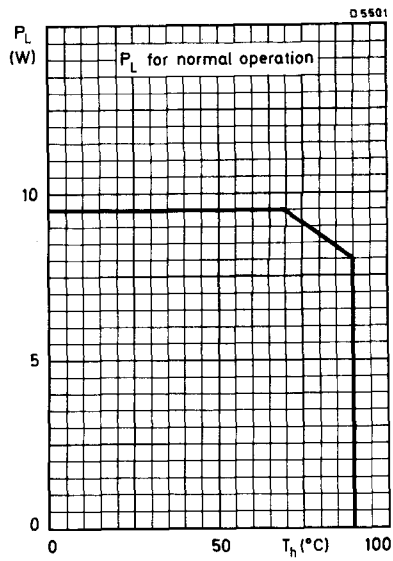


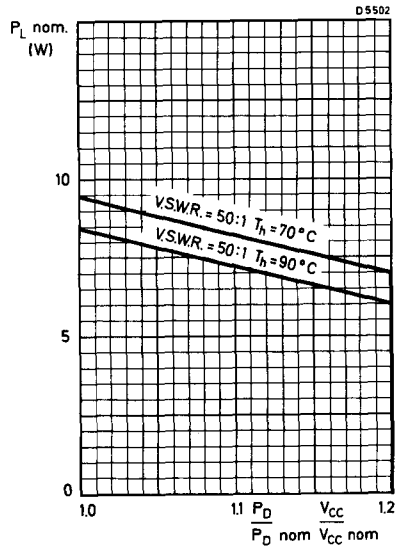
RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{CC}	max.	D.C. voltage - supply terminal to flange	18	V
*V_{in}	max.	D.C. voltage - input terminal to flange	± 0.5	V
V_{out}	max.	D.C. voltage - output terminal to flange	± 25	V
I_{in}	max.	D.C. supply terminal current	1.7	A
P_D	max.	V_{CC} = 13.5V, Z_L = 50Ω	3.5	W





Where P_L nom. = P_L at V_{CC} = 13.5V, Z_L = 50Ω (BGY23)

and P_L nom. = P_L at V_{CC} = 12.5V, Z_L = 50Ω (BGY23A)

*No external D.C. connection should be made to this terminal.

OPERATING CHARACTERISTICS (At $T_h = 25^o$ unless otherwise stated.)

Reference planes at RF input and output terminals are 1mm from the plastic encapsulation.

Frequency range 380 - 512 MHz, V_{CC} = 13.5V (BGY23)

Frequency range 420 - 480 MHz, V_{CC} = 12.5V (BGY23A)

			Min.	Typ.	Max.	
I_Q	Quiescent Current $P_D = 0$		-	-	5.0	mA
P_L	Load Power P_D = 2.5W, f = 380-480MHz	BGY 23	7.0	-	9.5	W
	P_D = 2.5W, f = 480-512MHz	BGY 23	-	7.5	-	W
	P_D = 2.5W, f = 420-480MHz	BGY 23A	7.0	-	9.5	W
η	Efficiency P_D = 2.5W		60	-	-	%
I_{in}	Module Current P_D = 2.5W		-	900	-	mA
Harmonic Content P_D = 2.5W					Any harmonic is at least 20dB down relative to carrier.	
Input V.S.W.R. with respect to 50Ω P_D = 2.5W			-	-	2: 1	
Temperature coefficient of P_L P_D = 2.5W, $T_h = 25^oC$ to 70^oC			-	−20	-	mW/^{o}C

Stability

V_{CC} = 10.5 to 15V, P_D = 1.0 to 3.5W

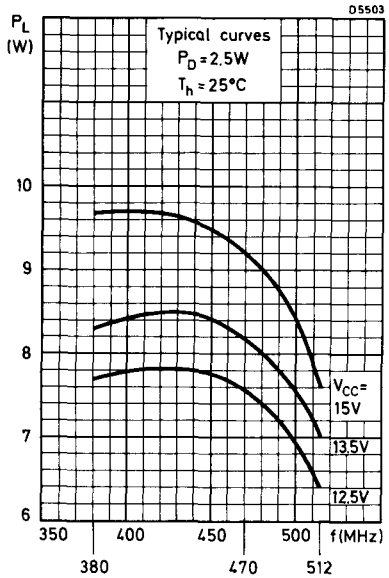
T_h = -40 to +90^{o}C

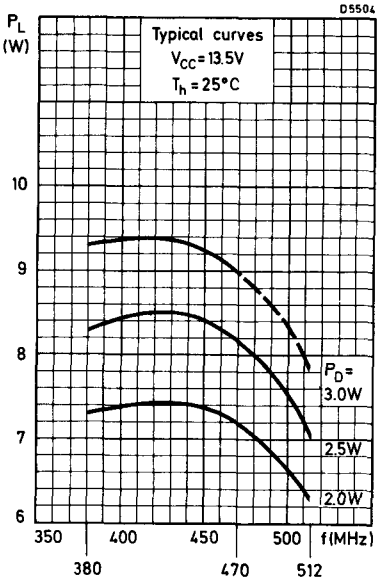
Output load V.S.W.R. ≤ 3: 1, all phases — No instabilities

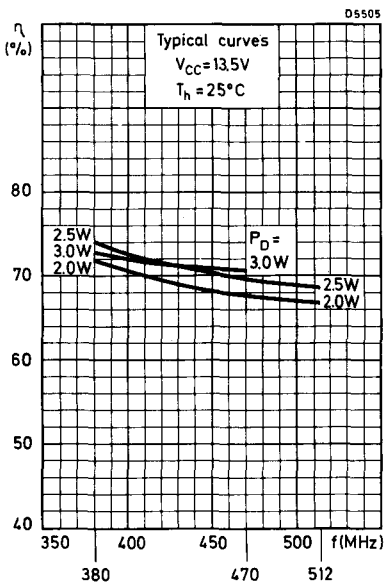
Output load V.S.W.R. ≤ 10: 1, all phases — No appreciable instabilities

THERMAL CHARACTERISTICS

T_{stg} range	-40 to +100	^{o}C
T_h range	-40 to +90	^{o}C


D5503
P_L (W)
Typical curves
P_D = 2.5W
T_h = 25°C
10
9
8
7
6
V_{CC}= 15V
13.5V
12.5V
350
400
450
500
f(MHz)
380
470
512


D5504
P_L (W)
Typical curves
V_{CC} = 13.5V
T_h = 25°C
10
9
8
7
6
P_D= 3.0W
2.5W
2.0W
350
400
450
500
f(MHz)
380
470
512


D5505
η (%)
Typical curves
V_{CC} = 13.5V
T_h = 25°C
80
70
60
50
40
2.5W
3.0W
2.0W
P_D= 3.0W
2.5W
2.0W
350
400
450
500
f(MHz)
380
470
512

APPLICATION INFORMATION

R. F. performance in c. w. operation, $T_h = 25^oC$

Drive Source and Load Impedance = 50Ω

Type	freq. range (MHz)	V_{CC} (V)	P_D (W)	P_L (W)	η (%)
BGY23	380-512	15.0	2.5	9.0 typ.	65 typ.
BGY23	380-480	13.5	2.5	7.0 min.	60 min.
BGY23	380-480	13.5	2.5	8.3 typ.	71 typ.
BGY23	480-512	13.5	2.5	7.5 typ.	69 typ.
BGY23	380-512	12.5	2.5	7.4 typ.	70 typ.
BGY23A	420-480	12.5	2.5	7.0 min.	60 min.

Connection to the BGY22/BGY22A respectively can be either by 50Ω transmission line or directly with a total lead length not greater than 2mm.

The module is designed to withstand full load mis-match under the following conditions:

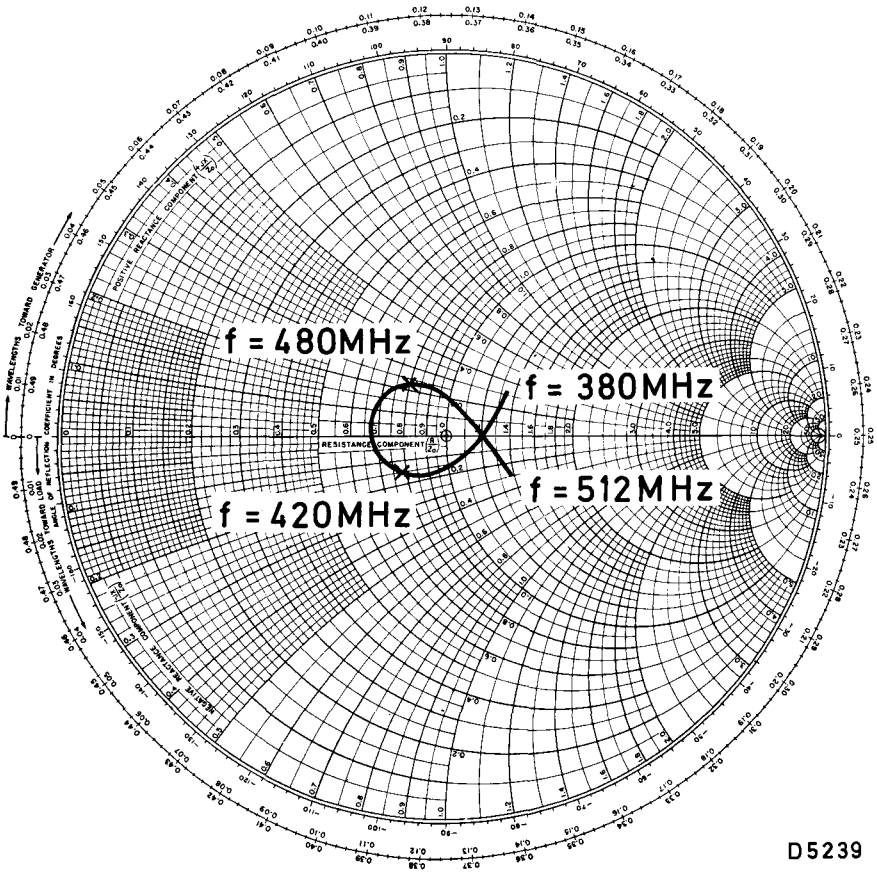
$P_D = P_D$ nom + 20%, $T_h = 70^oC$

$V_{CC} = 16.5V$ (BGY23)

$V_{CC} = 15.0V$ (BGY23A)

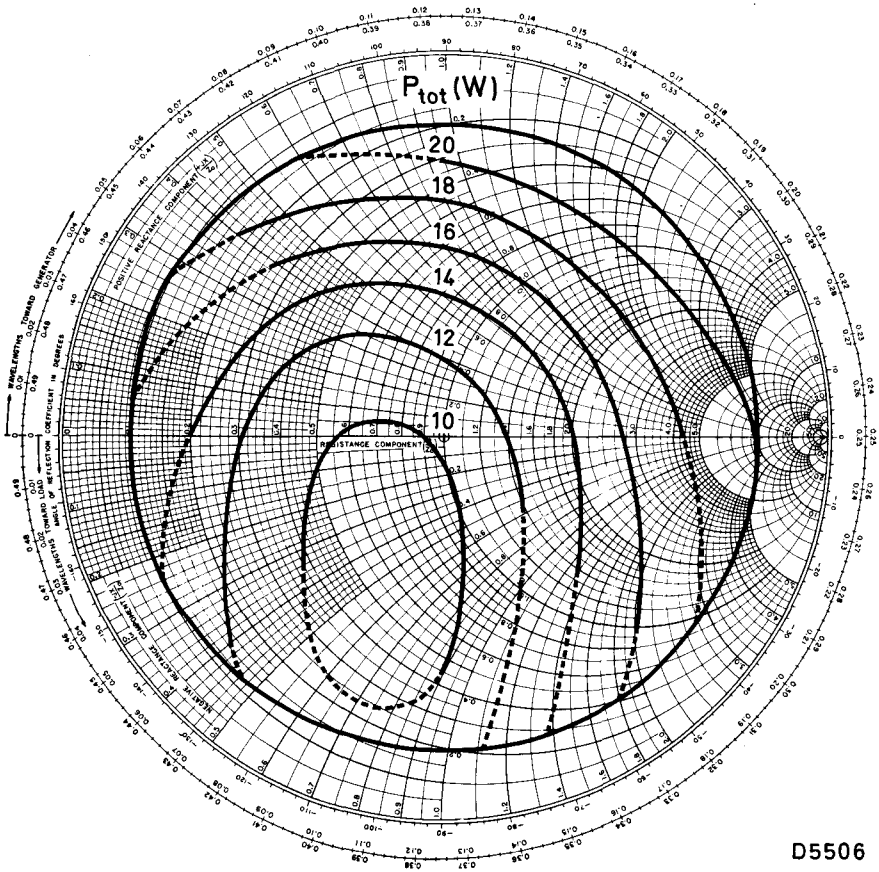
V.S.W.R. = 50: 1 at any phase.

where P_D nom = P_D for 7.0W module output under nominal conditions.



TYPICAL VARIATION OF INPUT IMPEDANCE WITH FREQUENCY

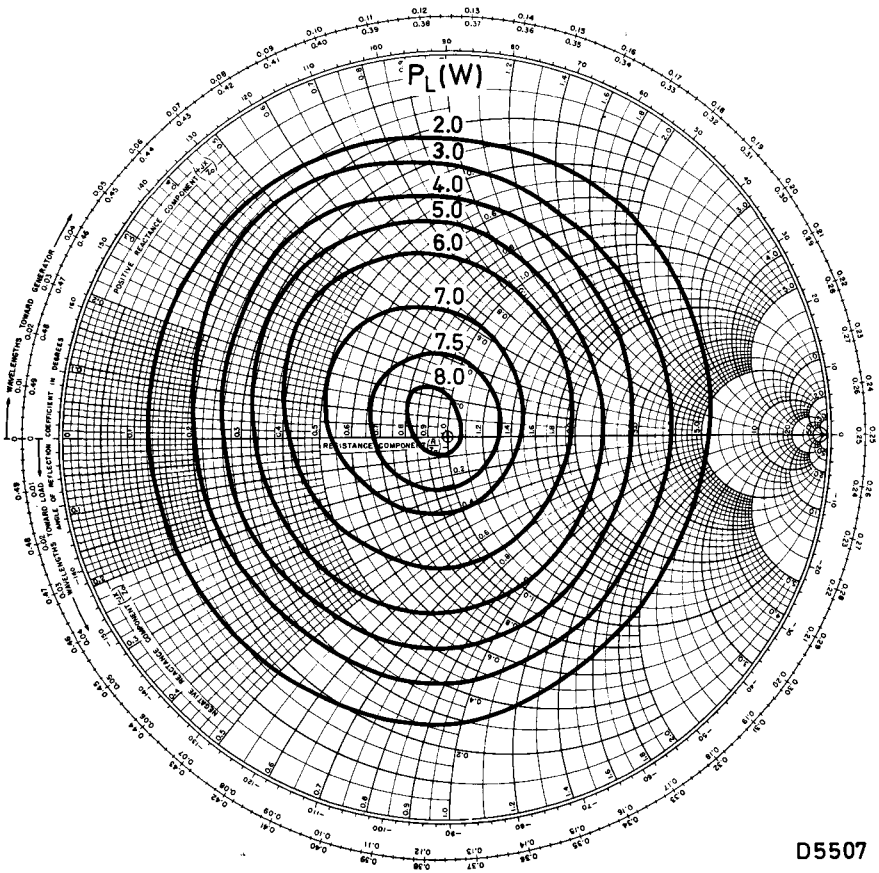
APPLICATION INFORMATION (Cont'd)



BGY22/23 or BGY22A/23A CASCADED AMPLIFIER AT 470 MHz

TYPICAL VARIATION OF OVERALL POWER DISSIPATION WITH LOAD IMPEDANCE

V_{CC} = 13.5V

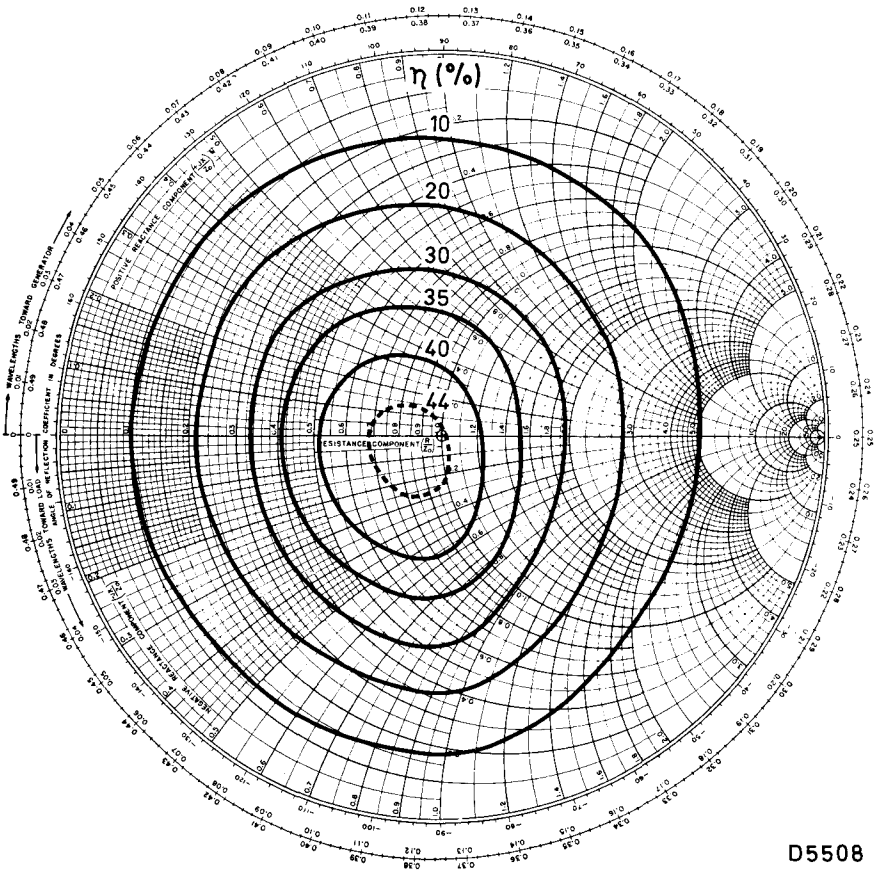


BGY22/23 or BGY22A/23A CASCADED AMPLIFIER AT 470 MHz

TYPICAL VARIATION OF LOAD POWER WITH LOAD IMPEDANCE

V_{CC} = 13.5V

APPLICATION INFORMATION (Cont' d)

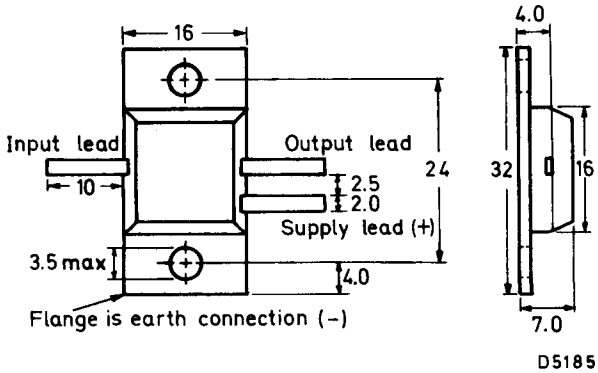


BGY22/23 or BGY22A/23A CASCADED AMPLIFIER AT 470 MHz

TYPICAL VARIATION OF OVERALL EFFICIENCY WITH LOAD IMPEDANCE

V_{CC} = 13.5V

OUTLINE AND DIMENSIONS



All dimensions in millimetres

MOUNTING

To ensure good thermal contact between mountingbase and heatsink, burrs or thickening at the edges of the heatsink holes should be removed and the package bolted down onto a flat surface.

Devices may be soldered directly into a circuit with a soldering iron at a maximum iron temperature of 245°C for 10 seconds at least 1mm from the plastic.

CAUTION

This device incorporated Beryllium Oxide, the dust of which is toxic. The device is entirely safe provided that it is not dismantled.

Care should be taken to ensure that all those who may handle, use or dispose of this device are aware of its nature and of the necessary safety precautions. In particular, it should never be thrown out with general industrial or domestic waste.

DISPOSAL SERVICE

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THE SERVICE DEPARTMENT
MULLARD LIMITED
P.O. BOX 142
NEW ROAD
MITCHAM
SURREY, CR4 4SR

N-P-N SILICON PLANAR EPITAXIAL V.H.F. TRANSISTOR

BLX13

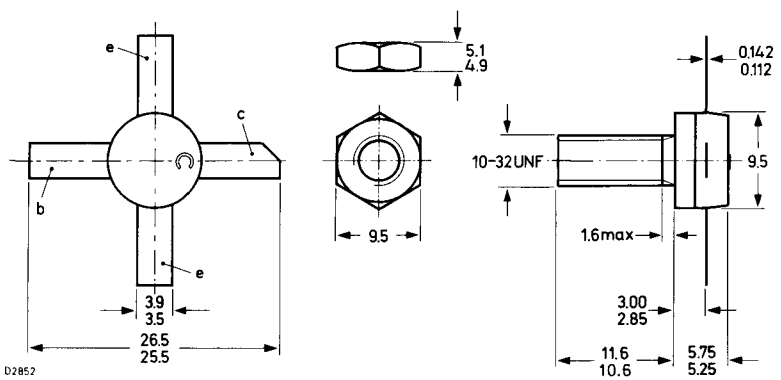
N-P-N silicon planar epitaxial transistor intended for s.s.b. in class A and AB and f.m. transmitting applications in class B with a supply voltage up to 28V. The transistor is designed to withstand severe load mismatch conditions. It has a capstan envelope with a moulded cap and all leads isolated from the stud.

QUICK REFERENCE DATA

Operation	Class	V_{CC} (V)	f_1 (MHz)	f_2 (MHz)	P_L (W)	G_p (dB)	d_3 (dB)	I_C (A)	dt (%)
s.s.b.	A	26	28.000	28.001	0-8(P.E.P.)	> 18	< -40	1.2	-
s.s.b.	AB	28	28.000	28.001	25(P.E.P.)	> 18	typ. -35	typ. 1.28	typ. 35

Operation	Class	V_{CC} (V)	f (MHz)	P_S (W)	P_L (W)	G_p (dB)	I_C (A)	η (%)	$\overline{z_i}$ (Ω)	$\overline{Y_L}$ (mA/V)
c.w.	B	28	70	typ. 0.5	25	typ. 17	typ. 1.49	typ. 60	0.53-j1.4	42.5-j54

OUTLINE AND DIMENSIONS



All dimensions in mm

Torque on nut: min. 15kg cm (1.5N m)
max. 17kg cm (1.7N m)

Diameter of clearance hole in heatsink: max. 5mm

Note: - Do not chamfer the edges of the mounting holes when removing burrs.

RATINGS

Limiting values of operation according to the absolute maximum system

Electrical

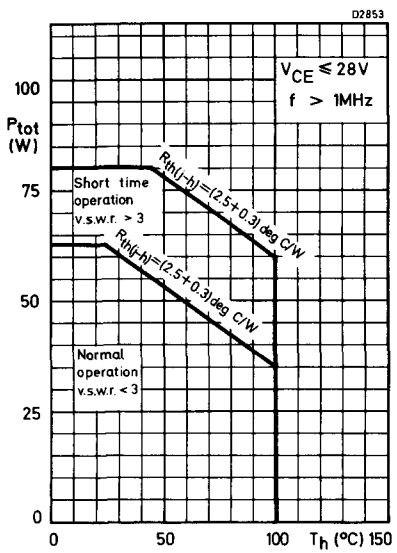
V_{CBOM} max.	65	V
V_{CEO} max.	36	V
V_{EBO} max.	4.0	V
$I_{C(AV)}$ max.	3.0	A
I_{CM} max. (f > 1MHz)	6.0	A
P_{tot} max. (T_h = 25°C, f > 1MHz)	62.5	W

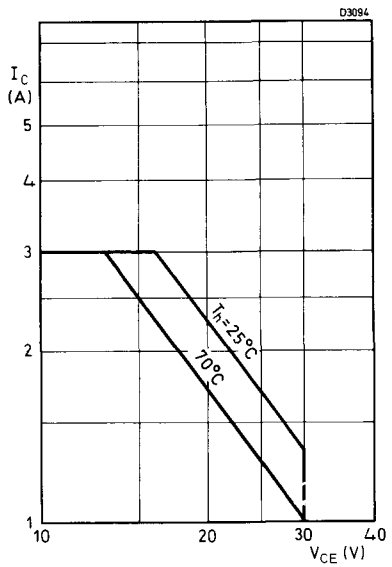
Temperature

T_{stg}	-30 to +200	°C
T_j max.	200	°C

THERMAL CHARACTERISTIC

$R_{th(j-mb)}$	2.5	degC/W
$R_{th(mb-h)}$	0.3	degC/W

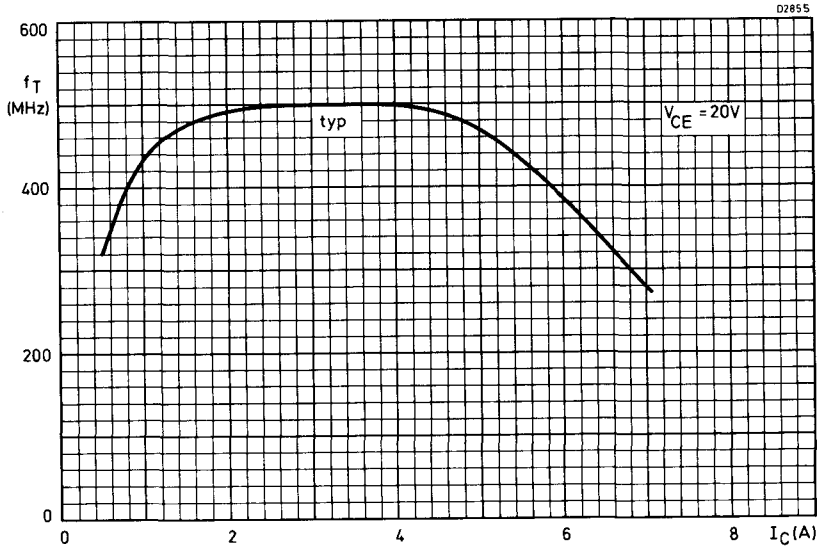


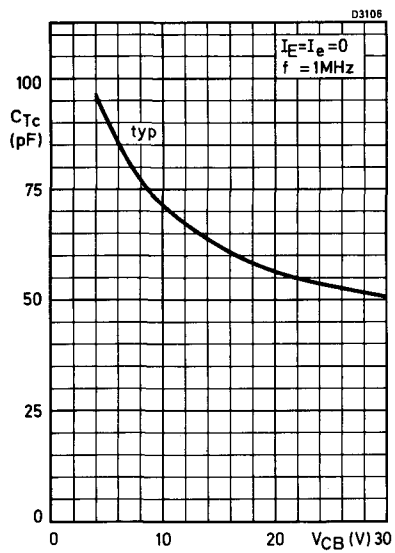


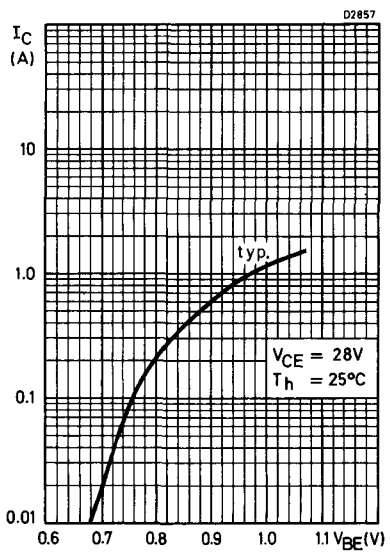
SAFE OPERATING AREAS

ELECTRICAL CHARACTERISTICS (T_j = 25°C unless otherwise stated)

		Min.	Typ.	Max.	
$V_{(BR)CBO}$	Collector-base breakdown voltage I_C = 50mA, open emitter	65	-	-	V
$V_{(BR)CEO}$	Collector-emitter breakdown voltage I_C = 50mA, open base	36	-	-	V
$V_{(BR)EBO}$	Emitter-base breakdown voltage I_E = 10mA, open collector	4.0	-	-	V
E	Transient energy L = 25mH, f = 50Hz				
	open base	8.0	-	-	mWs
	$-V_{BE}$ = 1.5V, R_{BE} = 33Ω	8.0	-	-	mWs
h_{FE}	Static forward current transfer ratio I_C = 1.0A, V_{CE} = 5V	10	50	100	
f_T	Transition frequency I_C = 3.0A, V_{CE} = 20V	-	500	-	MHz
C_{Tc}	Collector capacitance $I_E = I_e$ = 0, V_{CB} = 30V, f = 1MHz	-	50	65	pF
$-C_{re}$	Feedback capacitance I_C = 100mA, V_{CE} = 28V	-	31	-	pF
C_{cs}	Collector-stud capacitance	-	2.0	-	pF


D2855
600
f_T (MHz)
400
200
0
typ
V_{CE} = 20V
0
2
4
6
8
I_C(A)


D3106
$I_E = I_e = 0$
f = 1MHz
100
C_{Tc} (pF)
75
50
25
0
typ
0
10
20
V_{CB} (V) 30


D2857
I_C (A)
10
1.0
0.1
0.01
typ.
V_{CE} = 28V
T_h = 25°C
0.6
0.7
0.8
0.9
1.0
1.1 V_{BE}(V)

N-P-N SILICON PLANAR EPITAXIAL V.H.F. TRANSISTOR

BLX13

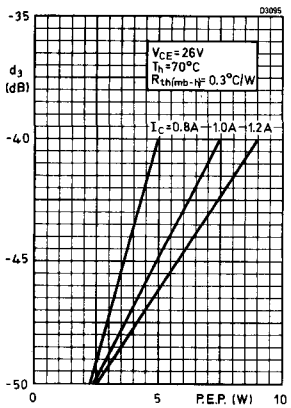
APPLICATION INFORMATION

R.F. performance in S.S.B. operation (linear power amplifier)

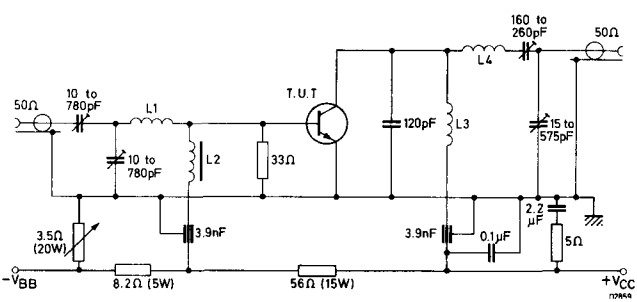
f_1 = 28.000MHz, f_2 = 28.001MHz

V_{CC} (V)	P_L (W)	G_p (dB)	$*d_3$ (dB)	I_C (A)	T_h (°C)	Class
26	0-8(P.E.P.)	>18	<-40	1.2	≤ 25	A

*The figure given is the maximum encountered at any driving level between the specified values of P.E.P. and is referred to the according level of either of the equal amplified tones. Relative to the according peak envelope power this figure should be increased by 6dB.



Test circuit: Class A



L1 = 3 turns of enamelled copper wire (1.5mm); winding pitch 2.5mm; int. dia. 7mm, leads 50mm (total).
L2 = 7 turns of enamelled copper wire (0.7mm); 60µH.
L3 = 4 turns of enamelled copper wire (1.5mm); winding pitch 2.5mm; int. dia. 10mm.
L4 = 7 turns of enamelled copper wire (1.5mm); winding pitch 2.5mm; int. dia. 12mm.

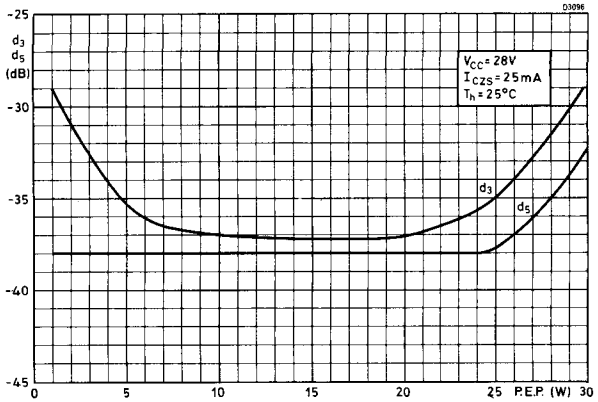
APPLICATION INFORMATION (contd.)

R.F. performance in S.S.B. operation (linear power amplifier)

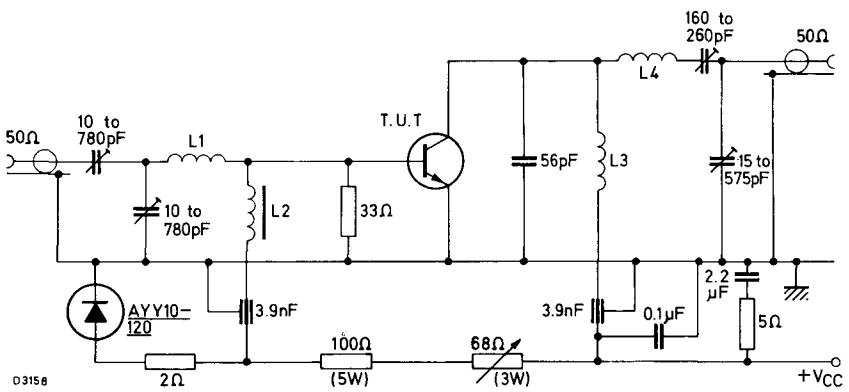
f_1 = 28.000MHz, f_2 = 28.001MHz, $T_h \leq 25^oC$

V_{CC} (V)	P_L (W)	G_p (dB)	$*d_3$ (dB)	dt (%)	I_{CZS} (mA)	I_C (A)	Class
28	25(P.E.P.)	>18	typ. -35	typ. 35	25	typ. 1.28	AB

*Intermodulation distortion figure quoted is related to the according level of either of the equal amplified tones. Relative to the according peak envelope power, this figure should be increased by 6dB.



Test circuit:- Class AB



L1 = 3 turns of enamelled copper wire (1.5mm); winding pitch 2.5mm; int.dia.7mm, leads 50mm (total)

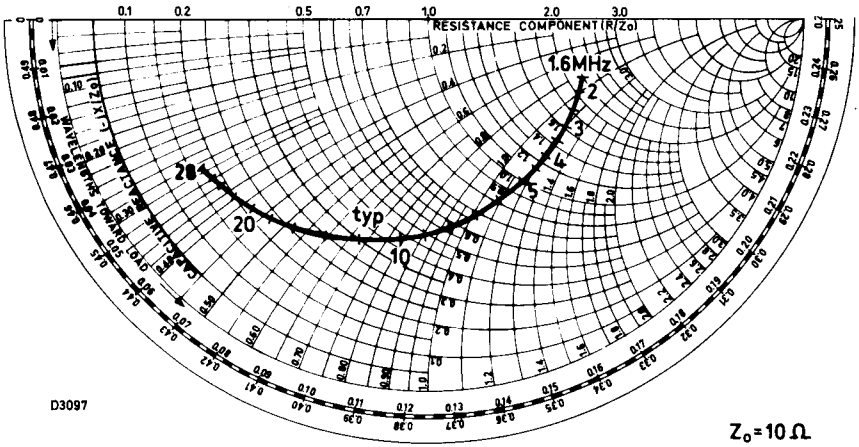
L2 = 7 turns of enamelled copper wire (0.7mm); 60µH.

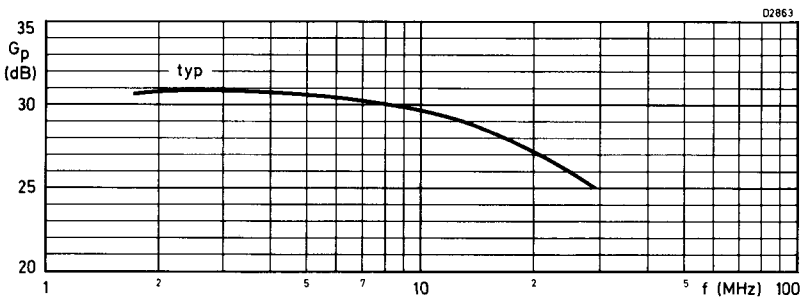
L3 = 4 turns of enamelled copper wire (1.5mm); winding pitch 2.5mm; int. dia. 10mm.

L4 = 7 turns of enamelled copper wire (1.5mm); winding pitch 2.5mm; int. dia. 12mm.

APPLICATION INFORMATION (contd.)

Typical large signal input impedance and transistor power gain in a class AB amplifier at V_{CC} = 28V, P_L = 25W(P.E.P.), Z_L = 12.5Ω, I_{CZS} = 25mA, T_h = 25°C.



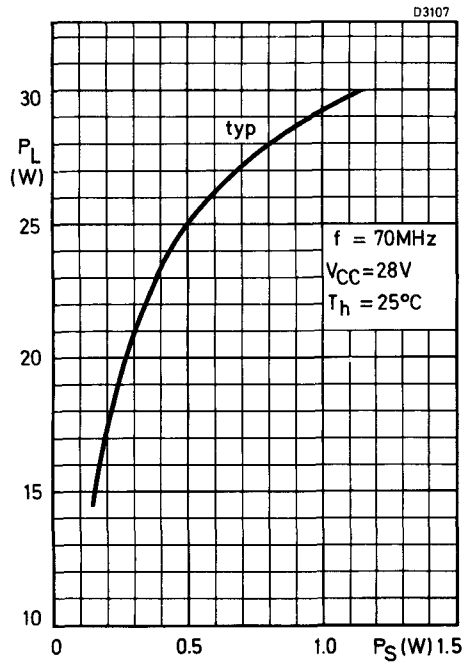


APPLICATION INFORMATION (contd.)

R. F. performance in C. W. operation (Class B)

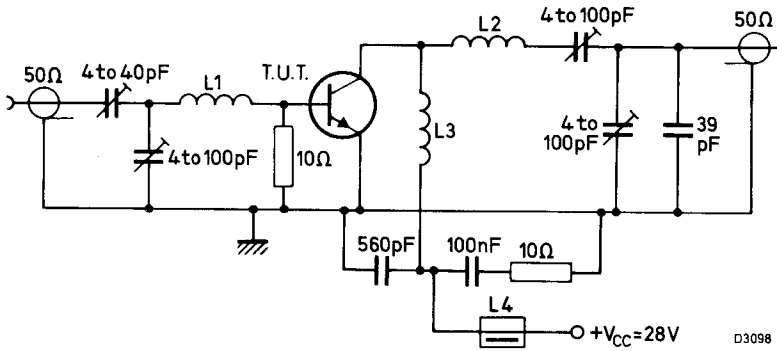
$V_{CC} = 28V$, $T_h \leq 25^oC$

f (MHz)	P_S (W)	P_L (W)	I_C (A)	G_p (dB)	η (%)	$\overline{z_i}$ (Ω)	$\overline{Y_L}$ (mmho)
70	typ. 0.5	25	typ. 1.49	17	60	0.53-j1.4	42.5-j54



APPLICATION INFORMATION (contd.)

Test circuit:- 70MHz (class B)



L1 = 3 turns of enamelled copper wire (1.5mm) 93nH; int. dia. 10mm, length 8mm, leads 2 × 5mm.

L2 = 5 turns of enamelled copper wire (1.5mm) 147nH; int. dia. 9mm, length 14mm, leads 2 × 5mm.

L3 = 4 turns of enamelled copper wire (1.5mm) 118nH; int. dia. 9mm, length 10.5mm, leads 2 × 5mm.

L4 = Ferroxcube choke

CAUTION

This device incorporates Beryllium Oxide, the dust of which is toxic. The device is entirely safe provided that it is not dismantled.

Care should be taken to ensure that all those who may handle, use or dispose of this device are aware of its nature and of the necessary safety precautions. In particular, it should never be thrown out with general industrial or domestic waste.

DISPOSAL SERVICE

Devices requiring disposal may be returned to the Mullard Service Department. They must be separately and securely packed and clearly identified. If any are damaged or broken they MUST NOT be sent through the post. In this case, advice is available from:

The Service Department
Mullard Limited
2 New Road
Mitcham Junction
Surrey. CR4 4XY.

N-P-N SILICON PLANAR EPITAXIAL V.H.F. TRANSISTOR

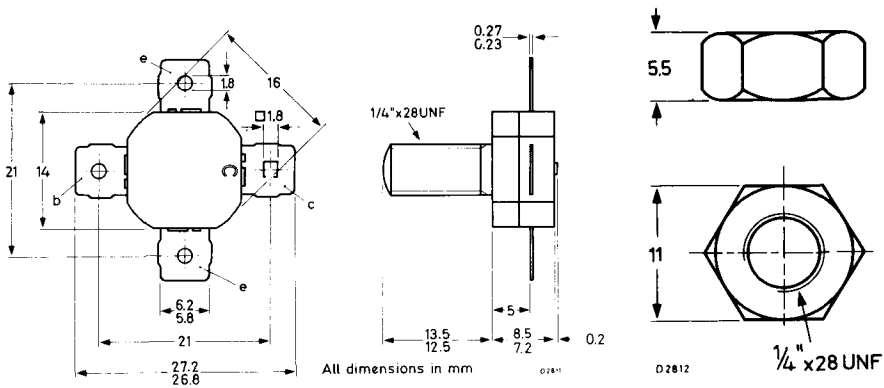
BLX14

Silicon n-p-n planar epitaxial transmitting transistor in a plastic stripline package, for use in s.s.b. and c.w. equipment with a 28V supply, operating in the v.h.f. band. The BLX14 is rated at 50W P.E.P. in the frequency range 1.6 to 28MHz (intermodulation better than 30dB down, full load mismatch permissible at stud temperatures up to 70°C) and at 50W for frequencies up to 70MHz in the c.w. operation.

QUICK REFERENCE DATA

Operation	Class	V_{CC} (V)	f (MHz)	P_L (W)	G_p (dB)	d_3 (dB)	I_{CZS} (A)
s.s.b.	A	28	1.6 to 28	15(P.E.P.)	>13	typ.-40	2.0
s.s.b.	AB	28	1.6 to 28	7.5 to 50 (P.E.P.)	>13	< -30	0.1
c.w.	B	28	70	50	>7.5		
c.w.	B	28	30	50	typ.16		

OUTLINE AND DIMENSIONS



Torque on nut: 23kg cm (2.3N m) min.
27kg cm (2.7N m) max.

Diameter of clearance hole in heatsink: 6.5mm max.

Note: Do not chamfer the edges of the mounting holes when removing burrs.

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

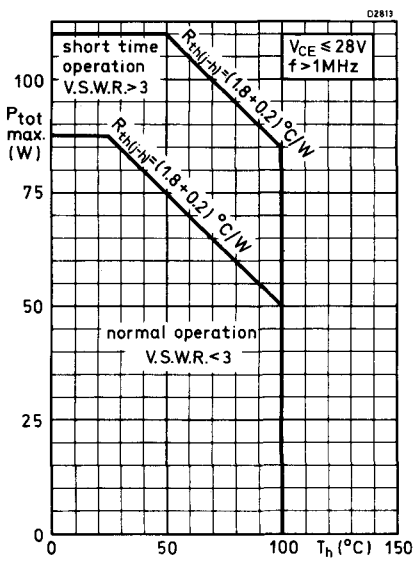
V_{CBOM} max.	85	V
V_{CERM} max. (R_{BE} = 10Ω)	85	V
V_{CEO} max.	36	V
V_{EBO} max.	4.0	V
$I_{C(AV)}$ max.	4.0	A
I_{CM} max. (f > 1MHz)	12	A
P_{tot} max. ($T_h \leq 25^oC$, f > 1MHz)	88	W

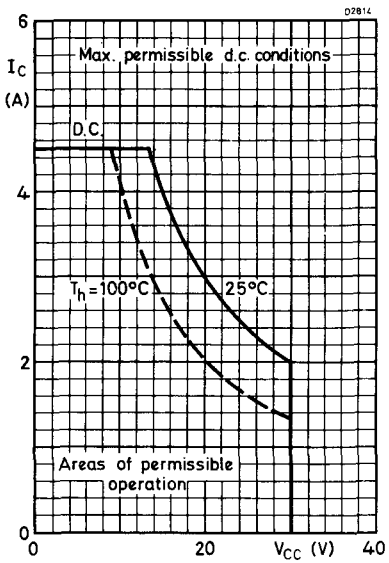
Temperature

T_{stg}	-65 to +200	^oC
T_j max.	200	^oC

THERMAL CHARACTERISTICS

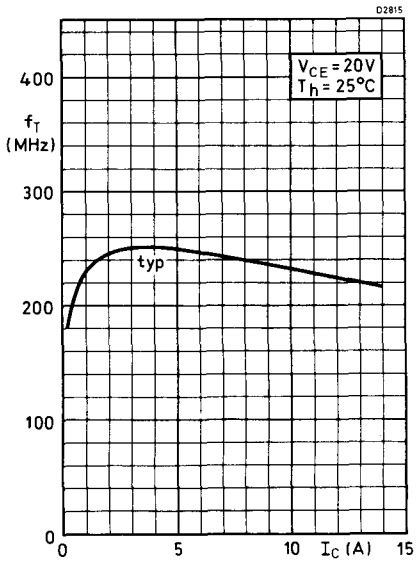
$R_{th(j-mb)}$	1.8	degC/W
$R_{th(mb-h)}$	0.2	degC/W

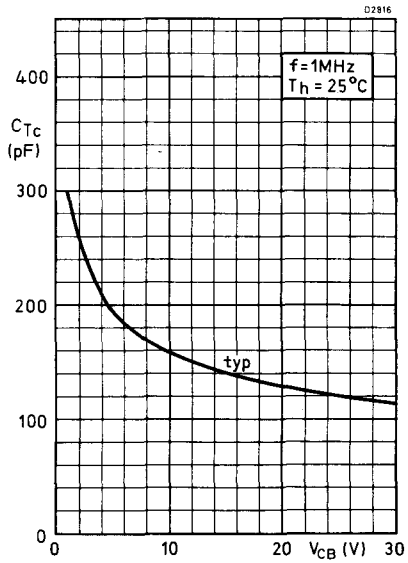


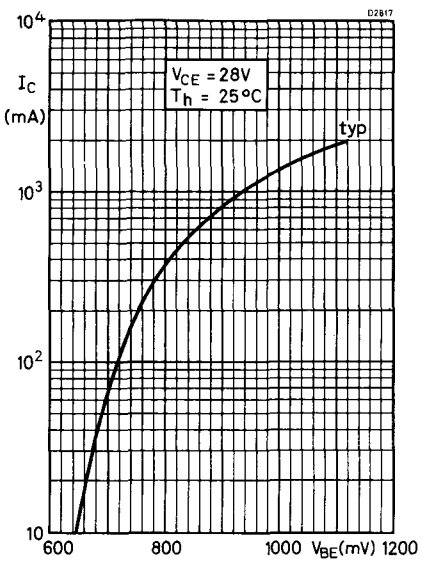


ELECTRICAL CHARACTERISTICS ($T_j = 25^oC$ unless otherwise stated)

		Min.	Typ.	Max.	
$V_{(BR)CBO}$	Collector-base breakdown voltage open emitter, $I_C = 25mA$	85	-	-	V
$V_{(BR)CER}$	Collector-emitter breakdown voltage $R_{BE} = 10\Omega$, $I_C = 25mA$	85	-	-	V
$V_{(BR)CEO}$	Collector-emitter breakdown voltage open base, $I_C = 50mA$	36	-	-	V
$V_{(BR)EBO}$	Emitter-base breakdown voltage open collector, $I_E = 10mA$	4.0	-	-	V
$V_{CE(sat)}$	Collector-emitter saturation voltage $I_C = 0.7A$, $I_B = 0.14A$	-	-	1.0	V
E	Transient energy L = 25mH, f = 50Hz				
	open base	8.0	-	-	mWs
	$-V_{BE} = 1.5V$, $R_{BE} = 33\Omega$	8.0	-	-	mWs
h_{FE}	Static forward current transfer ratio $I_C = 1.4A$, $V_{CE} = 6V$	15	-	100	
f_T	Transition frequency $I_C = 3.0A$, $V_{CE} = 10V$	-	250	-	MHz
C_{Tc}	Collector capacitance $I_E = I_e = 0$, $V_{CB} = 30V$, f = 1MHz	-	115	125	pF
$-C_{re}$	Feedback capacitance $I_C = 100mA$, $V_{CE} = 28V$, f = 1MHz	-	90	-	pF
C_{cs}	Collector-stud capacitance	-	3.5	-	pF


D2815
V_{CE} = 20V
T_h = 25°C
f_T (MHz)
400
300
200
100
0
typ
0
5
10
I_C (A)
15


D2816
f = 1MHz
T_h = 25°C
C_{Tc} (pF)
400
300
200
100
0
typ
0
10
20
V_{CB} (V)
30


D2817
V_{CE} = 28V
T_h = 25°C
I_C (mA)
10^4
10^3
10^2
10
typ
600
800
1000
V_{BE}(mV)
1200

APPLICATION INFORMATION

R.F. performance in S.S.B. operation (linear power amplifier)

V_{CC} = 28V; T_h up to 25°C

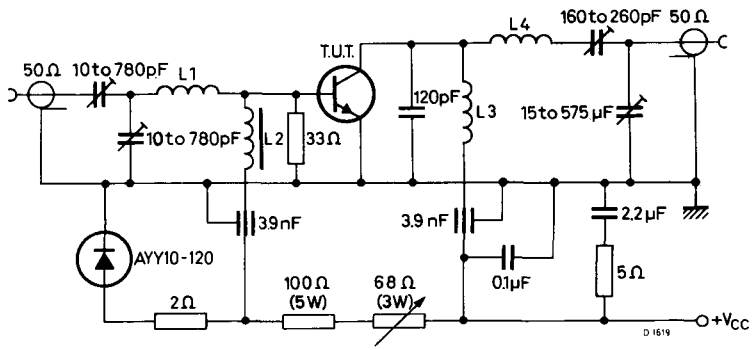
f_1 = 28.000MHz; f_2 = 28.001MHz

Output power (W)	G_p (dB)	η_{dt} (%)	d_3† (dB)	d_5† (dB)	I_{CZS} (A)	I_C (A)	Class
7.5 to 50 (P.E.P.)	>13	>35	<-30	<-30	0.1	<2.55	AB

At temperatures up to 90°C the output power relative to that at 25°C is diminished by a factor of -40mW/degC.

The transistor is designed to withstand a full load mismatch operating under 50W P.E.P. at V_{CC} = 28V and T_h = 70°C.

Test circuit:- Class A-B



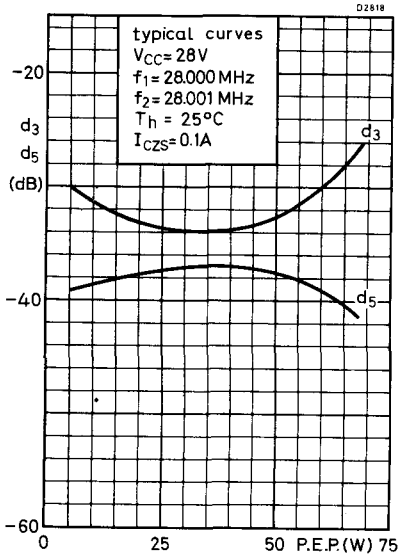
L1 = 3 turns of enamelled copper wire (1.5mm); winding pitch 2.5mm; int. dia. 7mm, leads 50mm (total).

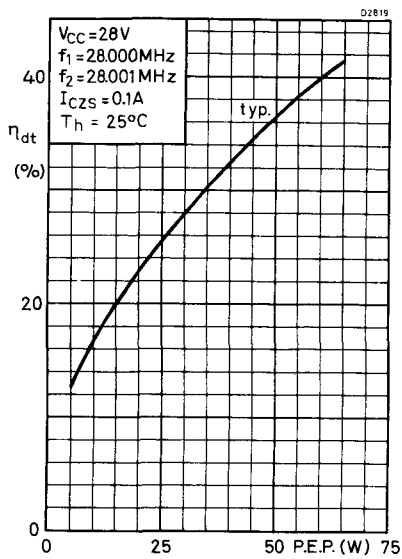
L2 = 7 turns of enamelled copper wire (0.7mm); 60μH.

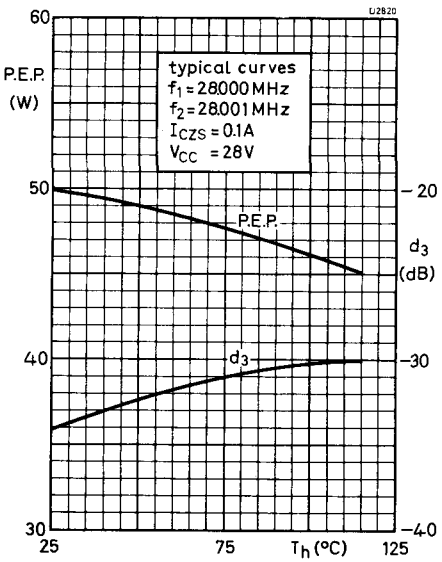
L3 = 4 turns of enamelled copper wire (1.5mm); winding pitch 2.5mm; int. dia. 10mm.

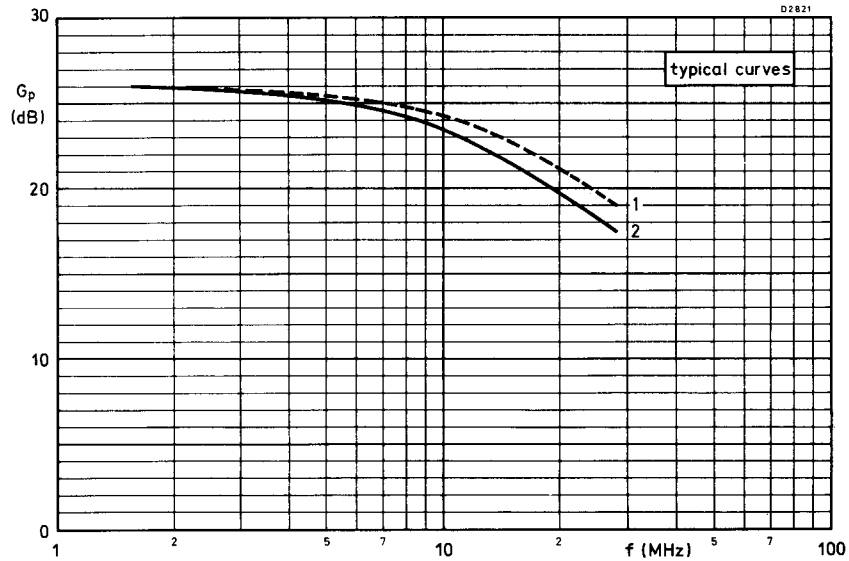
L4 = 7 turns of enamelled copper wire (1.5mm); winding pitch 2.5mm; int. dia. 12mm.

† Maximum values encountered at any level of drive refer to the amplitude of either of the two equal tones at that level.


D2818
typical curves
V_{CC} = 28V
f_1 = 28.000 MHz
f_2 = 28.001 MHz
T_h = 25°C
I_{CZS} = 0.1A
d_3
d_5
(dB)
−20
−40
−60
0
25
50
P.E.P.(W)
75


D2819
V_{CC} = 28V
f_1 = 28.000MHz
f_2 = 28.001MHz
I_{CZS} = 0.1A
T_h = 25°C
typ.
η_{dt}
(%)
40
20
0
0
25
50
P.E.P.(W)
75


D2820
typical curves
f_1 = 28.000 MHz
f_2 = 28.001 MHz
I_{CZS} = 0.1A
V_{CC} = 28V
P.E.P.
(W)
60
50
40
30
P.E.P.
d_3
−20
−30
−40
(dB)
25
75
T_h (°C)
125



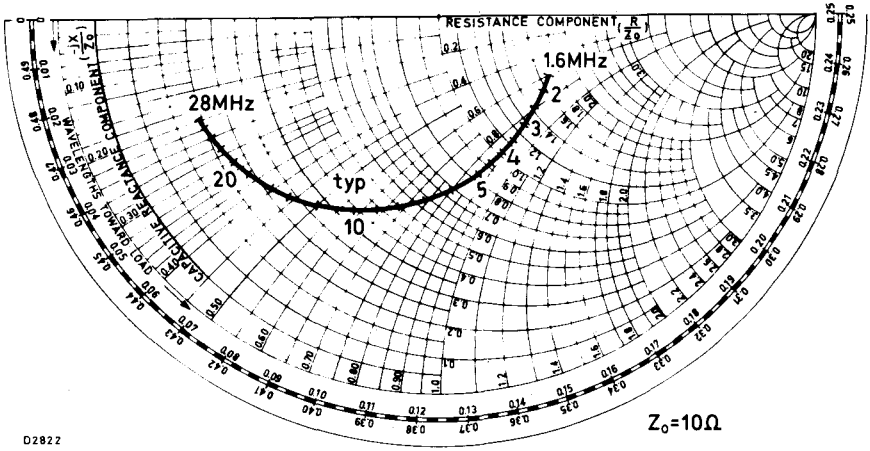
S.S.B. class AB operation

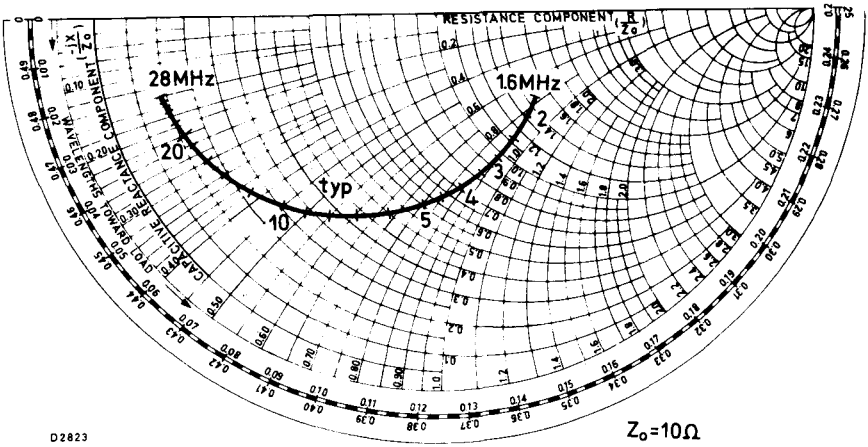
P_L = 50W P.E.P.
V_{CC} = 28V
I_C = 100mA
Z_L = 6.25Ω
T_h = 25°C

Curves

1. This curve applies to a push-pull amplifier with cross neutralisation. Collector-base neutralising capacitor = 82pF.

2. This curve applies to an un-neutralised amplifier.





S.S.B. class AB operation

P_L	= 50W P.E.P.	Z_L	= 6.25Ω
V_{CC}	= 28V	T_h	= 25°C
I_C	= 100mA		

The upper curve applies to a push-pull amplifier with cross neutralisation. Collector-base neutralising capacitor = 82pF

The lower curve applies to an un-neutralised amplifier.

APPLICATION INFORMATION (contd.)

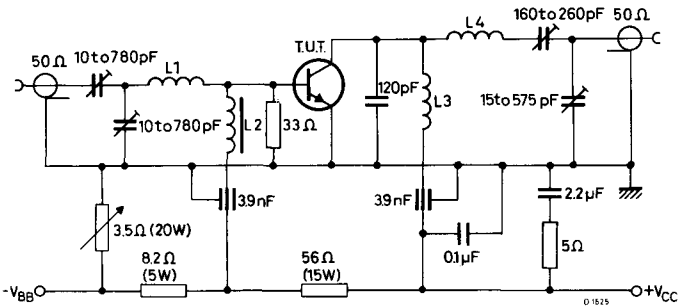
R.F. performance in S.S.B. operation (linear power amplifier)

V_{CC} = 28V, T_h up to 25°C, f_1 = 28.000MHz, f_2 = 28.001MHz

Output power (W)	G_p (dB)	η_{dt} (%)	d_3† (dB)	d_5† (dB)	I_C (A)	Class
15 P.E.P.	>13	-	typ. -40	typ. -45	2.0	A

† See note on page 5.

Test circuit: - Class A

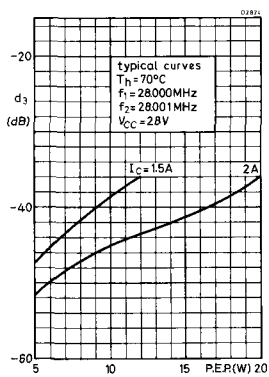


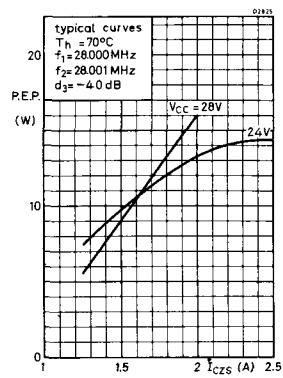
L1 = 3 turns of enamelled copper wire (1.5mm); winding pitch 2.5mm; int. dia. 7mm, leads 50mm (total).

L2 = 7 turns of enamelled copper wire (0.7mm); 60μH.

L3 = 4 turns of enamelled copper wire (1.5mm); winding pitch 2.5mm; int. dia. 10mm.

L4 = 7 turns of enamelled copper wire (1.5mm); winding pitch 2.5mm; int. dia. 12mm.





APPLICATION INFORMATION (contd.)

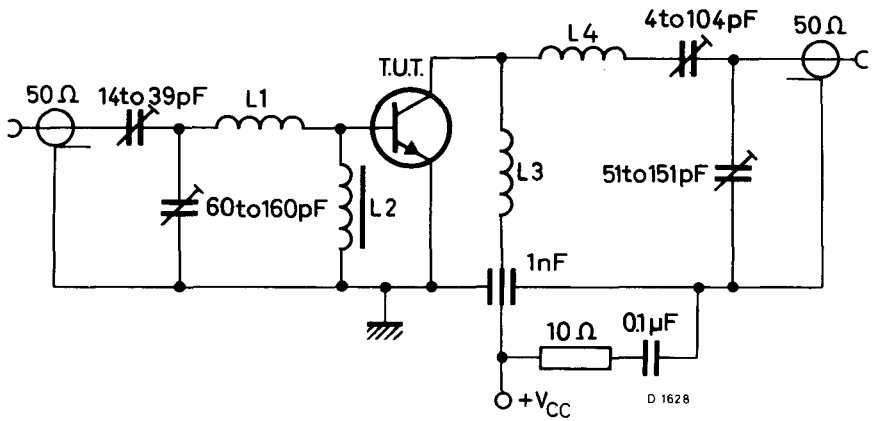
R.F. performance in c.w. operation (class B)

V_{CC} = 28V, T_h up to 25°C

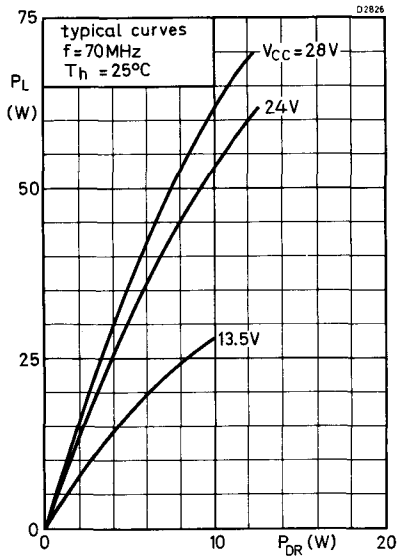
f (MHz)	P_{DR} (W)	P_L (W)	I_C (A)	G_p (dB)	η (%)	$\overline{z_i}$ (Ω)	$\overline{Y_L}$ (mA/V)
70	< 8.9	50	< 3.25	> 7.5	> 55	1.0 +j0.2	115-j77
50	typ. 4	50	typ. 3.25	typ. 11	typ. 55	0.9 -j0.5	104-j85
30	typ. 1.2	50	typ. 3.25	typ. 16	typ. 55	0.75-j1.6	89-j101

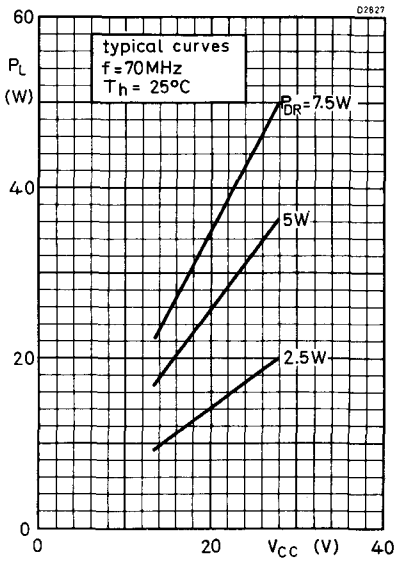
At temperatures up to 90°C the output power relative to that at 25°C is diminished by a factor of -40mW/degC.

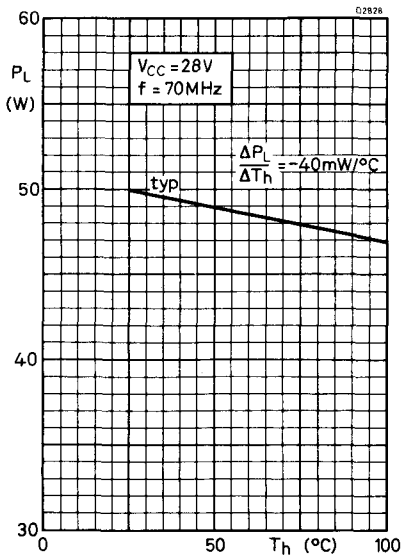
Test circuit: - f = 70MHz



L1 = 60mm of straight enamelled copper wire (1.5mm); 9mm above chassis
L2 = FXC choke coil
L3 = 2 turns of enamelled copper wire (1.5mm); winding pitch 2mm; int.dia.10mm, leads 55mm (total)
L4 = 3 turns of enamelled copper wire (1.5mm); winding pitch 2.5mm; int. dia. 10mm, leads 50mm (total)

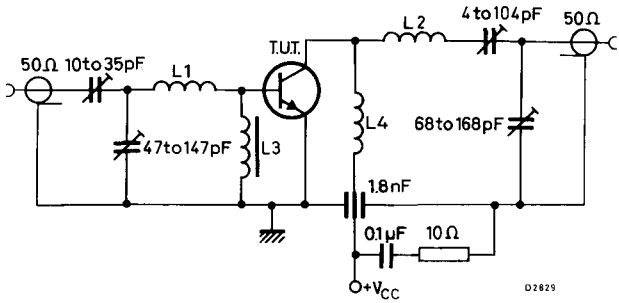

D2826
typical curves
f = 70MHz
Th = 25°C
PL (W)
VCC = 28V
24V
13.5V
75
50
25
0
0
10
PDR (W)
20


D2827
typical curves
f = 70MHz
Th = 25°C
PL (W)
PDR = 7.5W
5W
2.5W
60
40
20
0
0
20
VCC (V)
40

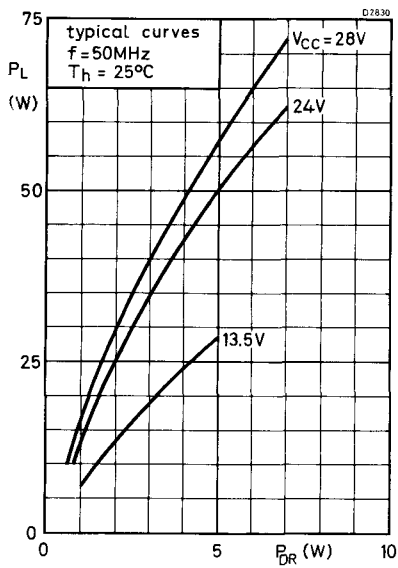

D2828
VCC = 28V
f = 70MHz
PL (W)
ΔPL/ΔTh = -40mW/°C
typ
60
50
40
30
0
50
Th (°C)
100

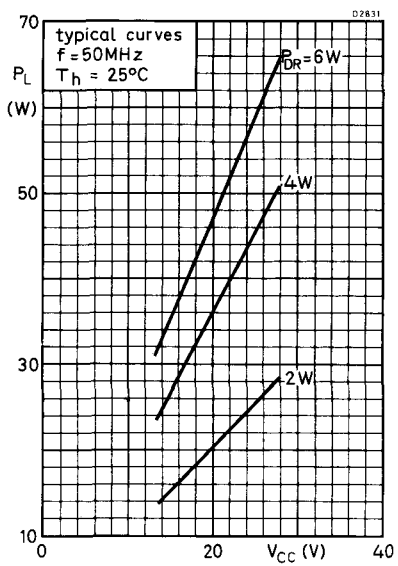
APPLICATION INFORMATION (contd.)

Test circuit:- f=50MHz



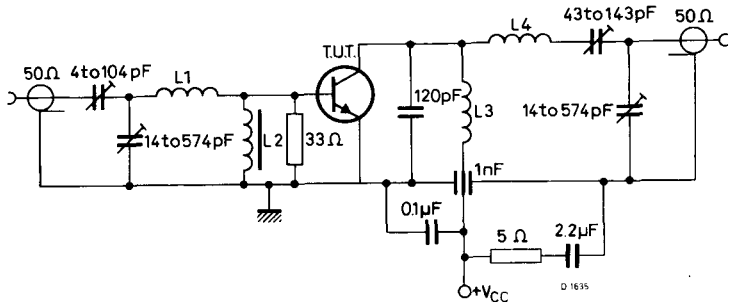
L1 = 1 turn of enamelled copper wire (1.5mm); int.dia. 10mm; leads 40mm (total)
L2 = 4 turns of enamelled copper wire (1.5mm); int.dia. 12mm; leads 40mm (total)
L3 = FXC choke coil
L4 = 3 turns of enamelled copper wire (1.5mm); int.dia.10mm; leads 40mm (total), winding pitch 2mm



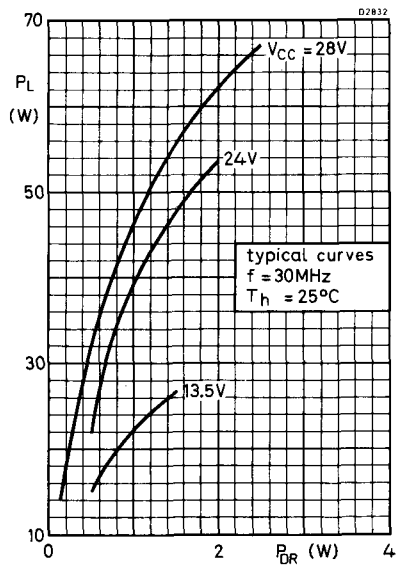


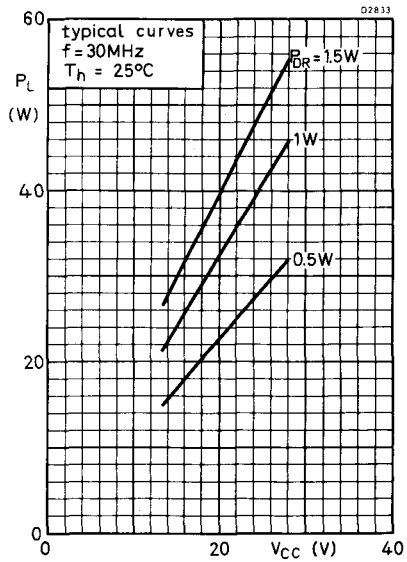
APPLICATION INFORMATION (contd.)

Test circuit: - f = 30MHz



L1 = 2 turns of enamelled copper wire (1.5mm); winding pitch 2mm; int.dia.10mm; leads 60mm (total)
L2 = 7 turns of enamelled copper wire (0.7mm); 60μH
L3 = 4 turns of enamelled copper wire (1.5mm); winding pitch 2mm; int.dia.10mm; leads 50mm (total)
L4 = 6 turns of enamelled copper wire (1.5mm); winding pitch 2mm; int.dia.12mm; leads 50mm (total)





CAUTION

This device incorporates Beryllium Oxide, the dust of which is toxic. The device is entirely safe provided that it is not dismantled.

Care should be taken to ensure that all those who may handle, use or dispose of this device are aware of its nature and of the necessary safety precautions. In particular, it should never be thrown out with general industrial or domestic waste.

DISPOSAL SERVICE

Devices requiring disposal may be returned to the Mullard Service Department. They must be separately and securely packed and clearly identified. If any are damaged or broken they MUST NOT be sent through the post. In this case, advice is available from:

THE SERVICE DEPARTMENT
MULLARD LIMITED
2 NEW ROAD, MITCHAM JUNCTION
SURREY, CR4 4 XY.

N-P-N SILICON PLANAR V.H.F./U.H.F. TRANSISTOR

BLX65

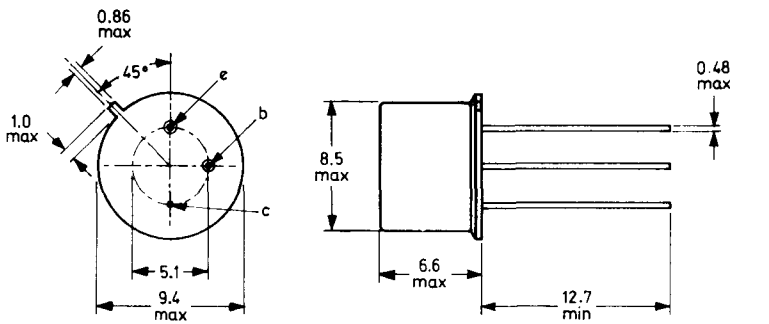
Silicon n-p-n transistor, mounted in a TO-39 envelope, for v.h.f./u.h.f. mobile applications. With a supply voltage of 13.8V and a signal frequency of 470MHz, the BLX65 will produce typically 2.0W output into a 50Ω load.

QUICK REFERENCE DATA

V_{CC} (V)	f (MHz)	P_{DR} (W)	P_L into 50Ω (W)	η (%)	T_c (^oC)	Circuit
12.5	470	0.5	2.0 min.	65 min.	25	Un-neutralised common-emitter class B
13.8	470	0.4	2.0 typ.	66 typ.	25	
12.5	175	0.12	2.0 typ.	75 typ.	25	

OUTLINE AND DIMENSIONS

Conforms to BS 3934 SO-3/SB3-3B
J.E.D.E.C. TO-39



All dimensions in mm

D1574

Collector connected to case

The maximum lead diameter is guaranteed only for 12.7mm

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{CBOM} max.	36	V
V_{CESM} max. (R_{BE} = 0)	36	V
V_{CEO} max.	18	V
V_{EBO} max.	4.0	V
I_C max.	0.7	A
I_{CM} max. ($f \geq 10MHz$)	2.0	A
P_{tot} max. ($f \geq 10MHz$, $T_c \leq 90^oC$)	3.0	W

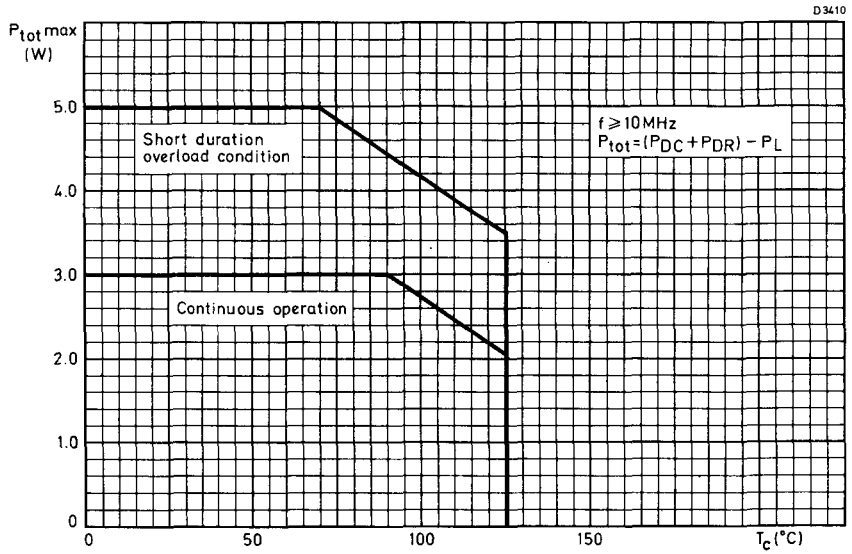
See also graph on page 3

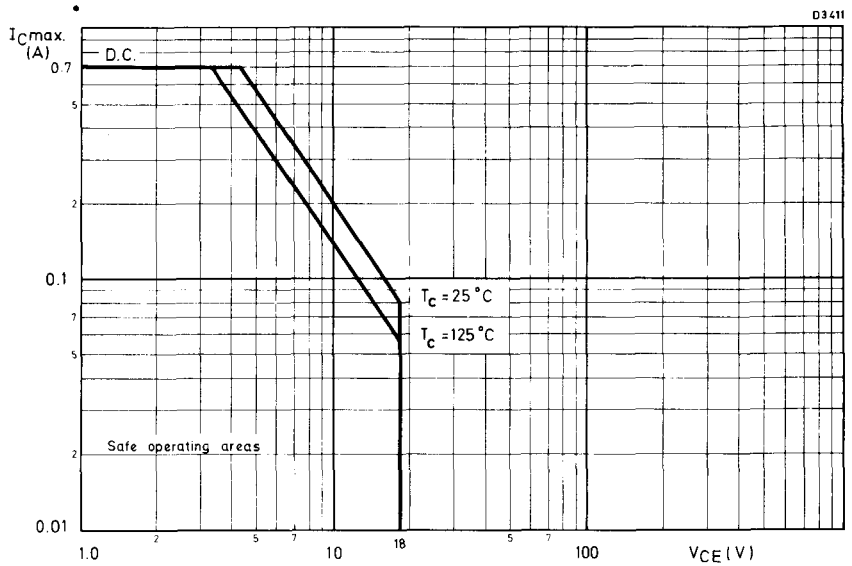
Temperature

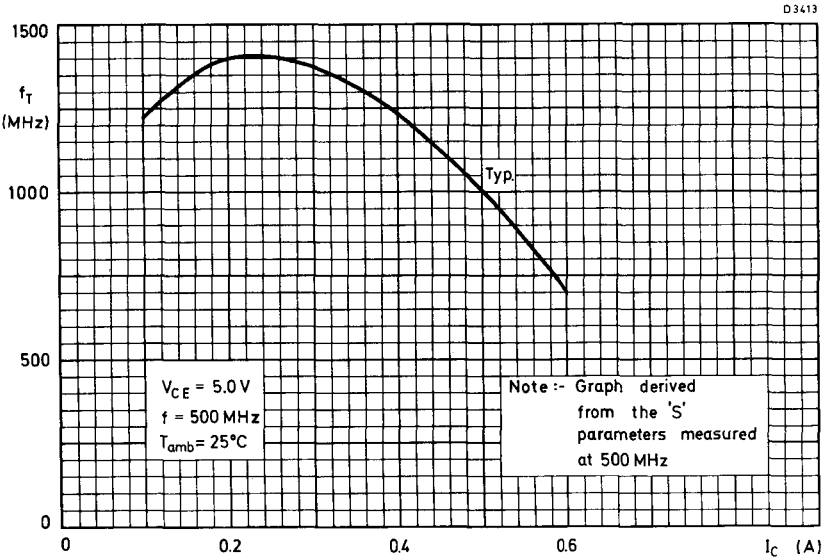
T_{stg}	-65 to +150	^oC

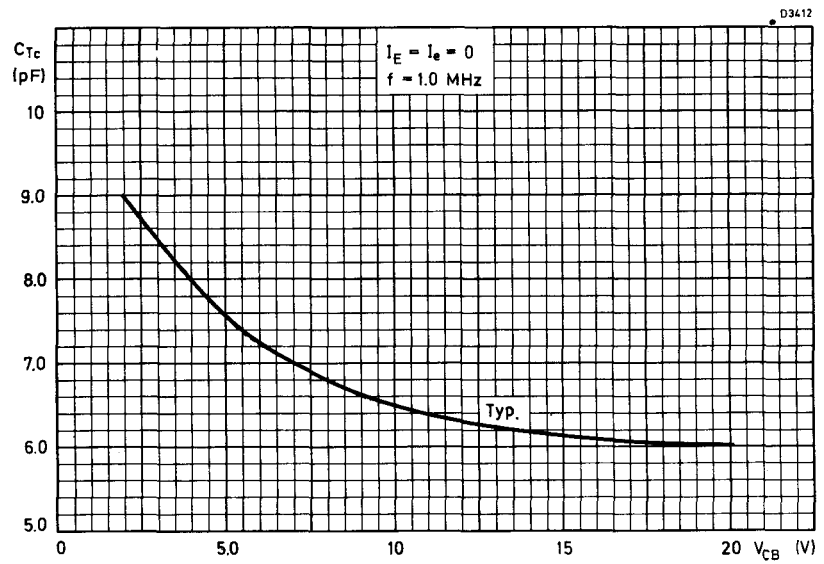
ELECTRICAL CHARACTERISTICS ($T_j = 25^oC$ unless otherwise stated)

		Min.	Typ.	Max.	
$V_{(BR)CBO}$	Collector-base breakdown voltage I_C = 10mA	36	-	-	V
$V_{(BR)CES}$	Collector-emitter breakdown voltage I_C = 10mA, R_{BE} = 0	36	-	-	V
$V_{(BR)CEO}$	Collector-emitter breakdown voltage I_C = 25mA	18	-	-	V
$V_{(BR)EBO}$	Emitter-base breakdown voltage I_E = 1.0mA	4.0	-	-	V
$V_{CE(sat)}$	Collector emitter saturation voltage I_C = 100mA, I_B = 20mA	-	0.1	-	V
h_{FE}	Static forward current transfer ratio I_C = 100mA, V_{CE} = 5.0V	10	40	-	
f_T	Transition frequency I_C = 200mA, V_{CE} = 5.0V, f = 500MHz	-	1400	-	MHz
C_{Tc}	Collector capacitance V_{CB} = 10V, $I_E = I_e$ = 0, f = 1.0MHz	-	6.5	9.0	pF


D3410
P_{tot} max (W)
5.0
4.0
3.0
2.0
1.0
0
Short duration overload condition
Continuous operation
f ⩾ 10 MHz
$P_{tot} = (P_{DC} + P_{DR}) - P_L$
0
50
100
150
T_c (°C)


D3411
I_C max. (A)
0.7
5
2
0.1
7
5
2
0.01
D.C.
T_c = 25 °C
T_c = 125 °C
Safe operating areas
1.0
2
5
7
10
18
5
7
100
V_{CE} (V)


D3413
1500
f_T
(MHz)
1000
500
0
Typ.
V_{CE} = 5.0 V
f = 500 MHz
T_{amb} = 25°C
Note :- Graph derived from the 'S' parameters measured at 500 MHz
0
0.2
0.4
0.6
I_C (A)


D3412
C_{Tc}
(pF)
10
9.0
8.0
7.0
6.0
5.0
$I_E = I_e = 0$
f = 1.0 MHz
Typ.
0
5.0
10
15
20 V_{CB} (V)

APPLICATION INFORMATION

R. F. Performance in c. w. operation (T_c = 25°C)

V_{CC} (V)	f (MHz)	P_{DR} (W)	P_L into 50Ω (W)	η (%)	$\overline{z_i}$ (Ω)	$\overline{Y_L}$ (mmho)
12.5	470	0.5	2.0 min.	65 min.	-	-
13.8	470	0.4	2.0 typ.	66 typ.	5 + j10	16 - j50
12.5	175	0.12	2.0 typ.	75 typ.	-	-

At P_L = 2.0W and V_{CC} = 12.5V, the output power at case temperatures between 25 and 90°C relative to that at 25°C is diminished typically by 5mW/°C.

The transistor is designed to withstand full load mismatch in the test circuit under the following conditions: -

V_{CC} = 16.5V f = 470MHz T_c = 70°C

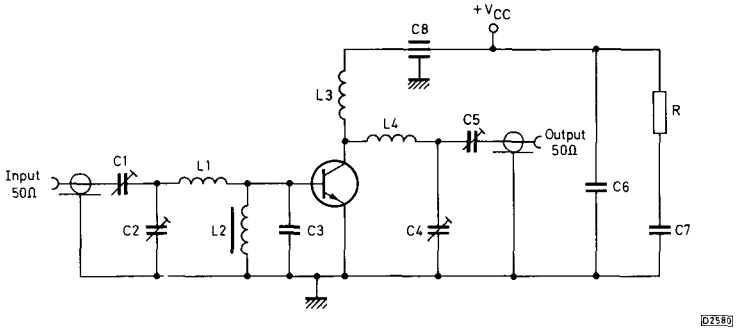
V.S.W.R. = 50:1 at any phase

P_{DR} = P_{DR} nom. +20%.

Where P_{DR} nom. = P_{DR} for 1.4W transistor output into 50Ω load at V_{CC} = 13.8V.

APPLICATION INFORMATION (contd.)

470MHz Amplifier circuit

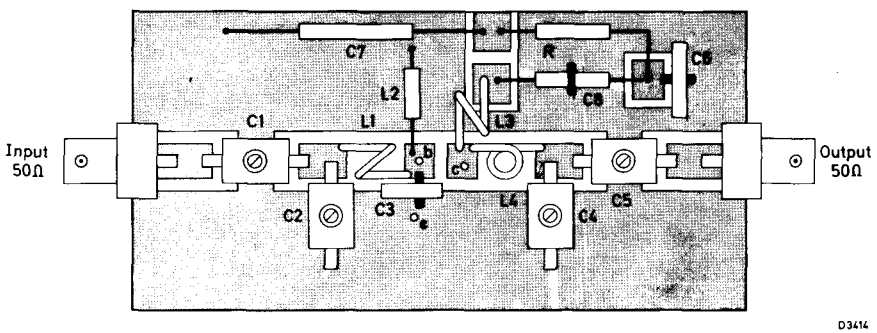


Component values for 470MHz amplifier circuit

C1 = C2 = C4 = C5 = 1.8 to 18pF film dielectric trimmer capacitors
C3 = 22pF disc ceramic capacitor
C6 = 10nF ceramic capacitor
C7 = 0.1μF disc ceramic capacitor
C8 = 4nF feed-through capacitor
L1 = 1 turn of 1mm copper wire, int. dia. 5mm, lead length <1mm
L2 = 0.22μH choke
L3 = 1 turn of 1mm copper wire, int. dia. 7mm, lead length 2mm
L4 = 1 turn of 1mm copper wire, int. dia. 5mm, lead length 2mm
R = 10Ω - carbon

Component layout on 1.5mm single copper clad fibre-glass board

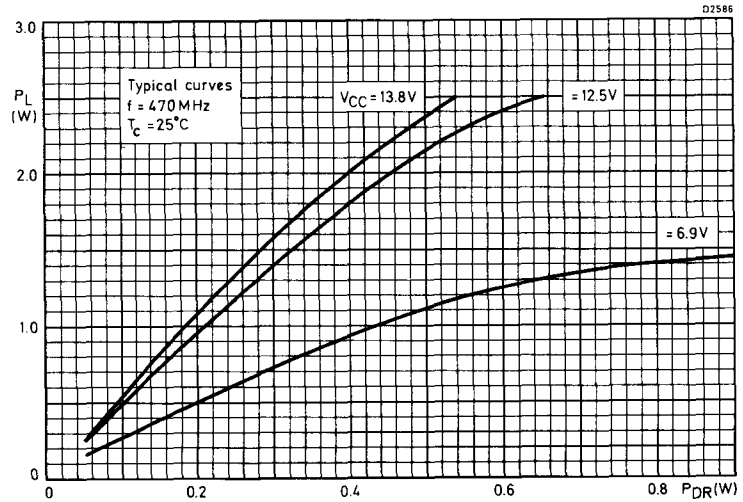
Dimensions of the board: - 80 × 40mm

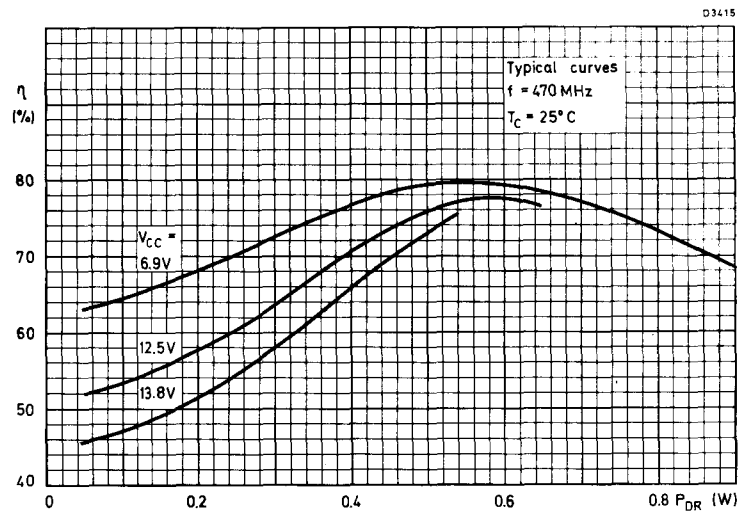


Shaded area copper

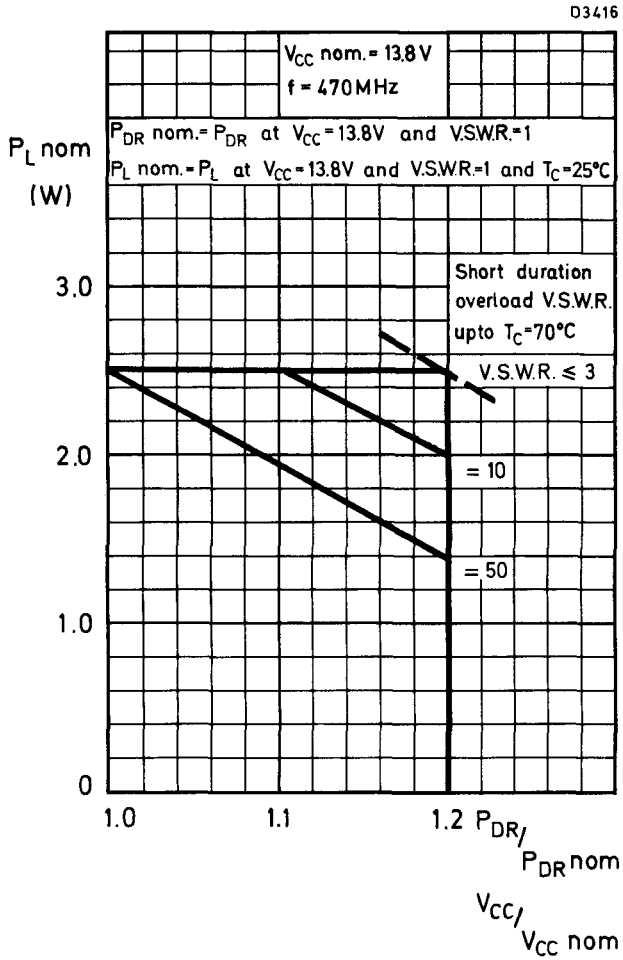
To obtain the specified gain performance, the emitter lead length should not exceed 1.6mm.

APPLICATION INFORMATION (contd.)





TYPICAL VARIATION OF LOAD POWER AND EFFICIENCY WITH DRIVE POWER

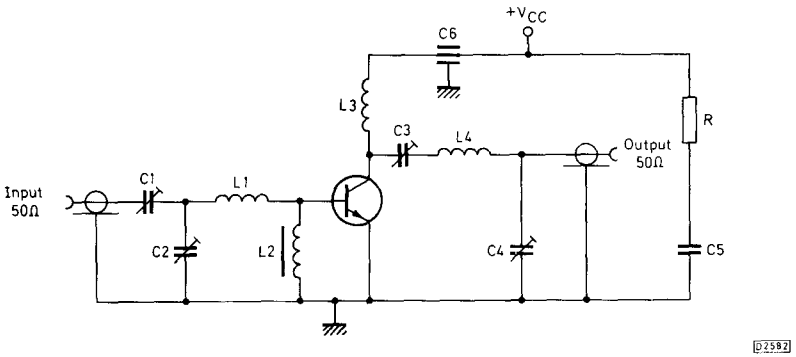


INDICATED LOAD POWER AS A FUNCTION OF OVERLOAD

The transistor is suitable for use with unstabilised supply voltages. The above graph has been derived from an evaluation of the performance of transistors matched up to 2.5 watts load power in the circuit on page 6, and subsequently subjected to various voltage overloads and mismatch conditions with v.s.w.r. up to 50:1 at a heatsink temperature of 70°C. This indicates a restriction to the load power matched under nominal conditions with varying supply voltages and v.s.w.r. in the recommended circuit.

APPLICATION INFORMATION

175MHz Amplifier circuit

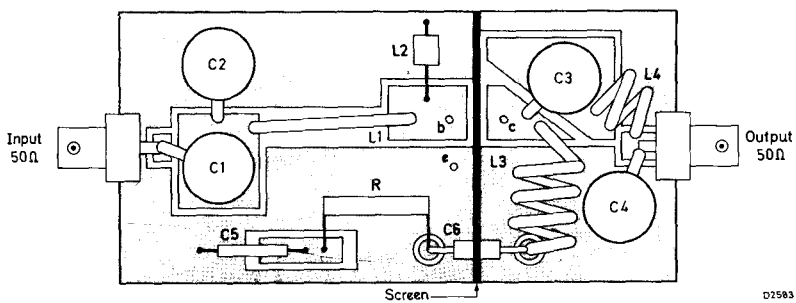


Component values for 175MHz amplifier circuit

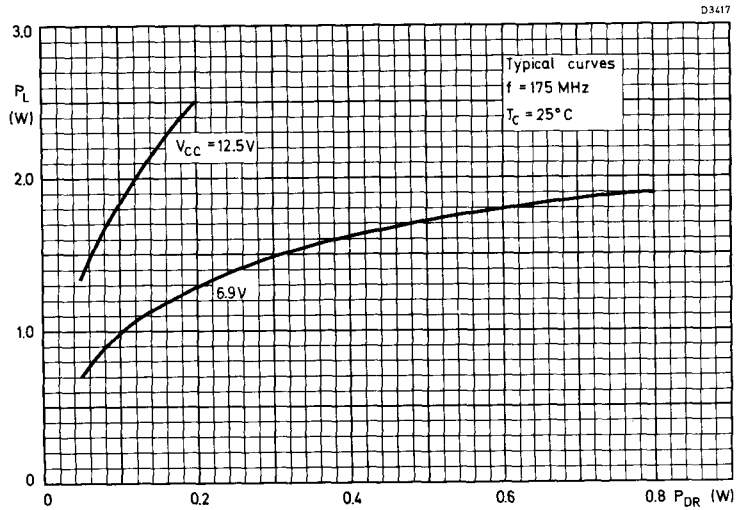
C1 = C4 = 0 to 60pF
C2 = C3 = 0 to 30pF
} concentric trimmer capacitors

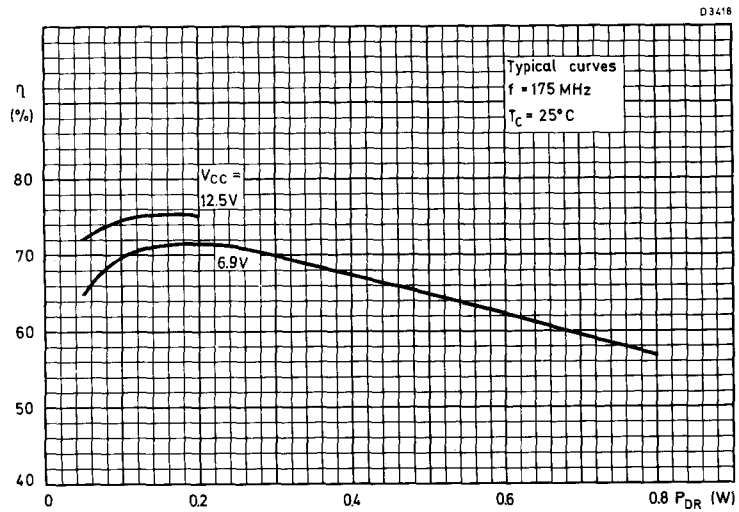
C5 = 0.25μF disc ceramic capacitor
C6 = 4nF feed-through capacitor
L1 = 25mm straight 1.2mm copper wire. Height above board = 3mm
L2 = 3 turns of 0.5mm copper wire on Ferrite FX1115
L3 = 5 turns of 1.2mm copper wire, int. dia. 10mm, close wound, lead length 5mm
L4 = 3 turns of 1.2mm copper wire, int. dia. 10mm, close wound, lead length 5mm
R = 10Ω - carbon

Component layout on 1.5mm single copper clad fibre-glass board
Dimensions of the board 80 × 40mm



Shaded area copper
To obtain the specified gain performance, the emitter lead length should not exceed 1.6mm.





TYPICAL VARIATION OF LOAD POWER AND EFFICIENCY WITH DRIVE POWER

N-P-N SILICON PLANAR V.H.F./U.H.F. TRANSISTOR

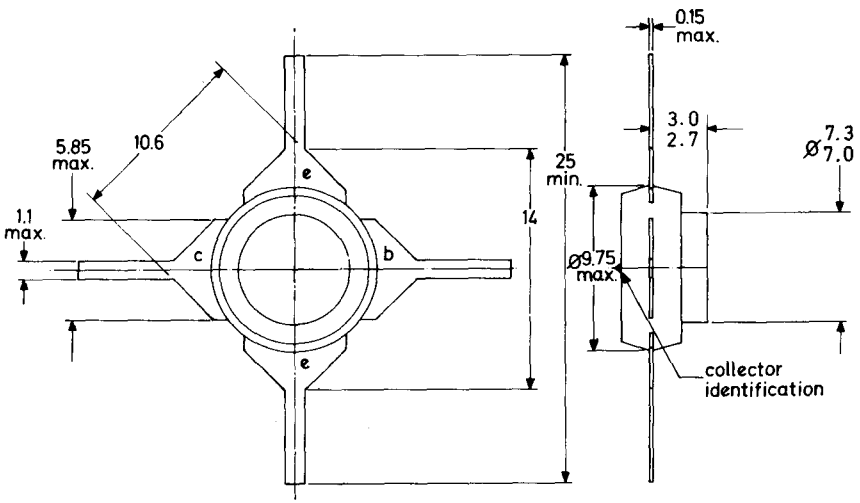
BLX66

Silicon n-p-n transistor for v.h.f./u.h.f. mobile applications. The device is mounted in a plastic, studless, capstan strip-line encapsulation. With a supply voltage of 13.8V and a signal frequency of 470MHz, the BLX66 will produce typically 2.5W output into a 50Ω load.

QUICK REFERENCE DATA

V_{CC} (V)	f (MHz)	P_{DR} (W)	P_L into 50Ω (W)	η (%)	T_{mb} (°C)	Circuit
12.5	470	0.35	2.5 min.	65 min.	25	Un-neutralised common-emitter class B
13.8	470	0.28	2.5 typ.	75 typ.	25	
13.8	470	0.15	1.5 typ.	65 typ.	25	
12.5	175	0.03	3.0 typ.	84 typ.	25	

OUTLINE AND DIMENSIONS



All dimensions in mm

D3419

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{CBOM} max.	36	V
V_{CESM} max. (R_{BE} = 0)	36	V
V_{CEO} max.	18	V
V_{EBO} max.	4.0	V
I_C max.	0.7	A
I_{CM} max. (f ≥ 10MHz)	2.0	A
P_{tot} max. (f ≥ 10MHz, T_{mb} ≤ 90°C)	4.0	W

See also graph on page 3

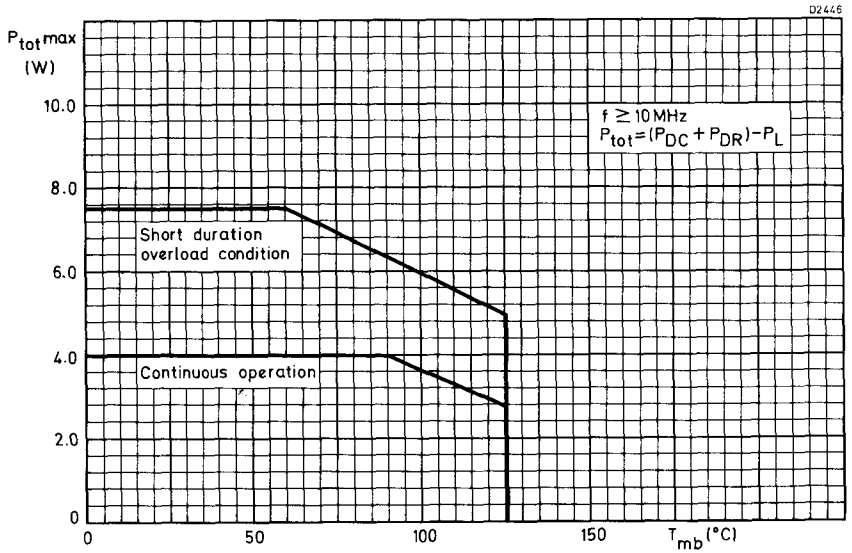
Temperature

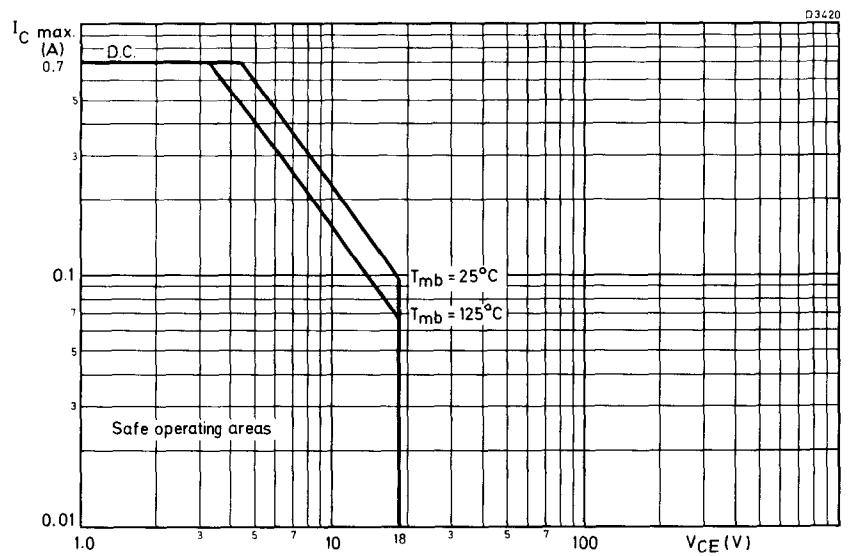
T_{stg}	-65 to +150	°C

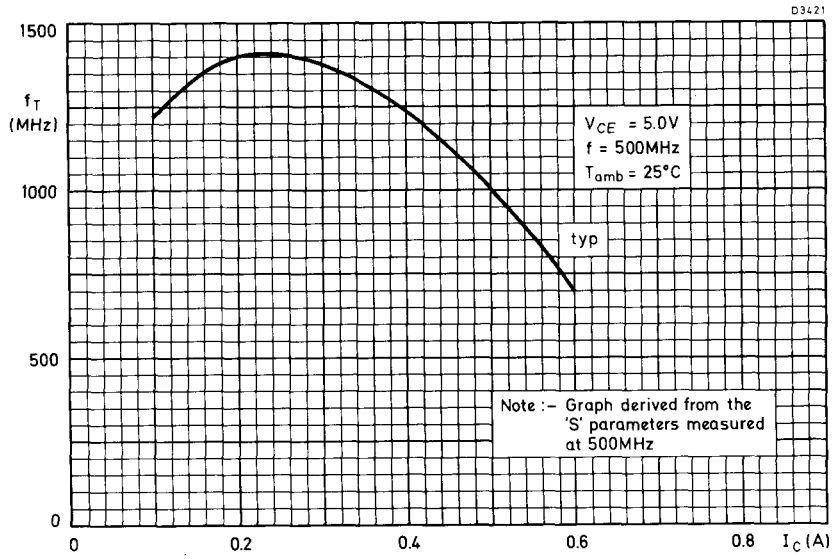
ELECTRICAL CHARACTERISTICS (T_j = 25°C unless otherwise stated)

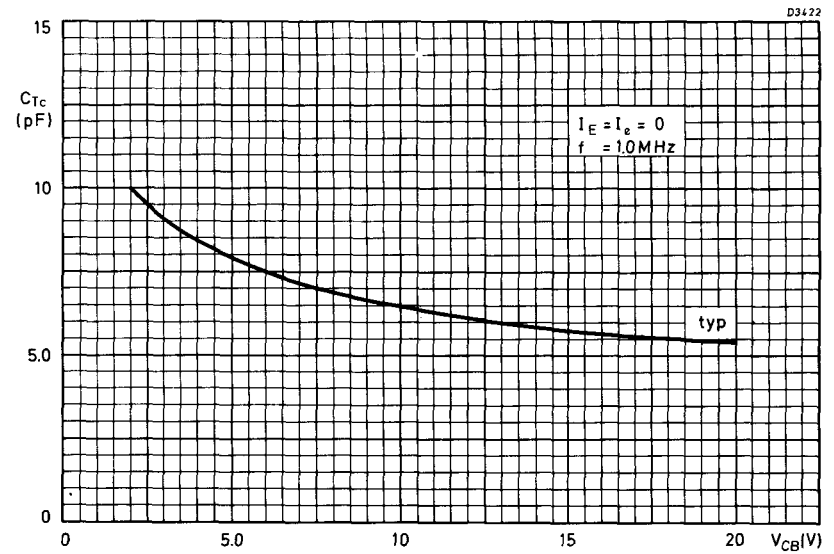
		Min.	Typ.	Max.	
$V_{(BR)CBO}$	Collector-base breakdown voltage I_C = 10mA	36	-	-	V
$V_{(BR)CES}$	Collector-emitter breakdown voltage I_C = 10mA, R_{BE} = 0	36	-	-	V
$V_{(BR)CEO}$	Collector-emitter breakdown voltage I_C = 25mA	18	-	-	V
$V_{(BR)EBO}$	Emitter-base breakdown voltage I_E = 1.0mA	4.0	-	-	V
$V_{CE(sat)}$	Collector-emitter saturation voltage I_C = 100mA, I_B = 20mA	-	0.1	-	V
h_{FE}	Static forward current transfer ratio I_C = 100mA, V_{CE} = 5.0V	10	40	-	
*f_T	Transition frequency I_C = 200mA, V_{CE} = 5.0V, f = 500MHz	-	1400	-	MHz
C_{Tc}	Collector capacitance V_{CB} = 10V, $I_E = I_e$ = 0, f = 1.0MHz	-	6.5	9.0	pF

*Derived from the 'S' parameters measured at f = 500MHz, T_{amb} = 25°C


D2446
P_{tot} max (W)
10.0
8.0
6.0
4.0
2.0
0
$f \geq 10$ MHz
$P_{tot} = (P_{DC} + P_{DR}) - P_L$
Short duration overload condition
Continuous operation
0
50
100
150
T_{mb} (°C)


D3420
I_C max. (A)
D.C.
0.7
5
3
0.1
7
5
3
0.01
T_{mb} = 25°C
T_{mb} = 125°C
Safe operating areas
1.0
3
5
7
10
18
3
5
7
100
V_{CE} (V)


D3421
1500
f_T (MHz)
1000
500
0
0
0.2
0.4
0.6
0.8
I_C (A)
V_{CE} = 5.0V
f = 500MHz
T_{amb} = 25°C
typ
Note :- Graph derived from the 'S' parameters measured at 500MHz


D3422
15
C_{Tc} (pF)
10
5.0
0
0
5.0
10
15
20
V_{CB}(V)
$I_E = I_e = 0$
f = 1.0MHz
typ

APPLICATION INFORMATION

R.F. performance in c.w. operation ($T_{mb} = 25^{o}C$)

V_{CC} (V)	f (MHz)	P_{DR} (W)	P_L into 50Ω (W)	η (%)	$\overline{z_i}$ (Ω)	$\overline{Y_L}$ (mmho)
12.5	470	0.35	2.5 min.	65 min.	-	-
13.8	470	0.28	2.5 typ.	75 typ.	2.5+j4.5	23-j35
13.8	470	0.15	1.5 typ.	65 typ.	-	-
12.5	175	0.03	3.0 typ.	84 typ.	2.4-j3.8	35-j40

At P_L = 2.5W and V_{CC} = 12.5V, the output power at mounting-base temperatures between 25 and 90°C relative to that at 25°C is diminished typically by 5mW/°C.

The transistor is designed to withstand full load mismatch in the test circuit under the following conditions: -

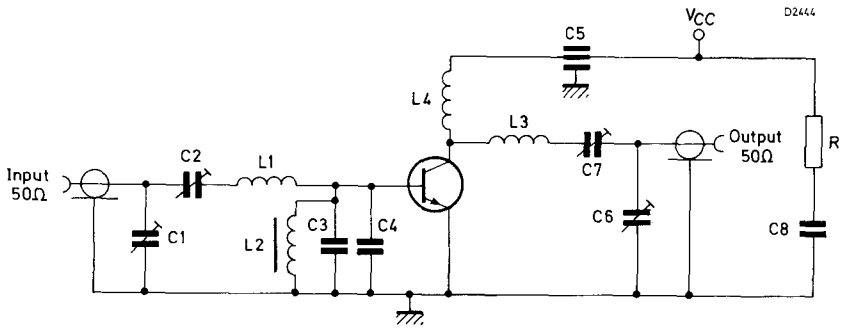
V_{CC} = 16.5V, f = 470MHz, T_{mb} = 70°C

V.S.W.R. = 50:1 at any phase

$P_{DR} = P_{DR}$ nom. +20%

Where P_{DR} nom. = P_{DR} for 2.5W transistor output into a 50Ω load at V_{CC} = 13.8V.

470MHz Amplifier circuit

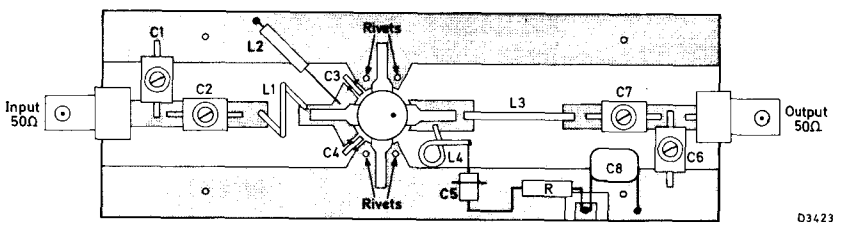


Component values for 470MHz amplifier circuit

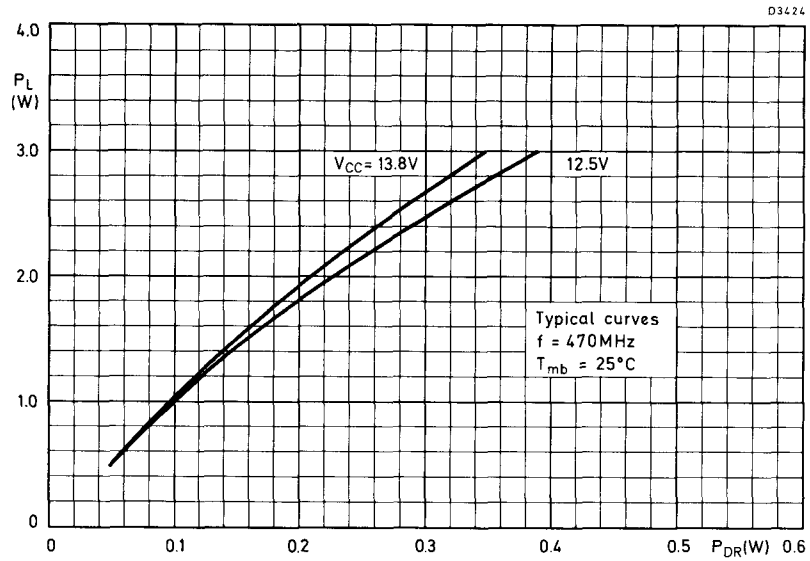
C1 = C2 = C6 =C7 = 1.8 to 18pF film dielectric trimmers
C3 = C4 = 18pF disc ceramic capacitors
C5 = 4nF feed-through capacitor
C8 = 0.1μF disc ceramic capacitor
L1 = 1 turn of 1.2mm copper wire, int. dia. 6mm, lead length < 1mm
L2 = 1μH choke
L3 = 30mm of straight 2mm copper wire. Height above board = 2mm
L4 = 2 turns of 0.5mm copper wire, int. dia. 3mm, close wound, lead length = 8mm
R = 10Ω - carbon

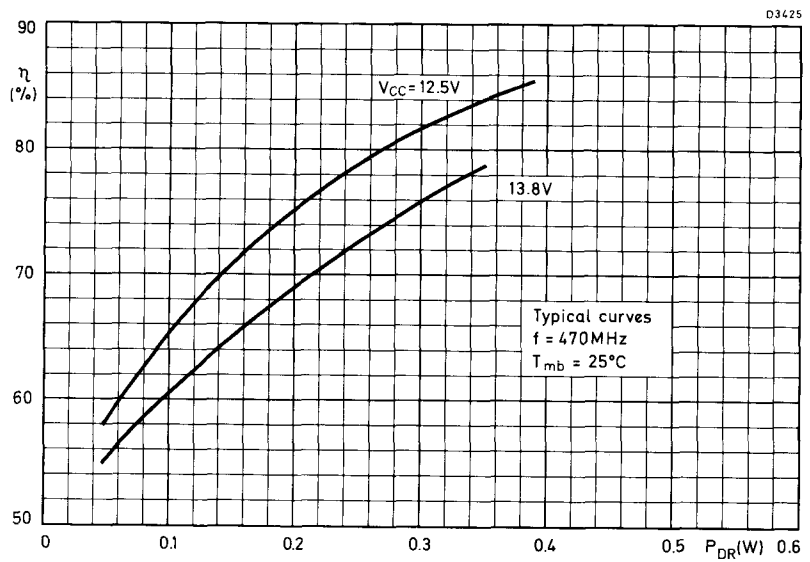
Component layout on 1.5mm double copper clad fibre-glass board

Dimensions of the board: - 110 × 50mm

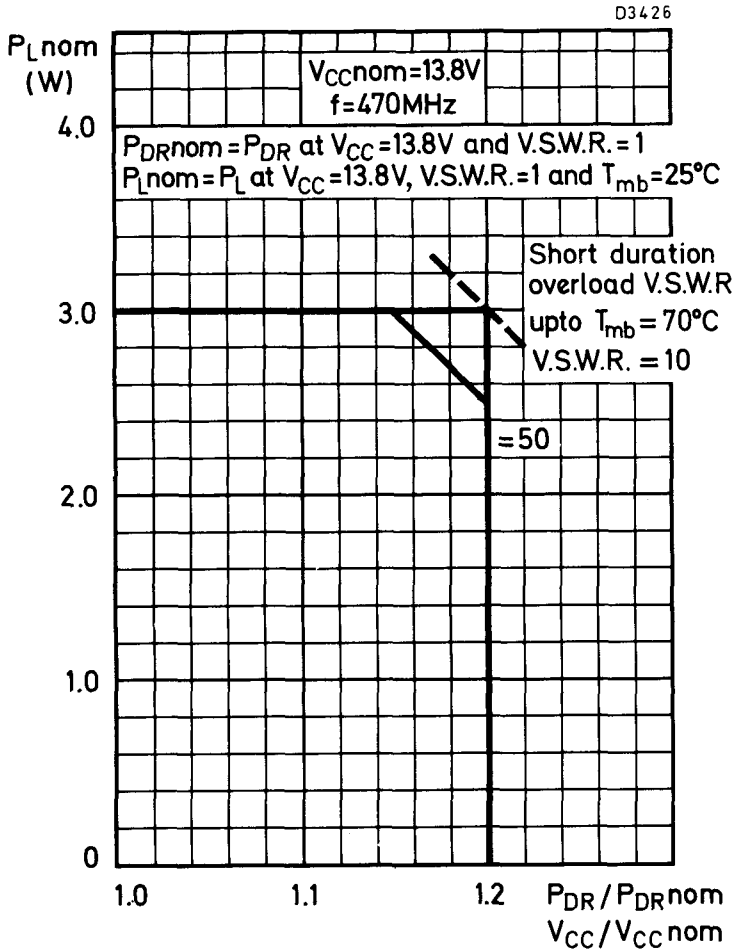


Shaded area copper
Underside area completely copper clad





TYPICAL VARIATION OF LOAD POWER AND EFFICIENCY WITH DRIVE POWER



INDICATED LOAD POWER AS A FUNCTION OF OVERLOAD

The transistor is suitable for use with unstabilised supply voltages. The above graph has been derived from an evaluation of the performance of transistors matched up to 3 watts load power in the circuit on page 6, and subsequently subjected to various voltage overloads and mismatch conditions with v.s.w.r. up to 50: 1 at a heatsink temperature of 70°C. This indicates a restriction to the load power matched under nominal conditions with varying supply voltages and v.s.w.r. in the recommended circuit.

CAUTION

This device incorporates Beryllium Oxide, the dust of which is toxic. The device is entirely safe provided that it is not dismantled.

Care should be taken to ensure that all those who may handle, use or dispose of this device are aware of its nature and of the necessary safety precautions. In particular, it should never be thrown out with general industrial or domestic waste.

DISPOSAL SERVICE

Devices requiring disposal may be returned to the Mullard Service Department. They must be separately and securely packed and clearly identified. If any are damaged or broken they MUST NOT be sent through the post. In this case, advice is available from:

THE SERVICE DEPARTMENT
MULLARD LIMITED
P.O. BOX 142
NEW ROAD
MITCHAM
SURREY, CR4 4SR.

N-P-N SILICON PLANAR V.H.F./U.H.F. TRANSISTOR

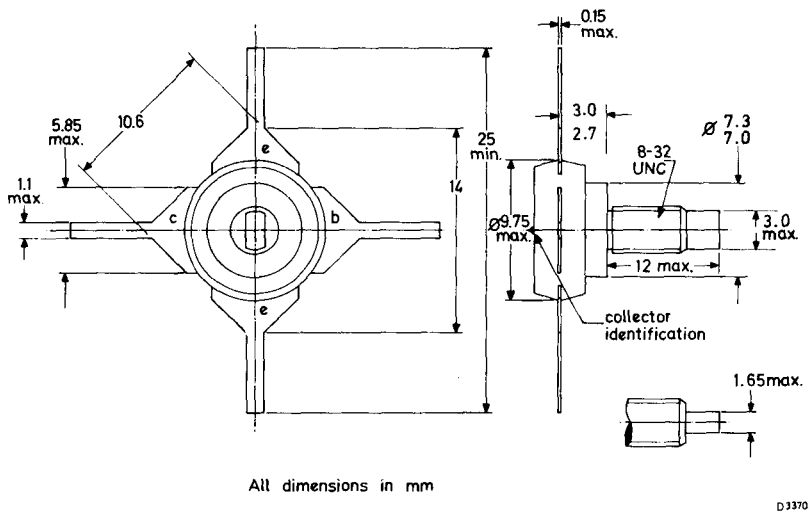
BLX67

Silicon n-p-n transistor for v.h.f./u.h.f. mobile applications. The device is mounted in a plastic, capstan strip-line encapsulation. With a supply voltage of 13.8V and a signal frequency of 470MHz, the BLX67 will produce typically 3W output into a 50Ω load.

QUICK REFERENCE DATA

V_{CC} (V)	f (MHz)	P_{DR} (W)	P_L into 50Ω (W)	η (%)	T_h (°C)	Circuit
12.5	470	0.35	2.5 min.	65 min.	25	Un-neutralised common-emitter class B
13.8	470	0.35	3.0 typ.	79 typ.	25	
13.8	470	0.15	1.5 typ.	65 typ.	25	
12.5	175	0.03	3.0 typ.	84 typ.	25	

OUTLINE AND DIMENSIONS



All dimensions in mm

D3370

ACCESSORIES

Nut and lock-washer supplied with device

Torque on nut: min. 0.75Nm (7.5kg cm)
max. 0.85Nm (8.5kg cm)

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{CBOM} max.	36	V
V_{CESM} max. (R_{BE} = 0)	36	V
V_{CEO} max.	18	V
V_{EBO} max.	4.0	V
I_C max.	0.7	A
I_{CM} max. ($f \geq 10MHz$)	2.0	A
P_{tot} max. ($f \geq 10MHz$, $T_h \leq 90^oC$)	4.5	W

See also graph on page 3

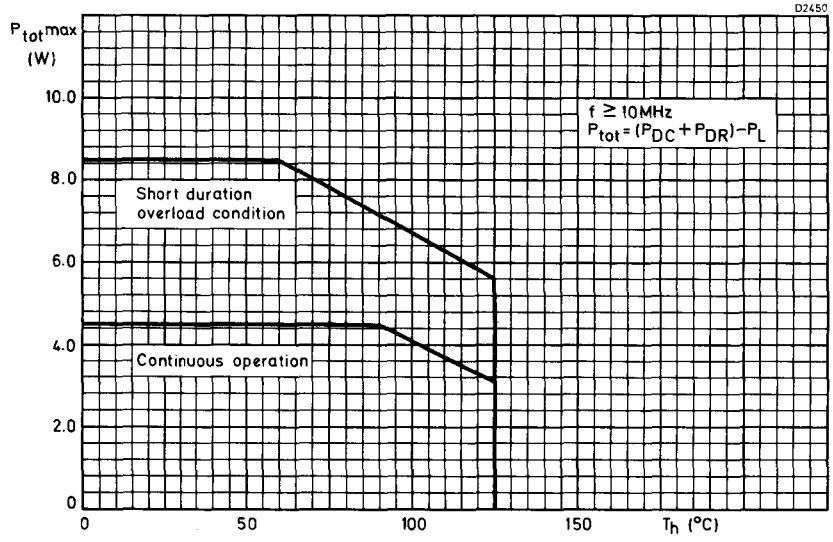
Temperature

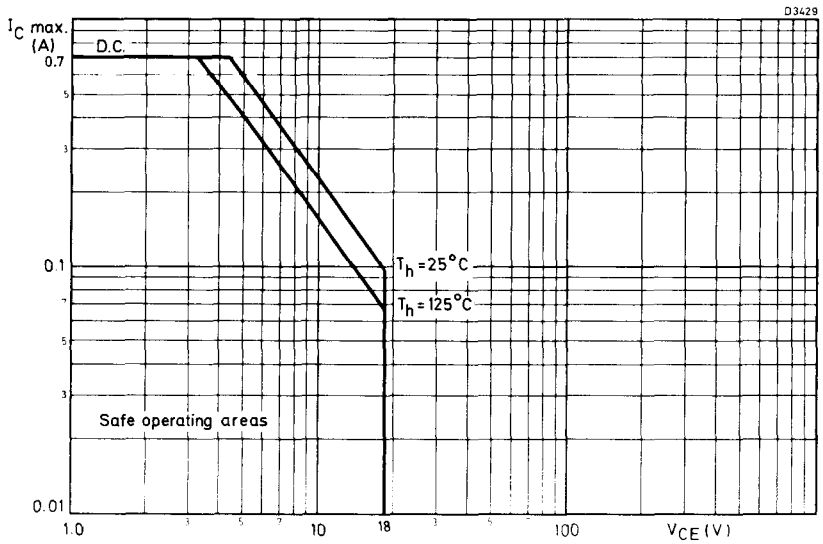
T_{stg}	-65 to +150	^oC

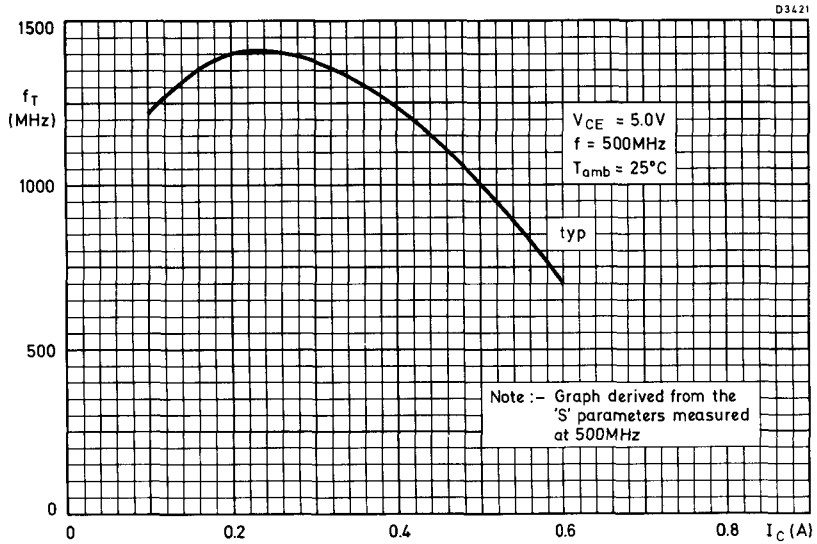
ELECTRICAL CHARACTERISTICS ($T_j = 25^oC$ unless otherwise stated)

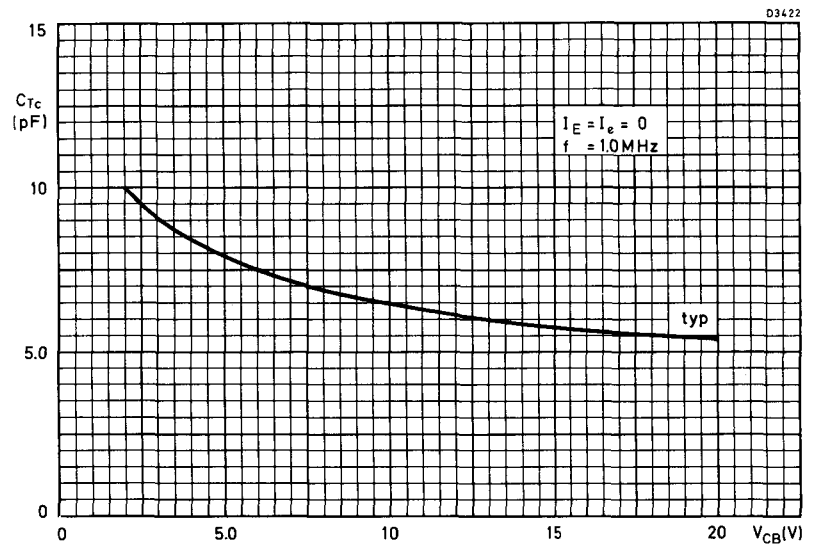
		Min.	Typ.	Max.	
$V_{(BR)CBO}$	Collector-base breakdown voltage I_C = 10mA	36	-	-	V
$V_{(BR)CES}$	Collector-emitter breakdown voltage I_C = 10mA, R_{BE} = 0	36	-	-	V
$V_{(BR)CEO}$	Collector-emitter breakdown voltage I_C = 25mA	18	-	-	V
$V_{(BR)EBO}$	Emitter-base breakdown voltage I_E = 1.0mA	4.0	-	-	V
$V_{CE(sat)}$	Collector-emitter saturation voltage I_C = 100mA, I_B = 20mA	-	0.1	-	V
h_{FE}	Static forward current transfer ratio I_C = 100mA, V_{CE} = 5.0V	10	40	-	
*f_T	Transition frequency I_C = 200mA, V_{CE} = 5.0V, f = 500MHz	-	1400	-	MHz
C_{Tc}	Collector capacitance V_{CB} = 10V, $I_E = I_e$ = 0, f = 1.0MHz	-	6.5	9.0	pF
C_{cs}	Collector-stud capacitance	-	2.0	-	pF

*Derived from the 'S' parameters measured at f = 500MHz, $T_{amb} = 25^oC$


D2450
P_{tot}max (W)
10.0
8.0
6.0
4.0
2.0
0
f ≥ 10MHz
$P_{tot} = (P_{DC} + P_{DR}) - P_L$
Short duration overload condition
Continuous operation
0
50
100
150
T_h (°C)


D3429
I_C max. (A)
D.C.
0.7
0.1
0.01
T_h = 25°C
T_h = 125°C
Safe operating areas
1.0
10
18
100
V_{CE} (V)


D3421
1500
f_T (MHz)
1000
500
0
0
0.2
0.4
0.6
0.8
I_C (A)
V_{CE} = 5.0V
f = 500MHz
T_{amb} = 25°C
typ
Note :- Graph derived from the 'S' parameters measured at 500MHz


D3422
15
C_{Tc} (pF)
10
5.0
0
0
5.0
10
15
20
V_{CB}(V)
$I_E = I_e = 0$
f = 1.0MHz
typ

APPLICATION INFORMATION

R.F. performance in c.w. operation (T_h = 25°C)

V_{CC} (V)	f (MHz)	P_{DR} (W)	P_L into 50Ω (W)	η (%)	$\overline{z_i}$ (Ω)	$\overline{Y_L}$ (mmho)
12.5	470	0.35	2.5 min.	65 min.	-	-
13.8	470	0.35	3.0 typ.	79 typ.	3+j5	27-j38
13.8	470	0.15	1.5 typ.	65 typ.	-	-
12.5	175	0.03	3.0 typ.	84 typ.	2.4-j3.8	35-j40

At P_L = 2.5W and V_{CC} = 12.5V, the output power at heatsink temperatures between 25 and 90°C relative to that at 25°C is diminished typically by 5mW/°C.

The transistor is designed to withstand full load mismatch in the test circuit under the following conditions:

V_{CC} = 16.5V, f = 470MHz T_h = 70°C

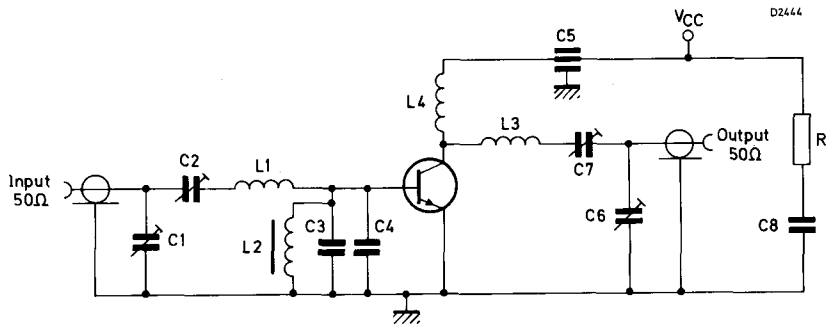
V.S.W.R. = 50:1 at any phase

$P_{DR} = P_{DR}$ nom. +20%

Where P_{DR} nom. = P_{DR} for 2.5W transistor output into a 50Ω load at V_{CC} = 13.8V.

APPLICATION INFORMATION (contd.)

470MHz Amplifier circuit

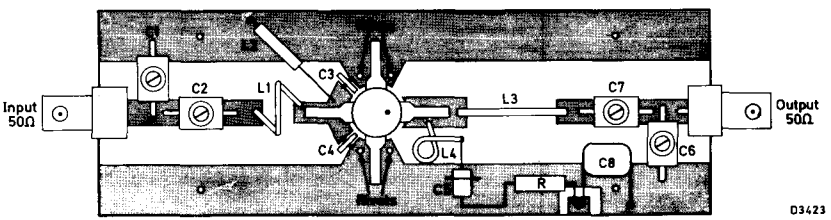


Component values for 470MHz amplifier circuit

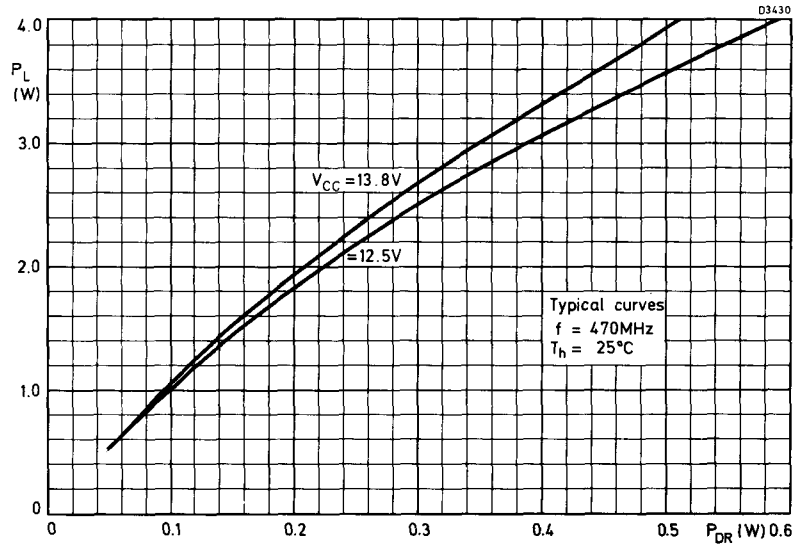
C1 = C2 = C6 = C7 = 1.8 to 18pF film dielectric trimmers
C3 = C4 = 18pF disc ceramic capacitors
C5 = 4nF feed-through capacitor
C8 = 0.1μF disc ceramic capacitor
L1 = 1 turn of 1.2mm copper wire, int. dia. 6mm, lead length <1mm
L2 = 1μH choke
L3 = 30mm of straight 2mm copper wire. Height above board = 2mm
L4 = 2 turns of 0.5mm copper wire int. dia. 3mm, close wound, lead length = 8mm
R = 10Ω - carbon

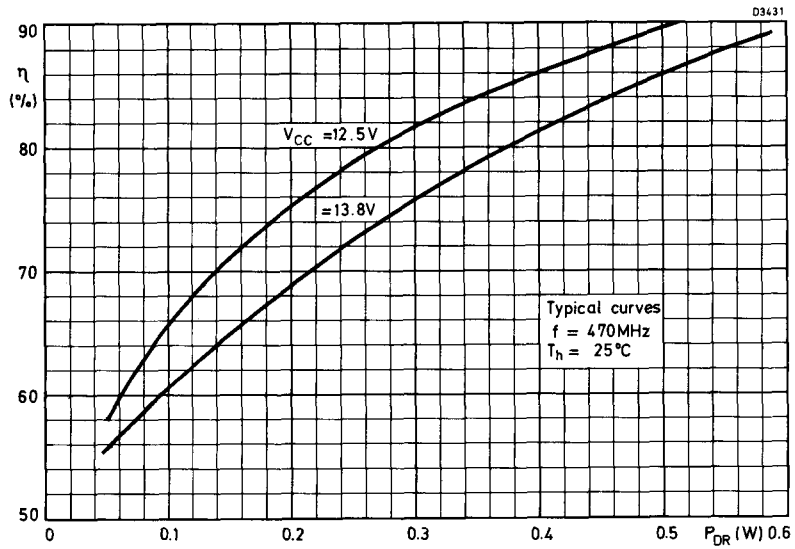
Component layout on 1.5mm double copper clad fibre-glass board

Dimensions of the board: - 110 × 50mm

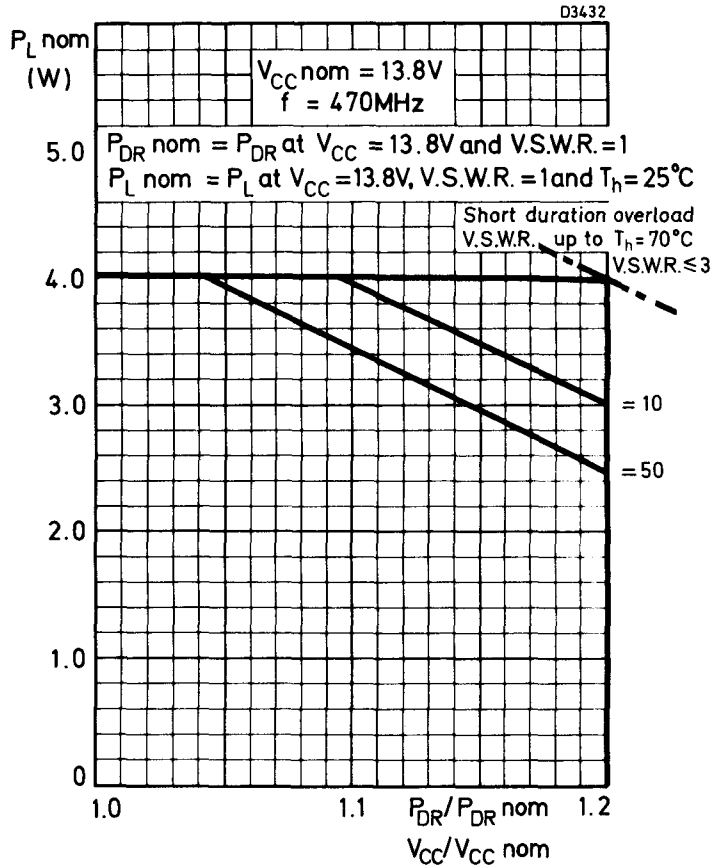


Shaded area copper
Underside area completely copper clad





TYPICAL VARIATION OF LOAD POWER AND EFFICIENCY WITH DRIVE POWER



INDICATED LOAD POWER AS A FUNCTION OF OVERLOAD

The transistor is suitable for use with unstabilised supply voltages. The above graph has been derived from an evaluation of the performance of transistors matched up to 4 watts load power in the circuit on page 6, and subsequently subjected to various voltage overloads and mismatch conditions with v.s.w.r. up to 50: 1 at a heatsink temperature of 70°C. This indicates a restriction to the load power matched under nominal conditions with varying supply voltages and v.s.w.r. in the recommended circuit.

CAUTION

This device incorporates Beryllium Oxide, the dust of which is toxic. The device is entirely safe provided that it is not dismantled.

Care should be taken to ensure that all those who may handle, use or dispose of this device are aware of its nature and of the necessary safety precautions. In particular, it should never be thrown out with general industrial or domestic waste.

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THE SERVICE DEPARTMENT
MULLARD LIMITED
P.O. BOX 142
NEW ROAD
MITCHAM
SURREY, CR4 4SR.

N-P-N SILICON PLANAR EPITAXIAL U.H.F. TRANSISTOR

BLX69

N-P-N epitaxial planar transistor intended for use in class A, B and C operated mobile, industrial and military transmitters with a supply voltage of 13.5 V. The transistor is resistance stabilized. Every transistor is tested under severe load mismatch conditions with a supply overvoltage to 16.5 V. It has a capstan envelope with a moulded cap. All leads are isolated from the stud.

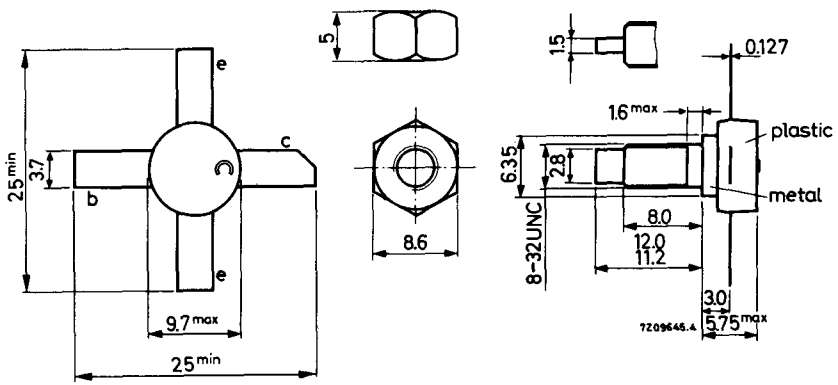
QUICK REFERENCE DATA

R.F. performance up to T_{mb} = 25 °C in an unneutralised common-emitter class B circuit.

Mode of operation	V_{CC} (V)	f (MHz)	P_S (W)	P_L (W)	I_C (A)	G_p (dB)	η (%)	$\overline{z_i}$ (Ω)	$\overline{Y_L}$ (mA/V)
c.w.	13.5	470	< 8	20	< 2.28	> 4	> 65	1.1 + j4.9	190-j45
c.w.	12.5	470	< 6.8	17	< 2.09	> 4	> 65		

MECHANICAL DATA

Dimensions in mm



Torque on nut: min. 7.5 kg cm
(0.75 Newton metres)
max. 8.5 kg cm
(0.85 Newton metres)

Diameter of clearance hole in heatsink: max. 4.17 mm.
Mounting hole to have no burrs at either end. De-burring must leave surface flat; do not chamfer or countersink either end of hole.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages

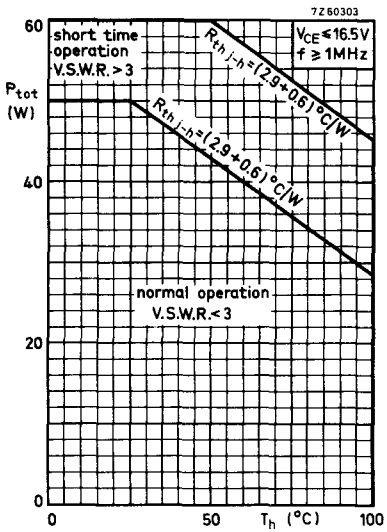
Collector-base voltage (open emitter) peak value	V_{CBOM}	max.	36	V
Collector-emitter voltage (open base)	V_{CEO}	max.	18	V
Emitter-base voltage (open collector)	V_{EBO}	max.	4	V

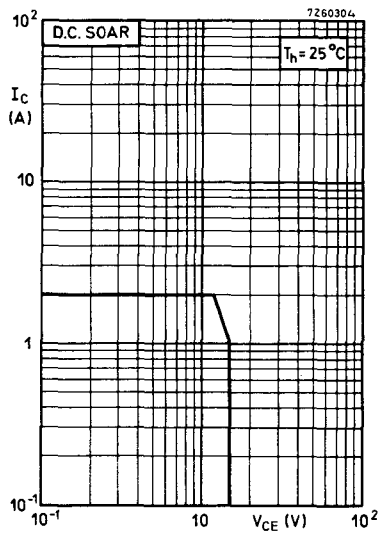
Currents

Collector current (average)	$I_{C(AV)}$	max.	3.5	A
Collector current (peak value) f > 1 MHz	I_{CM}	max.	10	A

Power dissipation

Total power dissipation up to T_h = 25 °C f > 1 MHz	P_{tot}	max.	50	W





Temperature

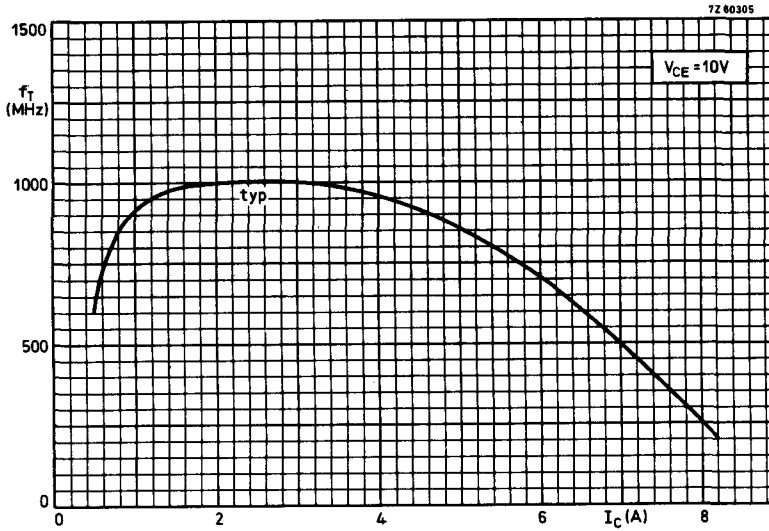
Storage temperature	T_{stg}		−30 to +200	°C
Operating junction temperature	T_j	max.	200	°C

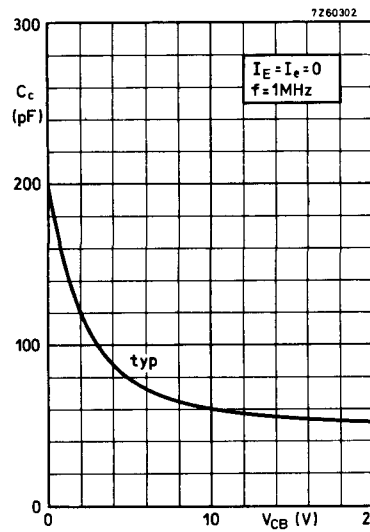
THERMAL RESISTANCE

From junction to mounting base	$R_{th\ j-mb}$ =	2.9	°C/W
From mounting base to heatsink	$R_{th\ mb-h}$ =	0.6	°C/W

CHARACTERISTICS T_j = 25 °C unless otherwise specified

Breakdown voltages				
Collector-base voltage open emitter, I_C = 25 mA	$V_{(BR)CBO}$	>	36	V
Collector-emitter voltage open base, I_C = 25 mA	$V_{(BR)CEO}$	>	18	V
Emitter-base voltage open collector; I_E = 10 mA	$V_{(BR)EBO}$	>	4	V
Transient energy				
L = 25 mH; f = 50 Hz				
open base	E	>	3.1	mWs
$-V_{BE}$ = 1.5 V; R_{BE} = 33 Ω	E	>	3.1	mWs
D.C. current gain				
I_C = 1 A; V_{CE} = 5 V	h_{FE}	> typ.	10 30	
Transition frequency				
I_C = 2 A; V_{CE} = 10 V	f_T	typ.	1.0	GHz
Collector capacitance at f = 1 MHz				
$I_E = I_e$ = 0; V_{CB} = 15 V	C_c	typ. <	55 70	pF pF
Feedback capacitance				
I_C = 100 mA; V_{CE} = 15 V	$-C_{re}$	typ.	32	pF
Collector-stud capacitance	C_{cs}	typ.	2	pF


7Z60305
1500
f_T (MHz)
1000
500
0
V_{CE} = 10V
typ
0
2
4
6
I_C (A)
8


7Z60302
300
C_c (pF)
200
100
0
$I_E = I_e = 0$
f = 1MHz
typ
0
10
V_{CB} (V)
20

N-P-N SILICON PLANAR EPITAXIAL U.H.F. TRANSISTOR

BLX69

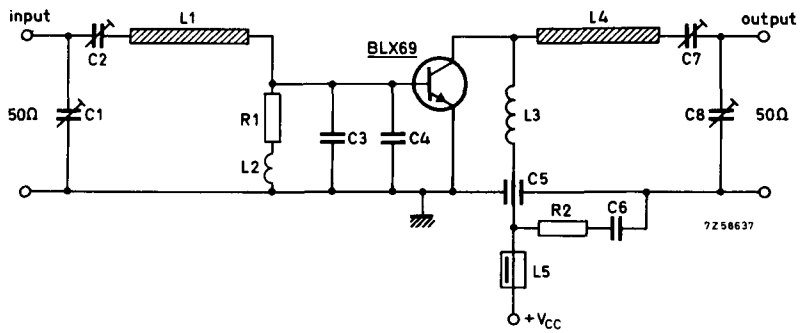
APPLICATION INFORMATION

R. F. performance in c. w. operation (unneutralised common-emitter class B ciruit)

T_{mb} up to 25 °C

f (MHz)	V_{CC} (V)	P_S (W)	P_L (W)	I_C (A)	G_p (dB)	η (%)	$\overline{z_i}$ (Ω)	$\overline{Y_L}$ (mA/V)
470	13.5	< 8	20	< 2.28	> 4	> 65	1.1 + j4.9	190-j45
470	12.5	< 6.8	17	< 2.09	> 4	> 65		
175	12.5	typ. 1.35	17	typ. 2.3	typ. 11	typ. 60	1.5 + j0.6	170-j57

Test circuit for 470 MHz:



List of components:

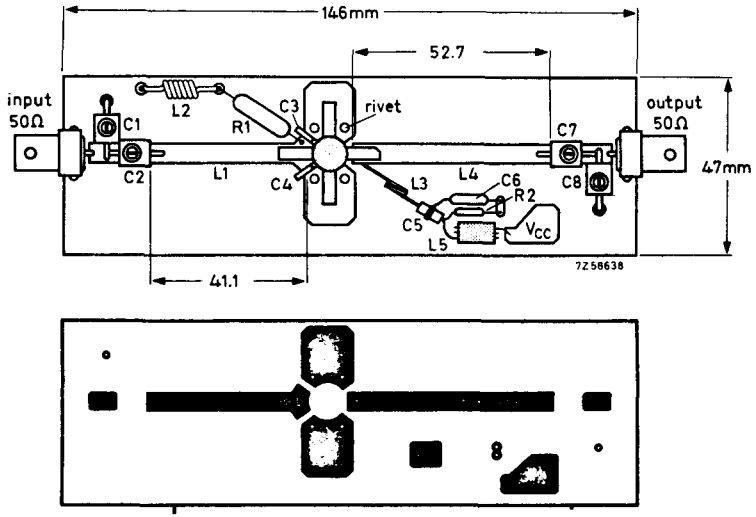
C1=C2=C7=C8=1.8 to 9.0 pF film dielectric trimmer
C3=C4= 15 pF chip capacitor
C5= 100 pF feed through capacitor
C6= 33 nF polyester capacitor
R1= 1 Ω
R2= 10 Ω
L1= strip-line (41.1 mm x 5.0 mm)
L2= 13 turns closely wound enamelled Cu wire (0.5 mm); int. diam. 4.0 mm (0.32 μH)
L3= 2 turns Cu wire (1 mm); winding pitch 1.5 mm; int. diam. 4 mm; leads 2x5 mm
L4= strip-line (52.7 mm x 5.0 mm)
L5= ferroxcube choke coil. Z (at f = 250 MHz) = 400 Ω ± 20%

L1 and L4 are strip lines on a double Cu clad print plate with teflon fibre glass dielectric
(ϵ_r = 2.74); thickness 1.45 mm

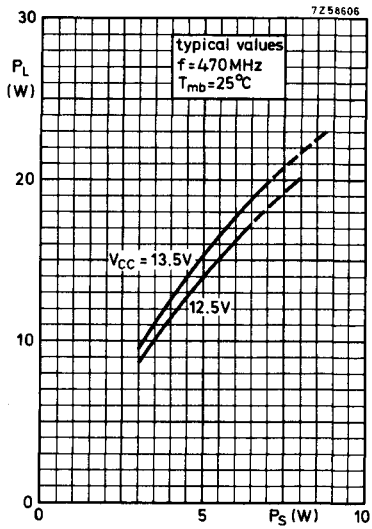
Component lay-out for 470 MHz: see page 6

APPLICATION INFORMATION (continued)

Component lay-out and printed circuit board for 470 MHz test circuit.



The circuit and the components are situated on one side of the epoxy fibre-glass board, the other side being fully metallised to serve as earth. Earth connections are made by means of hollow rivets.



N-P-N SILICON PLANAR EPITAXIAL U.H.F. TRANSISTOR

BLX69

CAUTION

This device incorporates Beryllium Oxide, the dust of which is toxic. The device is entirely safe provided that it is not dismantled.

Care should be taken to ensure that all those who may handle, use or dispose of this device are aware of its nature and of the necessary safety precautions. In particular, it should never be thrown out with general industrial or domestic waste.

DISPOSAL SERVICE

Devices requiring disposal may be returned to the Mullard Service Department. They must be separately and securely packed and clearly identified. If any are damaged or broken they MUST NOT be sent through the post. In this case, advice is available from:

THE SERVICE DEPARTMENT
MULLARD LIMITED
2.NEW ROAD, MITCHAM JUNCTION
SURREY, CR4 4XY.

N-P-N SILICON PLANAR U.H.F. TRANSISTOR

BLX91

TENTATIVE DATA

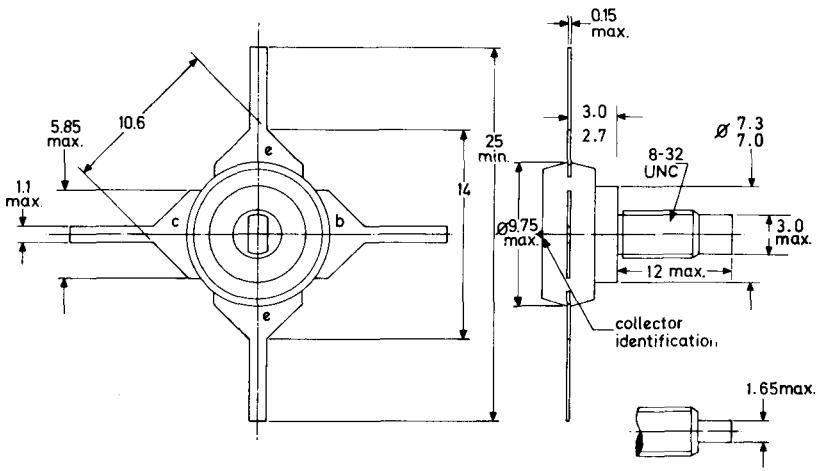
Silicon n-p-n transistor designed for u.h.f. operation in class A, B or C with frequencies up to 1GHz. The device is mounted in a plastic, capstan, strip-line encapsulation.

With a supply voltage of 28V and a signal frequency of 470MHz, the BLX91 will produce 1.0W output into a 50Ω load.

QUICK REFERENCE DATA

V_{CC} (V)	f (MHz)	P_{DR} (W)	P_L into 50Ω (W)	η (%)	T_h (°C)	Circuit
28	470	0.08	1.0 min.	50 min.	25	Un-neutralised common-emitter class B
28	470	0.08	1.45 typ.	60 typ.	25	

OUTLINE AND DIMENSIONS



All dimensions in mm

D3370

ACCESSORIES

Nut and lock-washer supplied with device

Torque on nut: min. 0.75Nm (7.5kg cm)
max. 0.85Nm (8.5kg cm)

RATINGS

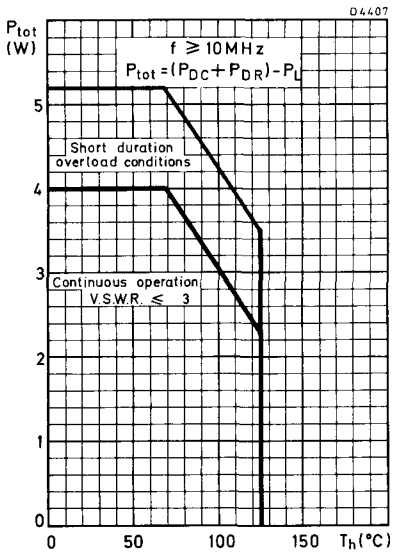
Limiting values of operation according to the absolute maximum system.

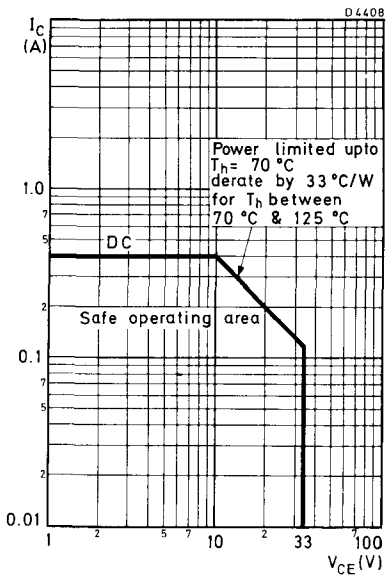
Electrical

V_{CBOM}	max.	65	V
V_{CESM}	max. (R_{BE} = 0)	65	V
V_{CEO}	max.	33	V
V_{EBO}	max.	4.0	V
I_C	max.	400	mA
I_{CM}	max. (f ≥ 10MHz)	800	mA
P_{tot}	max. (f ≥ 10MHz, $T_h \leq 70^oC$) see also graphs below	4.0	W

Temperature

T_{stg}	-65 to +150	^oC

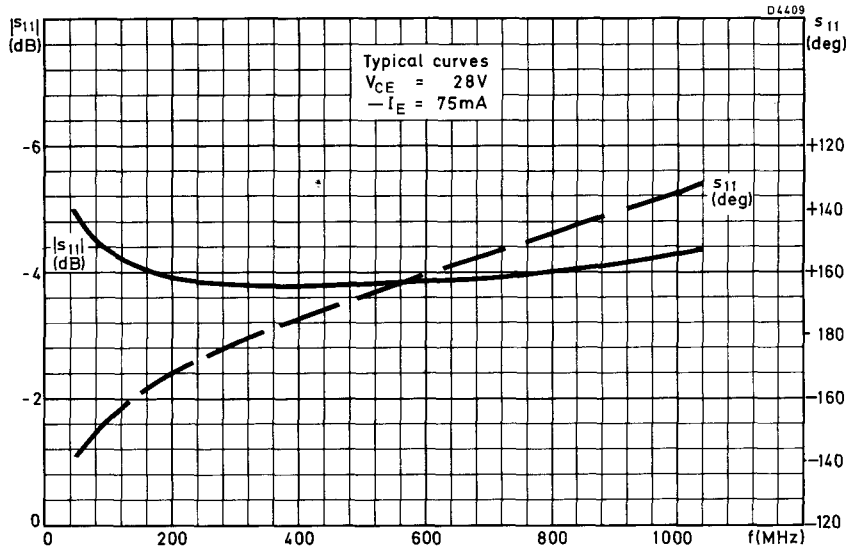


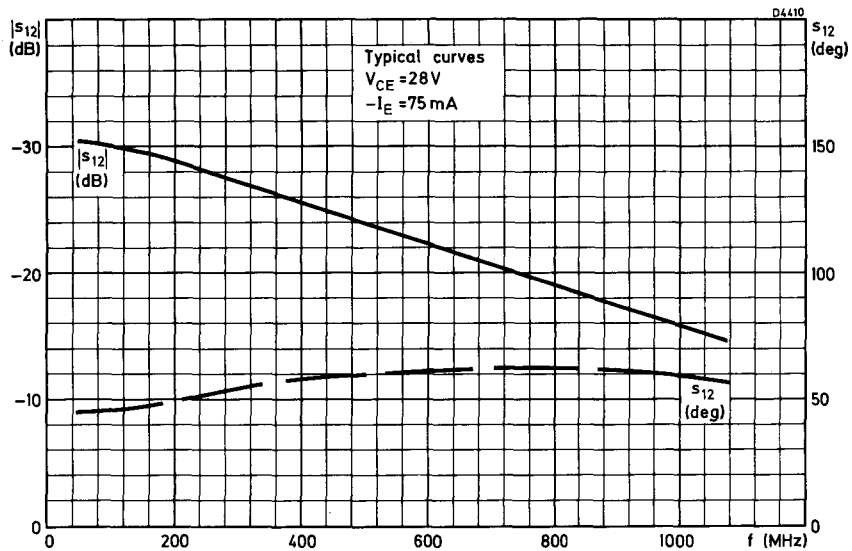


ELECTRICAL CHARACTERISTICS ($T_j = 25^oC$ unless otherwise stated)

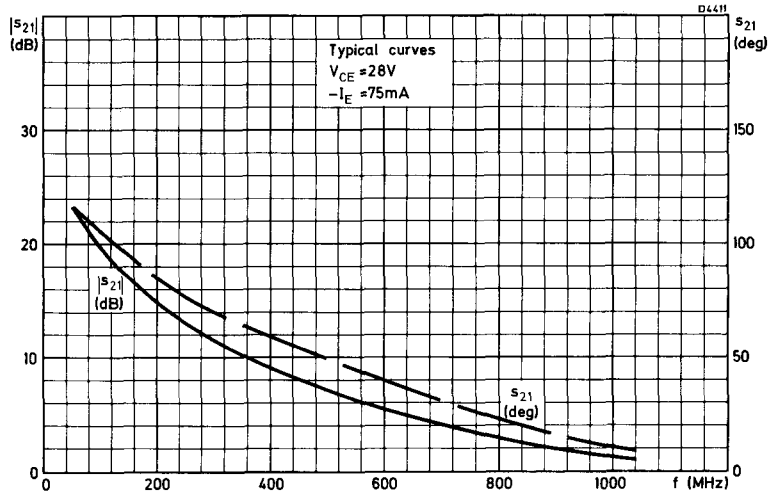
		Min.	Typ.	Max.	
$V_{(BR)CBO}$	Collector-base breakdown voltage I_C = 10mA	65	-	-	V
$V_{(BR)CES}$	Collector-emitter breakdown voltage I_C = 10mA, R_{BE} = 0	65	-	-	V
$V_{(BR)CEO}$	Collector-emitter breakdown voltage I_C = 25mA	33	-	-	V
$V_{(BR)EBO}$	Emitter-base breakdown voltage I_E = 1.0mA	4.0	-	-	V
h_{FE}	Static forward current transfer ratio I_C = 100mA, V_{CE} = 5.0V	10	35	-	
*f_T	Transition frequency I_C = 50mA, V_{CE} = 5.0V, f = 500MHz	-	1200	-	MHz
C_{Tc}	Collector capacitance V_{CB} = 10V, $I_E = I_e$ = 0, f = 1.0MHz	-	3.5	-	pF
C_{Te}	Emitter capacitance V_{EB} = 0, $I_C = I_c$ = 0, f = 1.0MHz	-	11	-	pF
C_{cs}	Collector-stud capacitance	-	2.0	-	pF

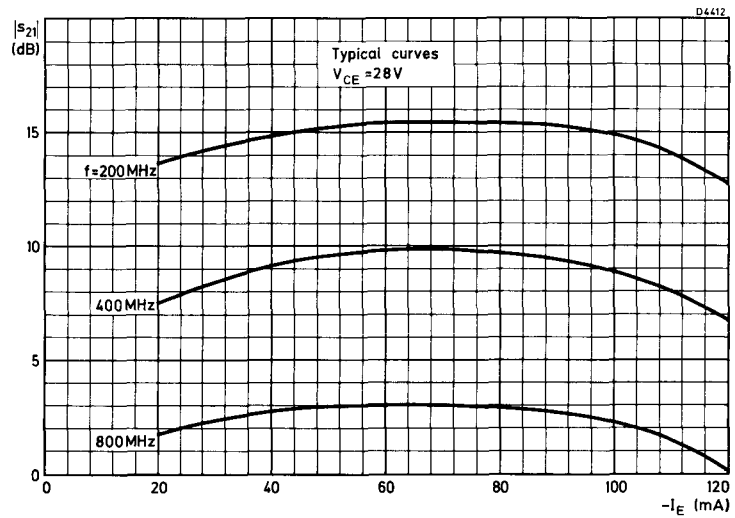
*Derived from the 's' parameters measured at f = 500MHz, $T_{amb} = 25^oC$



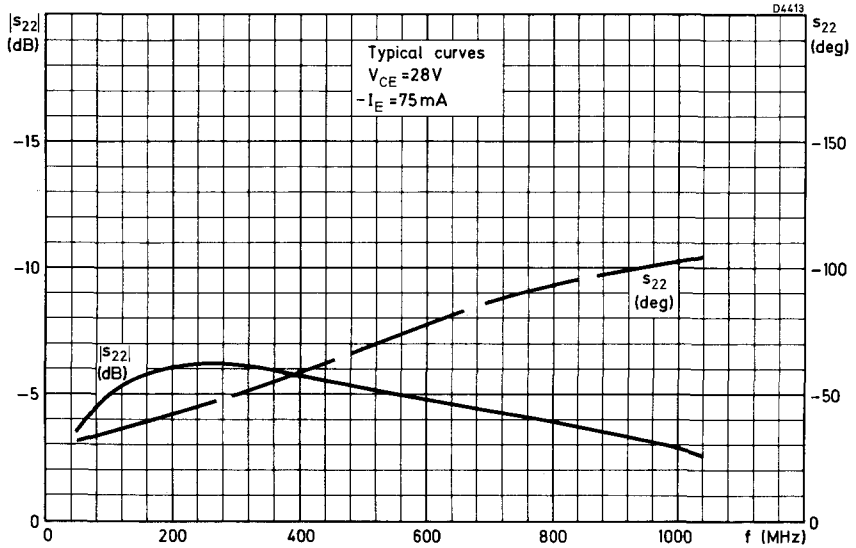


TYPICAL VARIATION OF INPUT REFLECTION COEFFICIENT AND FEEDBACK COEFFICIENT WITH FREQUENCY

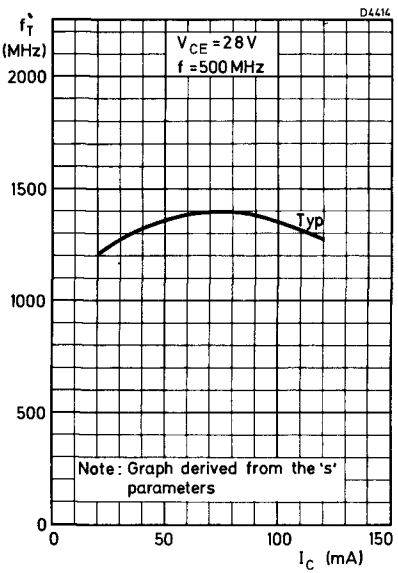


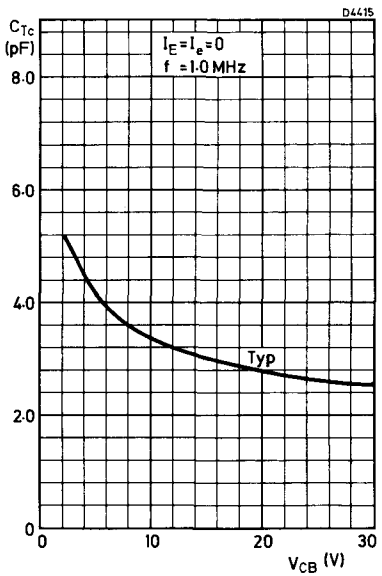


TYPICAL VARIATION OF FORWARD TRANSFER COEFFICIENT WITH FREQUENCY AND EMITTER CURRENT



TYPICAL VARIATION OF OUTPUT REFLECTION COEFFICIENT WITH FREQUENCY





APPLICATION INFORMATION

R. F. Performance in c.w. operation (T_h = 25°C)

V_{CC} (V)	f (MHz)	P_{DR} (W)	P_L into 50Ω (W)	η (%)	$\bar{z}_i$ (Ω)	$\bar{Y}_L$ (mmho)
24	470	0.05	0.85 typ.	53 typ.	-	-
28	470	0.08	1.0 min.	50 min.	-	-
28	470	0.08	1.45 typ.	60 typ.	1.4 +j1.6	3.7-j22
28	1000	0.40	1.4 typ.	50 typ.	-	-

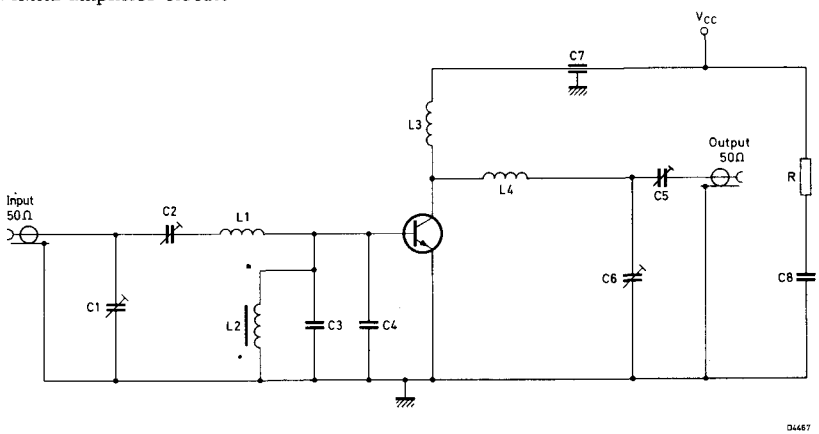
At P_L = 1.0W and V_{CC} = 28V, the output power at heatsink temperatures between 25 and 90°C relative to that at 25°C is diminished typically by 2mW/°C.

The transistor is designed to withstand full load mismatch in the test circuit under the following conditions: -

V_{CC} = 28V f = 470MHz T_h = 90°C

P_L = 1.2W V.S.W.R. = 50: 1 at any phase

470MHz amplifier circuit



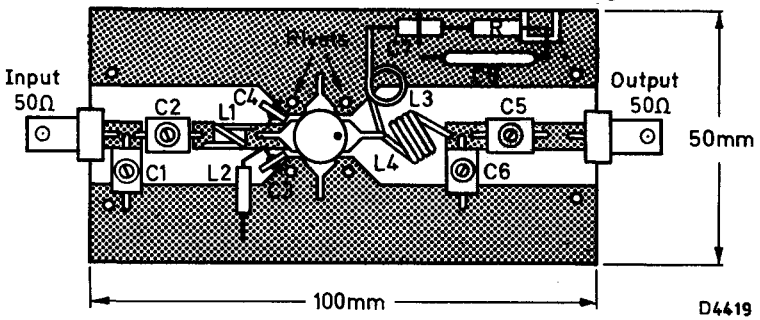
D4467

APPLICATION INFORMATION (contd.)

Component values for 470MHz amplifier circuit.

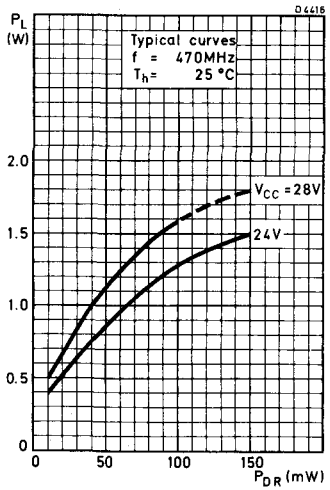
C1 = C2 = C5 = 1.8 to 18pF film-dielectric trimmer capacitors.
C3 = C4 = 18pF disc ceramic capacitors.
C6 = 1.0 to 9.0pF film-dielectric trimmer capacitors.
C7 = 1000pF feed-through capacitor.
C8 = 0.1μF ceramic capacitor.
L1 = 1 turn of 1.2mm Cu wire, internal diameter 5mm, lead length = 2mm.
L2 = 0.47μH choke.
L3 = 5 turns of 0.5mm Cu wire, internal diameter 4mm, lead length = 5mm, close wound.
L4 = 4 turns of 1.2mm Cu wire, internal diameter 6.5mm, lead length = 4mm, close wound.
R = 10Ω carbon.

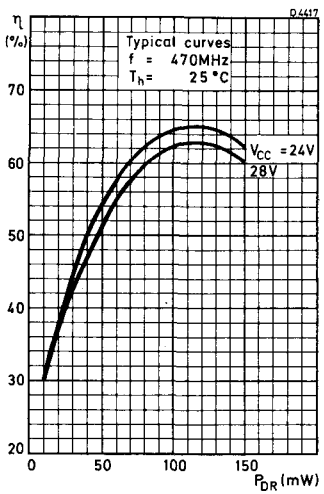
Component layout on 1.5mm double copper clad fibre glass board



Shaded area copper

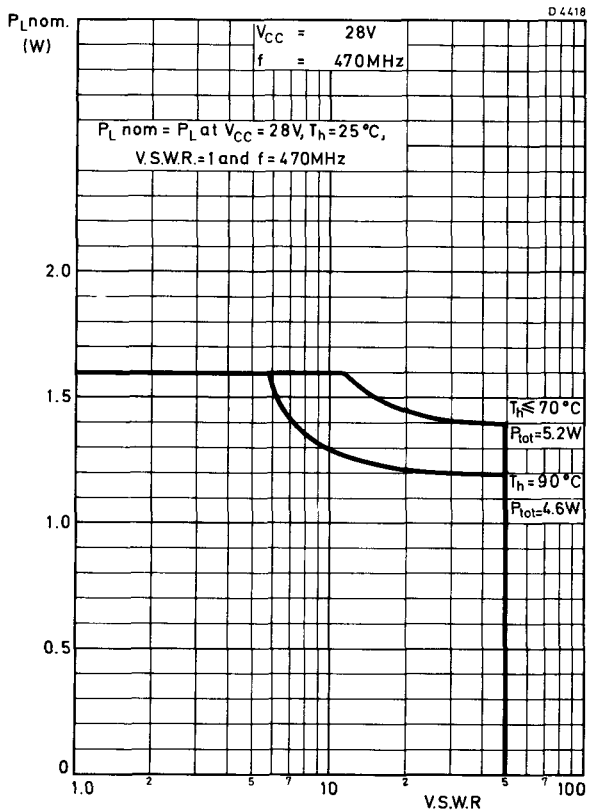
Underside area completely copper clad





TYPICAL VARIATION OF LOAD POWER AND EFFICIENCY WITH DRIVE POWER

APPLICATION INFORMATION (contd.)



INDICATED LOAD POWER AS A FUNCTION OF OVERLOAD

The above graph has been derived from an evaluation of the performance of transistors matched up to 1.6 watts load power in the test amplifier on Page 7 and subsequently subjected to various mismatch conditions at 28V with V.S.W.R. up to 50:1 and elevated heatsink temperatures. This indicates a restriction to the load power matched under nominal conditions in the recommended test configuration.

CAUTION

This device incorporates Beryllium Oxide, the dust of which is toxic. The device is entirely safe provided that it is not dismantled.

Care should be taken to ensure that all those who may handle, use or dispose of this device are aware of its nature and of the necessary safety precautions. In particular, it should never be thrown out with general industrial or domestic waste.

DISPOSAL SERVICE

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MULLARD LIMITED
P.O. BOX 142
NEW ROAD
MITCHAM
SURREY, CR4 4SR.

N-P-N SILICON PLANAR U.H.F. TRANSISTOR

BLX92

TENTATIVE DATA

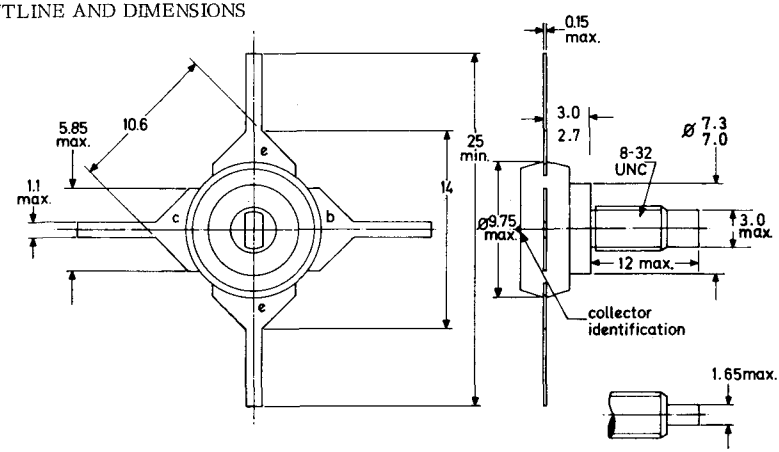
Silicon n-p-n transistor designed for u.h.f. operation in class A, B or C with frequencies up to 1GHz. The device is mounted in a plastic, capstan, strip-line encapsulation.

With a supply voltage of 28V and a signal frequency of 470MHz, the BLX92 will produce 2.5W output into a 50Ω load.

QUICK REFERENCE DATA

V_{CC} (V)	f (MHz)	P_{DR} (W)	P_L into 50Ω (W)	η (%)	T_h (^oC)	Circuit
24	470	0.2	2.4 typ.	70 typ.	25	Un-neutralised common-emitter class B
28	470	0.2	2.5 min.	60 min.	25	
28	470	0.2	3.0 typ.	66 typ.	25	
28	1000	0.7	2.5 typ.	50 typ.	25	

OUTLINE AND DIMENSIONS



All dimensions in mm

ACCESSORIES

Nut and lock-washer supplied with device

Torque on nut: min. 0.75Nm (7.5kg cm)
max. 0.85Nm (8.5kg cm)

RATINGS

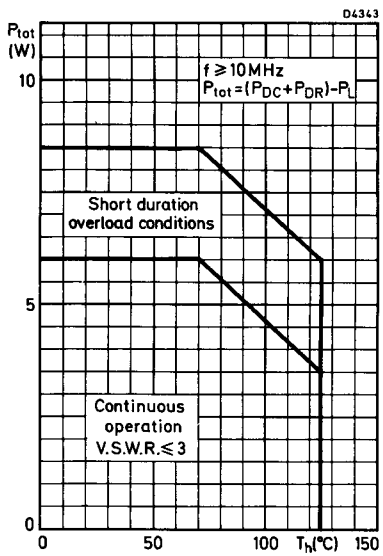
Limiting values of operation according to the absolute maximum system.

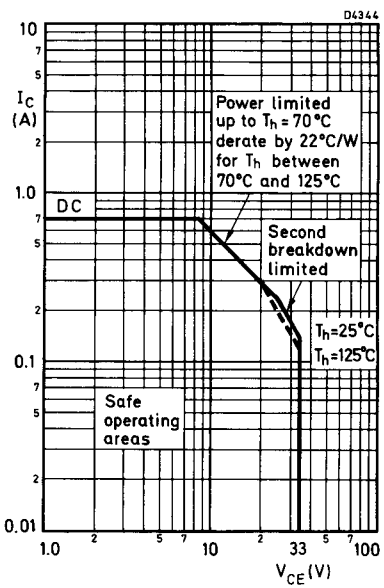
Electrical

V_{CBOM} max.		65	V
V_{CESM} max.	(R_{BE} = 0)	65	V
V_{CEO} max.		33	V
V_{EBO} max.		4.0	V
I_C max.		0.7	A
I_{CM} max.	(f ≥ 10MHz)	2.0	A
P_{tot} max.	(f ≥ 10MHz, $T_h \leq 70^oC$)	6.0	W
	See also graphs below		

Temperature

T_{stg}	-65 to +150	^oC

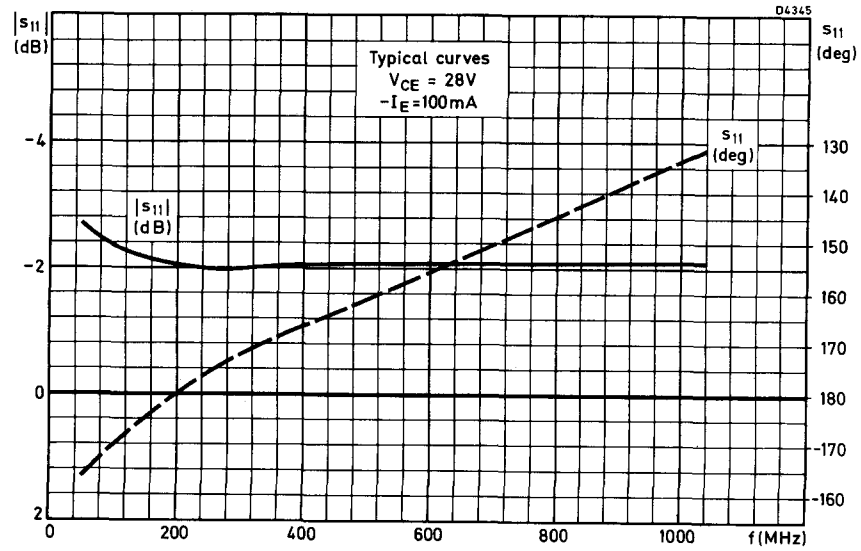


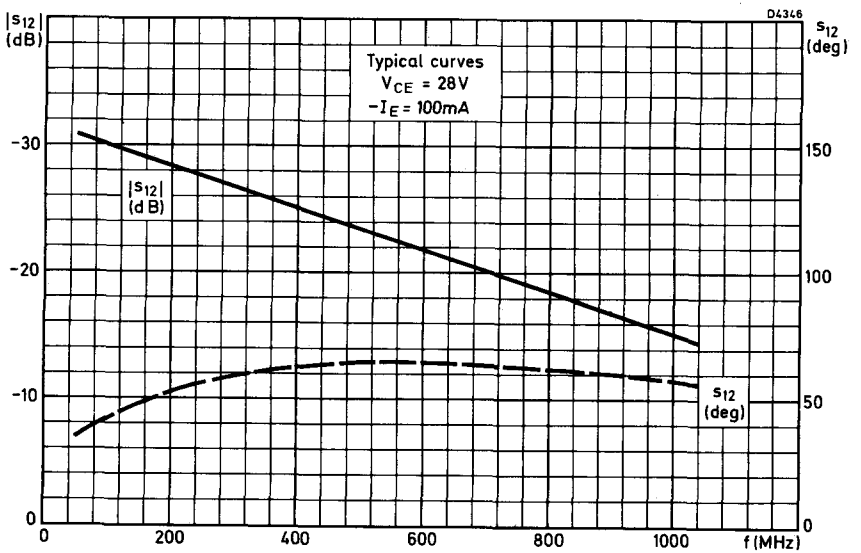


ELECTRICAL CHARACTERISTICS ($T_j = 25^oC$ unless otherwise stated)

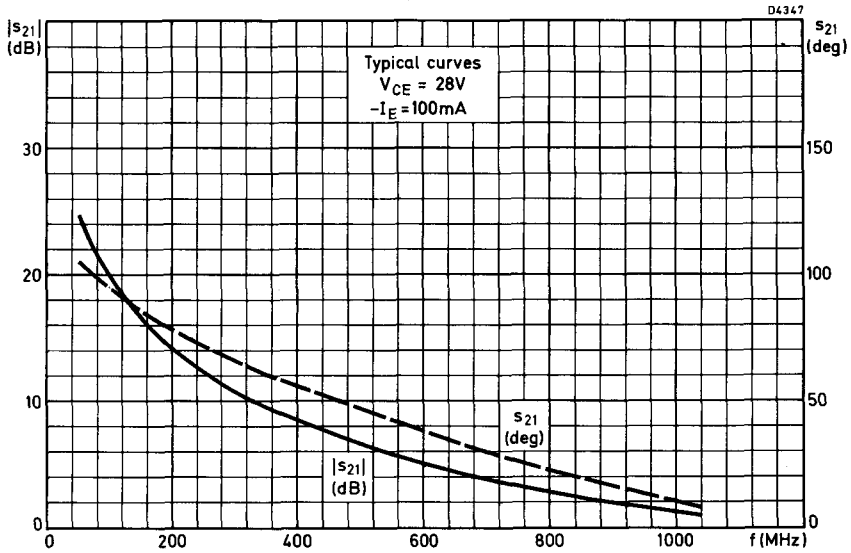
		Min.	Typ.	Max.	
$V_{(BR)CBO}$	Collector-base breakdown voltage I_C = 10mA	65	-	-	V
$V_{(BR)CES}$	Collector-emitter breakdown voltage I_C = 10mA, R_{BE} = 0	65	-	-	V
$V_{(BR)CEO}$	Collector-emitter breakdown voltage I_C = 25mA	33	-	-	V
$V_{(BR)EBO}$	Emitter-base breakdown voltage I_E = 1.0mA	4.0	-	-	V
$V_{CE(sat)}$	Collector-emitter saturation voltage I_C = 100mA, I_B = 20mA	-	0.17	-	V
h_{FE}	Static forward current transfer ratio I_C = 100mA, V_{CE} = 5.0V	10	40	-	
*f_T	Transition frequency I_C = 100mA, V_{CE} = 5.0V, f = 500MHz	-	1200	-	MHz
C_{Tc}	Collector capacitance V_{CB} = 10V, $I_E = I_e$ = 0, f = 1.0MHz	-	6.5	-	pF
C_{Te}	Emitter capacitance V_{EB} = 0, $I_C = I_c$ = 0, f = 1.0MHz	-	25	-	pF
C_{cs}	Collector-stud capacitance	-	2.0	-	pF

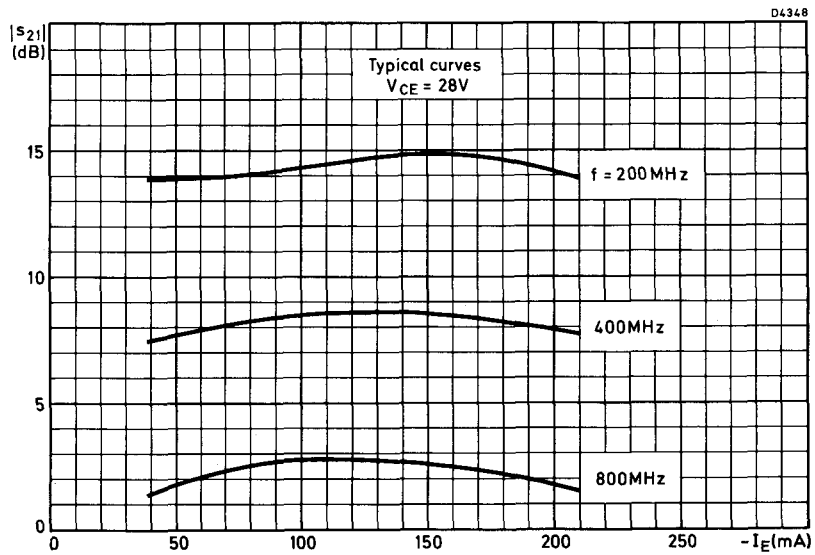
*Derived from the 's' parameters measured at f = 500MHz, $T_{amb} = 25^oC$



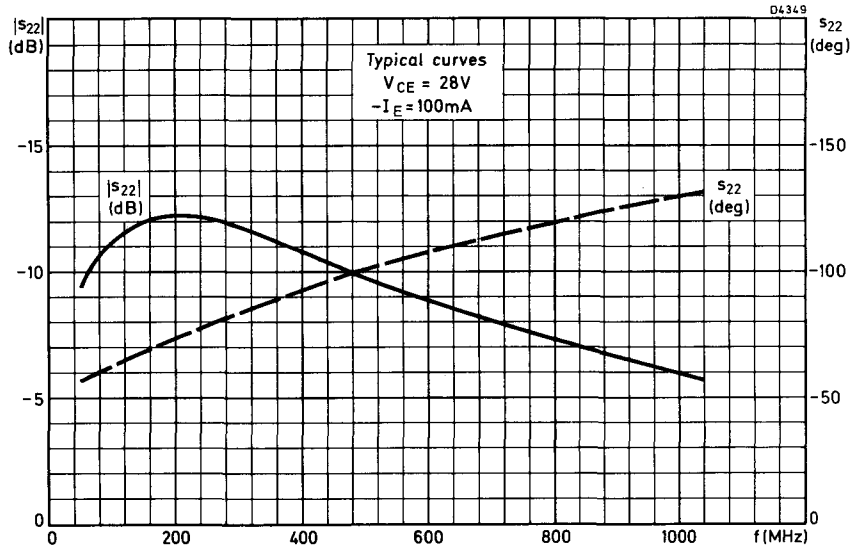


TYPICAL VARIATION OF INPUT REFLECTION COEFFICIENT AND FEEDBACK COEFFICIENT WITH FREQUENCY

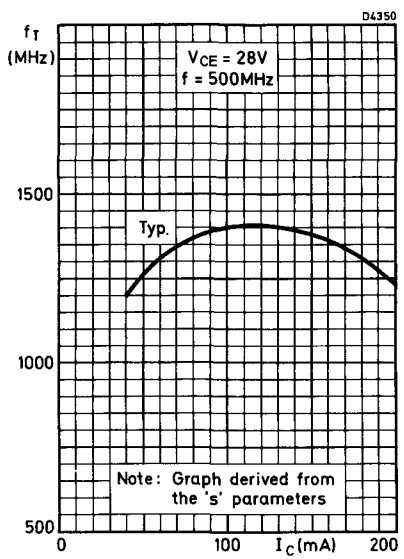


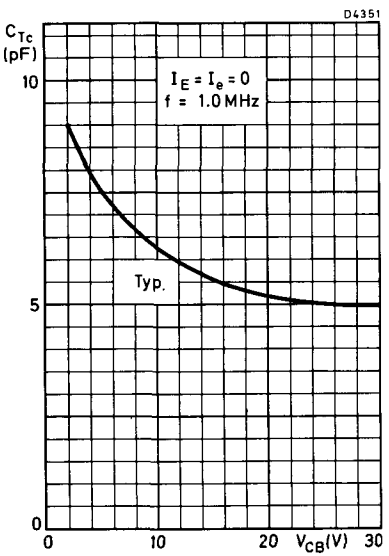


TYPICAL VARIATION OF FORWARD TRANSFER COEFFICIENT WITH FREQUENCY AND EMITTER CURRENT



TYPICAL VARIATION OF OUTPUT REFLECTION COEFFICIENT WITH FREQUENCY





APPLICATION INFORMATION

R. F. Performance in c.w. operation (T_h = 25°C)

V_{CC} (V)	f (MHz)	P_{DR} (W)	P_L into 50Ω (W)	η (%)	$\bar{z}_i$ (Ω)	$\bar{Y}_L$ (mmho)
24	470	0.2	2.5 typ.	70 typ.	-	-
28	470	0.2	2.5 min.	60 min.	-	-
28	470	0.2	3.0 typ.	66 typ.	1.6 +j3.4	7.7-j31
28	1000	0.7	2.5 typ.	50 typ.	-	-

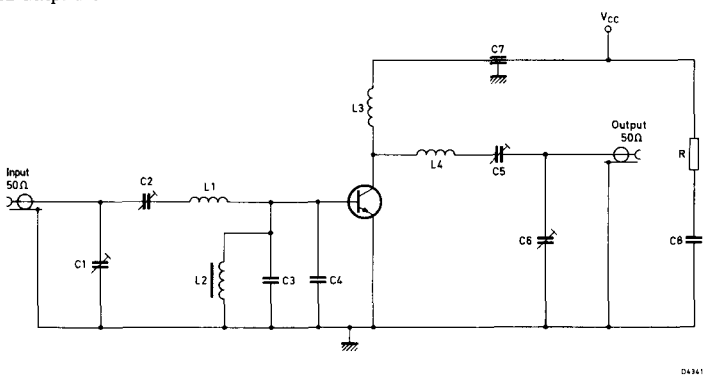
At P_L = 2.5W and V_{CC} = 28V, the output power at heatsink temperatures between 25 and 90°C relative to that at 25°C is diminished typically by 5mW/°C.

The transistor is designed to withstand full load mismatch in the test circuit under the following conditions: -

V_{CC} = 28V f = 470MHz T_h = 90°C

P_L = 2.5W V.S.W.R. = 50:1 at any phase

470MHz amplifier circuit

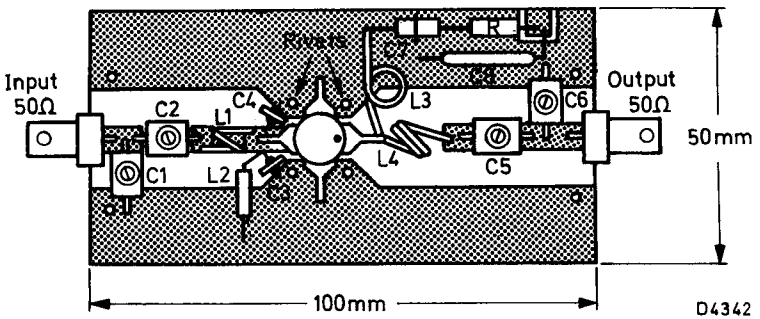


APPLICATION INFORMATION (contd.)

Component values for 470MHz amplifier circuit.

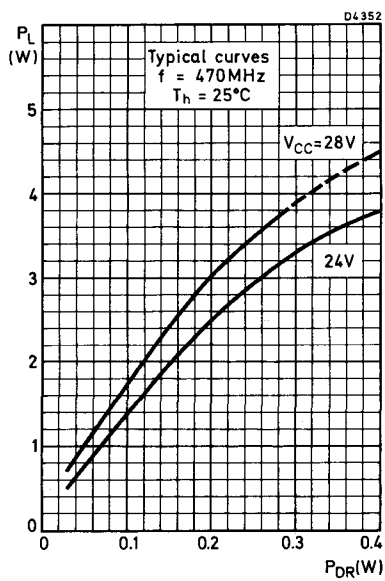
C1 = C2 = 1.8 to 18pF film-dielectric trimmer capacitors.
C3 = C4 = 18pF disc ceramic capacitors.
C5 = C6 = 1.0 to 9.0pF film-dielectric trimmer capacitors.
C7 = 1000pF feed-through capacitor.
C8 = 0.1μF ceramic capacitor.
L1 = 1 turn of 1.2mm Cu wire, internal diameter 5mm, lead length = 2mm.
L2 = 0.47μH choke.
L3 = 3 turns of 0.5mm Cu wire, internal diameter 4mm, lead length = 5mm
L4 = 2 turns of 1.2mm Cu wire, internal diameter 6.5mm, lead length = 4mm

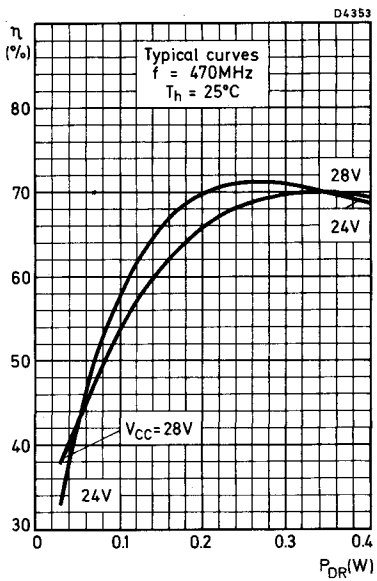
Component layout on 1.5mm double copper clad fibre glass board



Shaded area copper

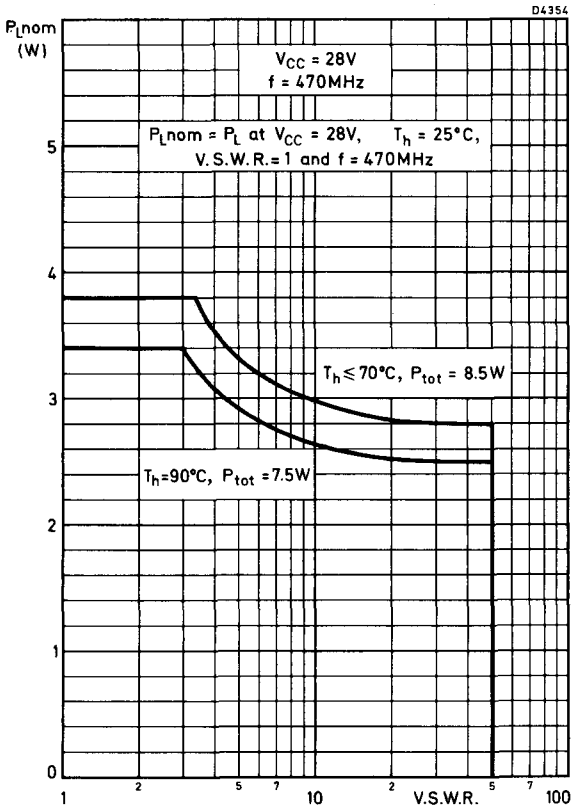
Underside area completely copper clad





TYPICAL VARIATION OF LOAD POWER AND EFFICIENCY WITH DRIVE POWER

APPLICATION INFORMATION (contd.)



INDICATED LOAD POWER AS A FUNCTION OF OVERLOAD

The above graph has been derived from an evaluation of the performance of transistors matched up to 3.8 watts load power in the test amplifier on Page 7 and subsequently subjected to various mismatch conditions at 28V with V.S.W.R. up to 50:1 and elevated heatsink temperatures. This indicates a restriction to the load power matched under nominal conditions in the recommended test configuration.

CAUTION

This device incorporates Beryllium Oxide, the dust of which is toxic. The device is entirely safe provided that it is not dismantled.

Care should be taken to ensure that all those who may handle, use or dispose of this device are aware of its nature and of the necessary safety precautions. In particular, it should never be thrown out with general industrial or domestic waste.

DISPOSAL SERVICE

Devices requiring disposal may be returned to the Mullard Service Department. They must be separately and securely packed and clearly identified. If any are damaged or broken they MUST NOT be sent through the post. In this case, advice is available from:

THE SERVICE DEPARTMENT
MULLARD LIMITED
P.O. BOX 142
NEW ROAD
MITCHAM
SURREY, CR4 4SR.

N-P-N SILICON PLANAR U.H.F. TRANSISTOR

BLX93

TENTATIVE DATA

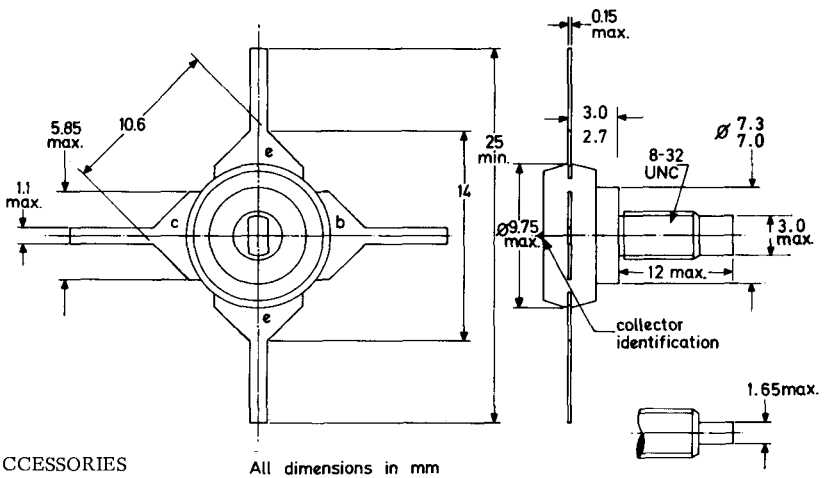
Silicon n-p-n transistor designed for u.h.f. operation in class A, B or C with frequencies up to 1GHz. The device is mounted in a plastic, capstan, strip-line encapsulation.

With a supply voltage of 28V and a signal frequency of 470MHz, the BLX93 will produce 7.0W output into a 50Ω load.

QUICK REFERENCE DATA

V_{CC} (V)	f (MHz)	P_{DR} (W)	P_L into 50Ω (W)	η (%)	T_h (°C)	Circuit
24	470	1.0	7.0 typ.	70 typ.	25	Un-neutralised common-emitter class B
28	470	1.0	7.0 min.	60 min.	25	
28	470	1.0	8.0 typ.	75 typ.	25	
28	1000	1.5	5.0 typ.	45 typ.	25	

OUTLINE AND DIMENSIONS



All dimensions in mm

D3370

ACCESSORIES

Nut and lock-washer supplied with device

Torque on nut: min. 0.75Nm (7.5kg cm)
max. 0.85Nm (8.5kg cm)

RATINGS

Limiting values of operation according to the absolute maximum system.

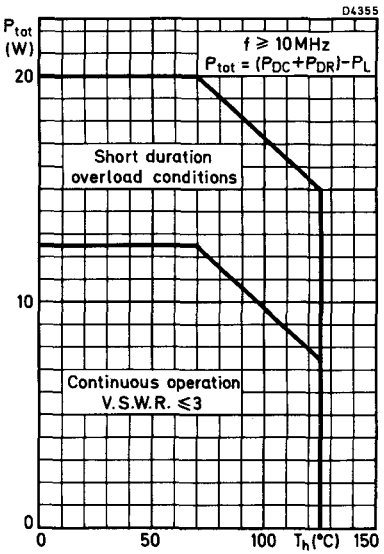
Electrical

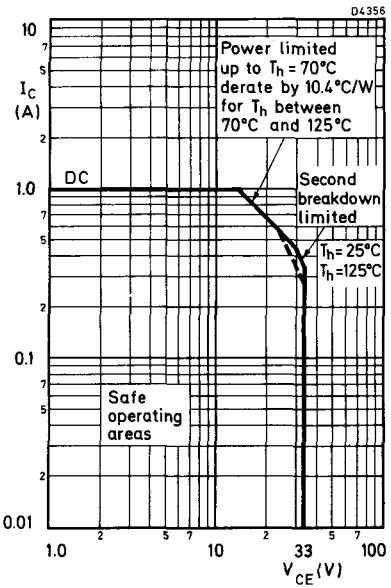
V_{CBOM} max.		65	V
V_{CESM} max.	(R_{BE} = 0)	65	V
V_{CEO} max.		33	V
V_{EBO} max.		4.0	V
I_C max.		1.0	A
I_{CM} max.	(f ≥ 10MHz)	3.0	A
P_{tot} max.	(f ≥ 10MHz, $T_h \leq 70^oC$)	12.5	W

See also graphs below

Temperature

T_{stg}	-65 to +150	^oC





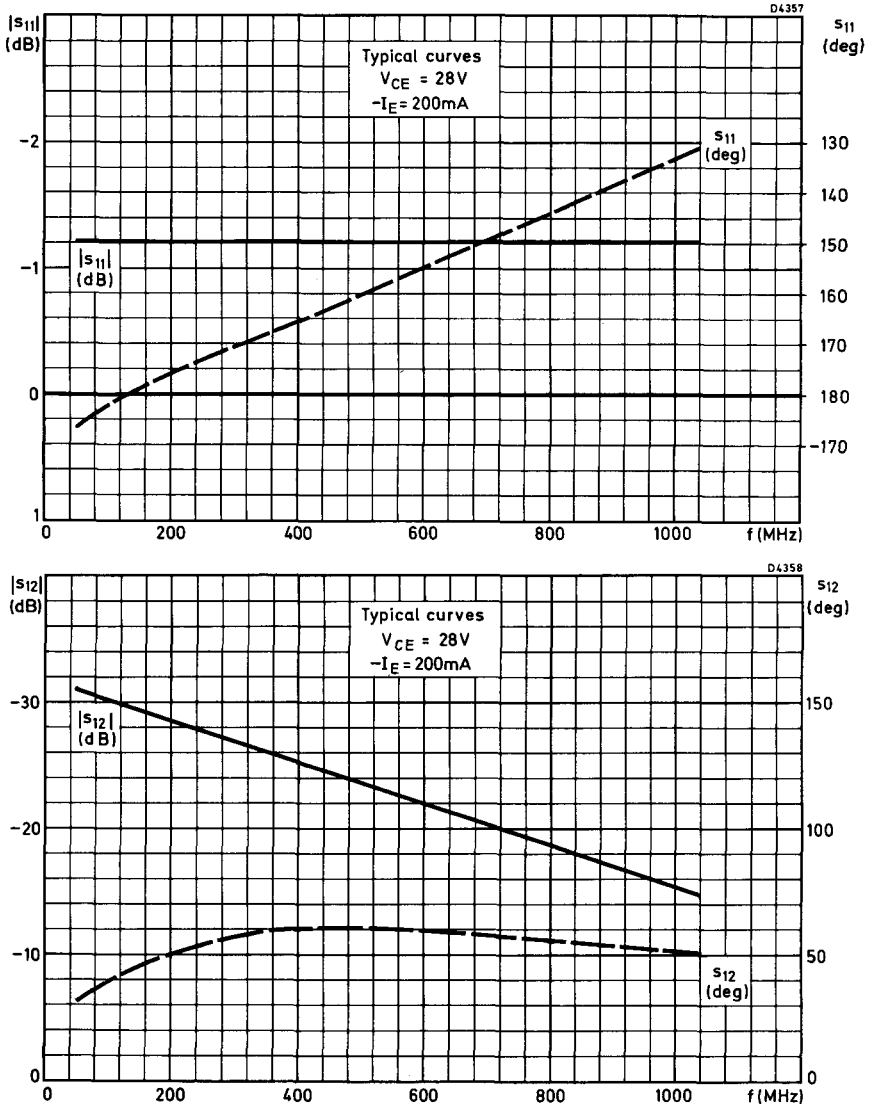
N-P-N SILICON PLANAR U.H.F. TRANSISTOR

BLX93

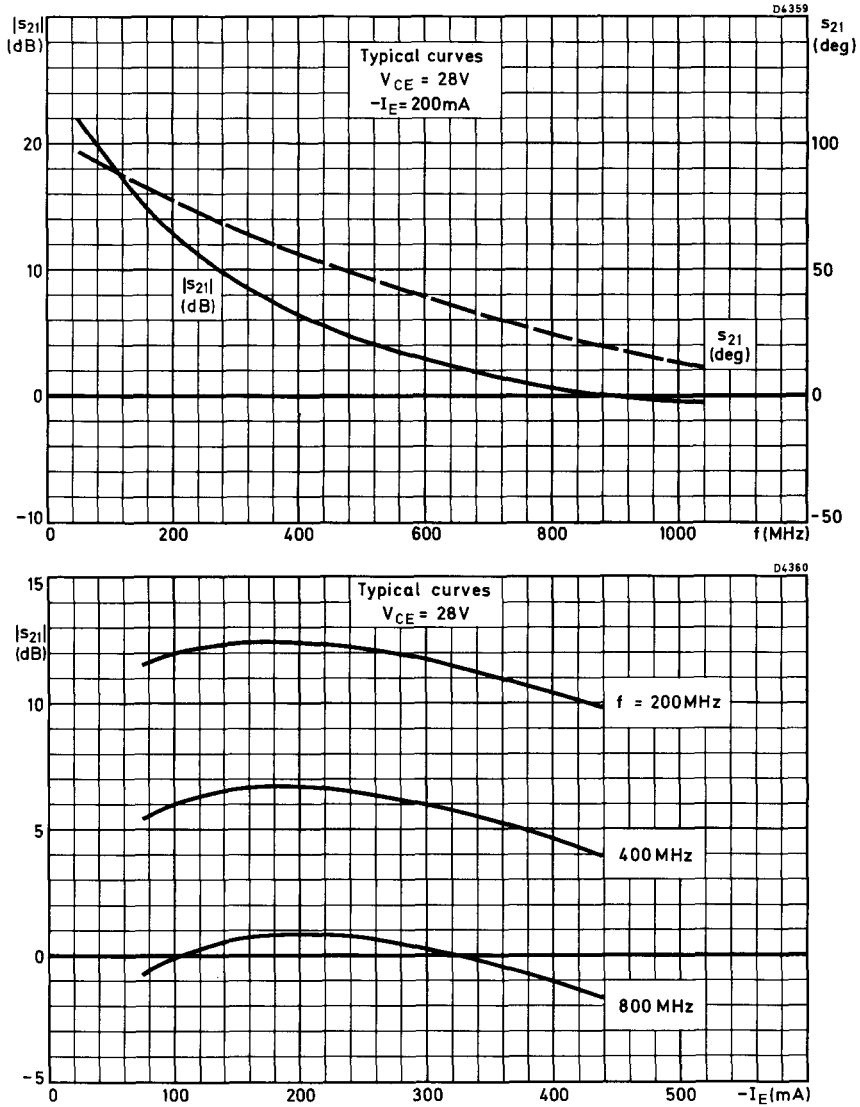
ELECTRICAL CHARACTERISTICS (T_j = 25°C unless otherwise stated)

		Min.	Typ.	Max.	
$V_{(BR)CBO}$	Collector-base breakdown voltage I_C = 10mA	65	-	-	V
$V_{(BR)CES}$	Collector-emitter breakdown voltage I_C = 10mA, R_{BE} = 0	65	-	-	V
$V_{(BR)CEO}$	Collector-emitter breakdown voltage I_C = 25mA	33	-	-	V
$V_{(BR)EBO}$	Emitter-base breakdown voltage I_E = 1.0mA	4.0	-	-	V
h_{FE}	Static forward current transfer ratio I_C = 100mA, V_{CE} = 5.0V	10	35	-	
*f_T	Transition frequency I_C = 200mA, V_{CE} = 5.0V, f = 500MHz	-	1200	-	MHz
C_{Tc}	Collector capacitance V_{CB} = 10V, $I_E = I_e$ = 0, f = 1.0MHz	-	14	-	pF
C_{Te}	Emitter capacitance V_{EB} = 0, $I_C = I_c$ = 0, f = 1.0MHz	-	60	-	pF
C_{cs}	Collector-stud capacitance	-	2.0	-	pF

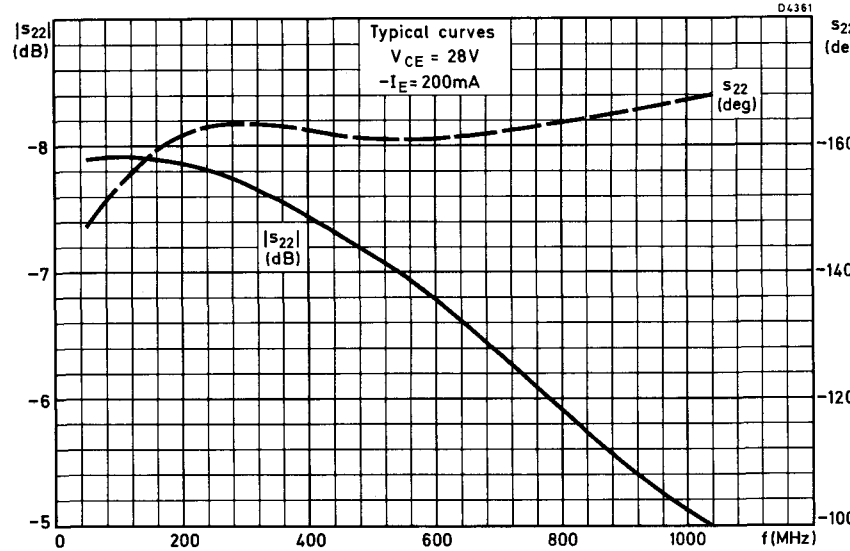
*Derived from the 's' parameters measured at f = 500MHz, T_{amb} = 25°C



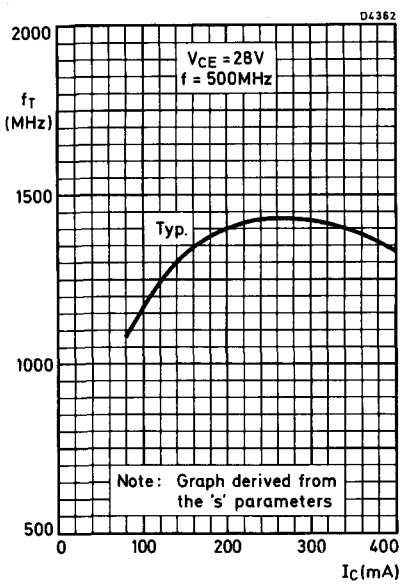
TYPICAL VARIATION OF INPUT REFLECTION COEFFICIENT AND FEEDBACK COEFFICIENT WITH FREQUENCY

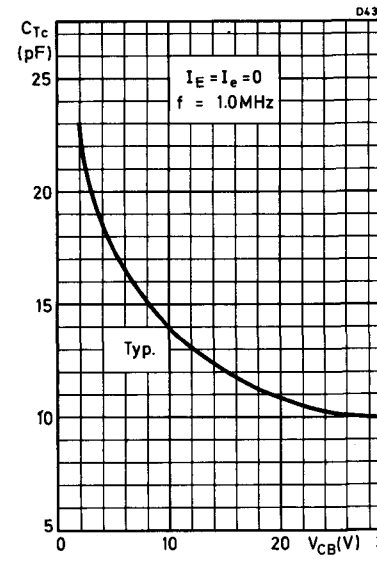


TYPICAL VARIATION OF FORWARD TRANSFER COEFFICIENT WITH FREQUENCY AND EMITTER CURRENT



TYPICAL VARIATION OF OUTPUT REFLECTION COEFFICIENT WITH FREQUENCY





APPLICATION INFORMATION

R.F. Performance in c.w. operation ($T_h = 25^oC$)

V_{CC} (V)	f (MHz)	P_{DR} (W)	P_L into 50Ω (W)	η (%)	$\bar{z}_i$ (Ω)	$\bar{Y}_L$ (mmho)
24	470	1.0	7.0 typ.	70 typ.	-	-
28	470	1.0	7.0 min.	60 min.	-	-
28	470	1.0	8.0 typ.	75 typ.	1.6 +j5.5	20-j40
28	1000	1.5	5.0 typ.	45 typ.	-	-

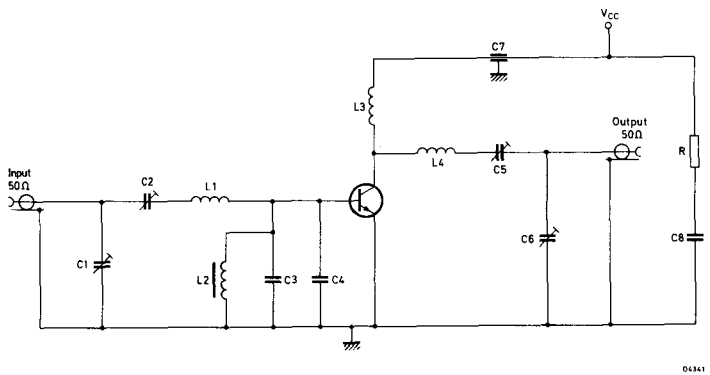
At $P_L = 7.0W$ and $V_{CC} = 28V$, the output power at heatsink temperatures between 25 and 90°C relative to that at 25°C is diminished typically by 10mW/°C.

The transistor is designed to withstand full load mismatch in the test circuit under the following conditions: -

$V_{CC} = 28V$ f = 470MHz $T_h = 90^oC$

$P_L = 7.0W$ V.S.W.R. = 50:1 at any phase

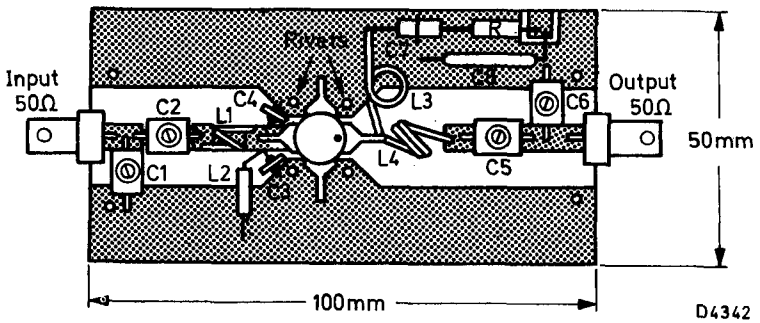
470MHz amplifier circuit



APPLICATION INFORMATION (contd.)

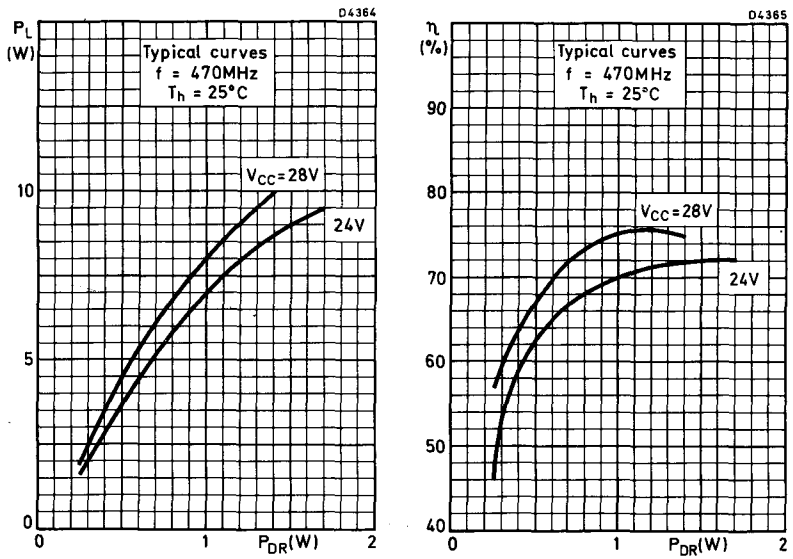
Component values for 470MHz amplifier circuit.
C1 = C2 = 1.8 to 18pF film-dielectric trimmer capacitors.
C3 = C4 = 18pF disc ceramic capacitors.
C5 = C6 = 1.0 to 9.0pF film-dielectric trimmer capacitors.
C7 = 1000pF feed-through capacitor.
C8 = 0.1μF ceramic capacitor.
L1 = 1 turn of 1.2mm Cu wire, internal diameter 5mm, lead length = 2mm.
L2 = 0.47μH choke.
L3 = 3 turns of 0.5mm Cu wire, internal diameter 4mm, lead length = 5mm
L4 = 2 turns of 1.2mm Cu wire, internal diameter 6.5mm, lead length = 4mm

Component layout on 1.5mm double copper clad fibre glass board



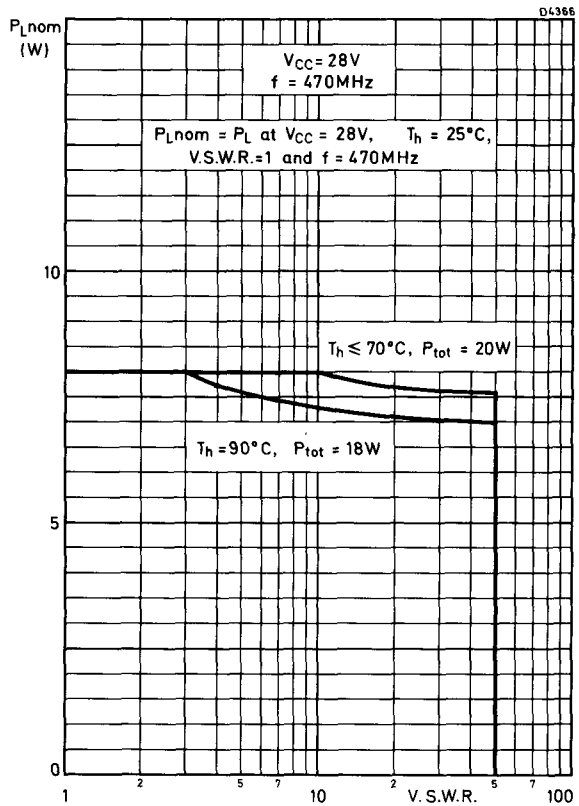
Shaded area copper

Underside area completely copper clad



TYPICAL VARIATION OF LOAD POWER AND EFFICIENCY WITH DRIVE POWER

APPLICATION INFORMATION (contd.)



INDICATED LOAD POWER AS A FUNCTION OF OVERLOAD

The above graph has been derived from an evaluation of the performance of transistors matched up to 8 watts load power in the test amplifier on Page 7 and subsequently subjected to various mismatch conditions at 28V with V.S.W.R. up to 50: 1 and elevated heatsink temperatures. This indicates a restriction to the load power matched under nominal conditions in the recommended test configuration.

CAUTION

This device incorporates Beryllium Oxide, the dust of which is toxic. The device is entirely safe provided that it is not dismantled.

Care should be taken to ensure that all those who may handle, use or dispose of this device are aware of its nature and of the necessary safety precautions. In particular, it should never be thrown out with general industrial or domestic waste.

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MITCHAM
SURREY, CR4 4SR.

N-P-N SILICON PLANAR EPITAXIAL U.H.F. TRANSISTOR

BLX94

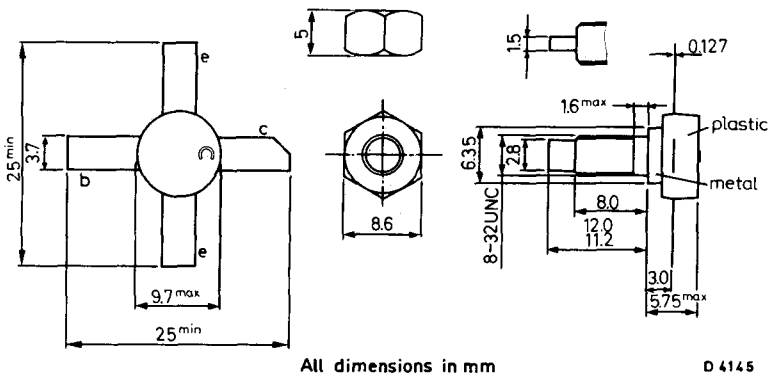
N-P-N silicon planar epitaxial transistor intended for transmitting applications in class A, B or C with a supply voltage up to 28V.
The transistor is resistance stabilised and is tested under severe load mismatch conditions.
It has a 1/4" capstan envelope with a moulded cap. All leads are isolated from the stud.

QUICK REFERENCE DATA

R. F. performance at $T_{mb} \leq 25^{o}C$ in an un-neutralised common-emitter class B circuit.

Mode of operation	V_{CC} (V)	f (MHz)	P_{DR} (W)	P_L (W)	I_C (A)	G_p (dB)	η (%)	$\overline{z_i}$ (Ω)	$\overline{Y_L}$ (mA/V)
C.W.	28	470	<5	20	<1.3	>6	>55	0.65+j3.9	62-j97

OUTLINE AND DIMENSIONS



All dimensions in mm D 4145

Torque on nut: 7.5kg cm (0.75Nm) min.
8.5kg cm (0.85Nm) max.

Diameter of clearance hole in heatsink: 4.17mm max.

Note: Do not chamfer the edges of the mounting holes when removing burrs. When locking is required, an adhesive instead of a lock washer is preferred.

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

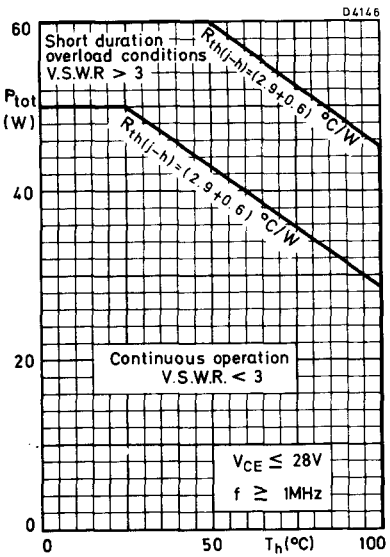
V_{CBOM} max.	65	V
V_{CEO} max.	33	V
V_{EBO} max.	4.0	V
$I_{C(AV)}$ max.	2.0	A
I_{CM} max. (f > 1.0MHz)	6.0	A
P_{tot} max. ($T_h \leq 25^oC$, f > 1.0MHz)	50	W

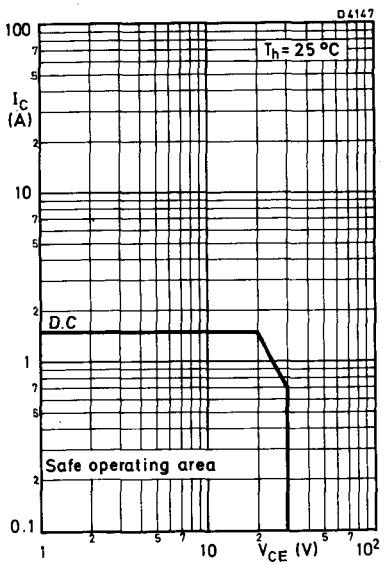
Temperature

T_{stg}	-30 to +200	^oC
T_j max.	200	^oC

THERMAL CHARACTERISTICS

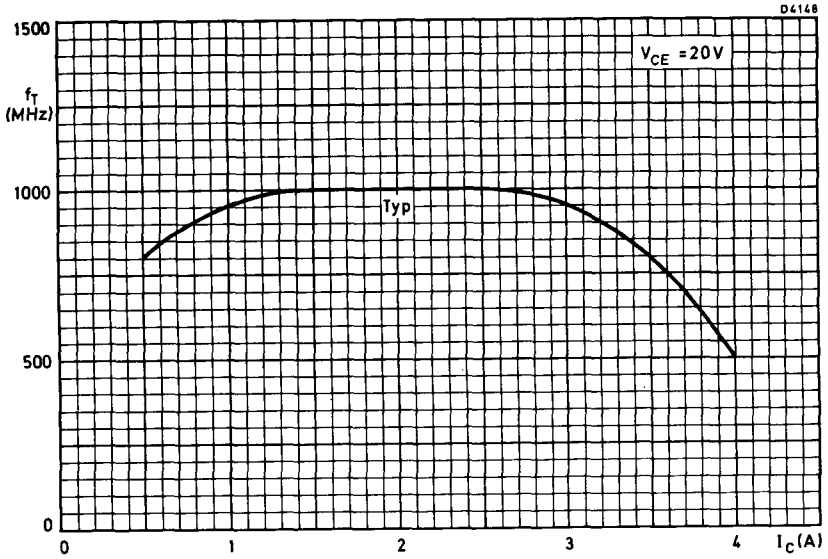
$R_{th(j-mb)}$	2.9	$^oC/W$
$R_{th(mb-h)}$	0.6	$^oC/W$

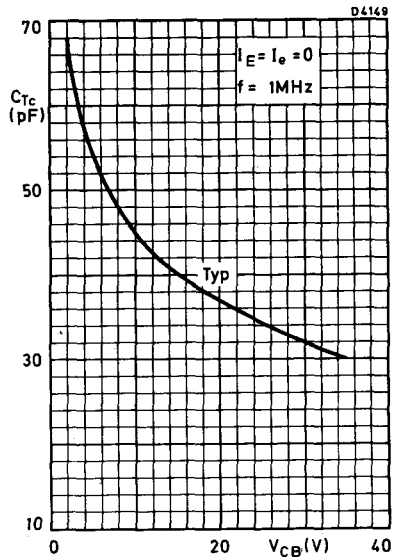




ELECTRICAL CHARACTERISTICS ($T_j = 25^oC$ unless otherwise stated)

		Min.	Typ.	Max.	
I_{CEO}	Collector cut-off current $I_B = 0$, $V_{CE} = 28V$	-	-	10	mA
$V_{(BR)CBO}$	Collector-base breakdown voltage open emitter $I_C = 25mA$	65	-	-	V
$V_{(BR)CEO}$	Collector-emitter breakdown voltage, open base $I_C = 25mA$	33	-	-	V
$V_{(BR)EBO}$	Emitter-base breakdown voltage open collector $I_E = 10mA$	4.0	-	-	V
E	Transient energy $L = 25mH$, $f = 50Hz$				
	open base	3.0	-	-	mWs
	$-V_{BE} = 1.5V$, $R_{BE} = 33\Omega$	3.0	-	-	mWs
h_{FE}	Static forward current transfer ratio				
	$I_C = 1.0A$, $V_{CE} = 5.0V$	15	50	-	
f_T	Transition frequency $I_C = 2.0A$, $V_{CE} = 20V$	-	1.0	-	GHz
C_{Tc}	Collector capacitance $I_E = I_e = 0$, $V_{CB} = 30V$, $f = 1.0MHz$	-	32	50	pF
$-C_{re}$	Feedback capacitance $I_C = 100mA$, $V_{CE} = 30V$, $f = 1.0MHz$	-	18	-	pF
C_{cs}	Collector-stud capacitance	-	2.0	-	pF


D4148
1500
f_T (MHz)
1000
500
0
V_{CE} = 20V
Typ
0
1
2
3
4
I_C(A)


D4149
70
C_{Tc} (pF)
50
30
10
$I_E = I_e = 0$
f = 1MHz
Typ
0
20
V_{CB}(V)
40

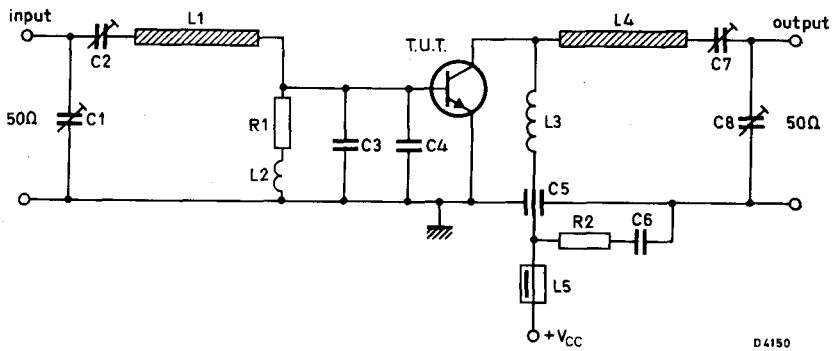
APPLICATION INFORMATION

R. F. performance in c. w. operation (un-neutralised common-emitter class B circuit)

f = 470MHz, T_{mb} = 25°C

V_{CC} (V)	P_{DR} (W)	P_L (W)	I_C (A)	G_p (dB)	η (%)	$\overline{z_i}$ (Ω)	Y_L (mA/V)
28	<5	20	<1.3	>6	>55	0.65+j3.9	62-j97

Test circuit



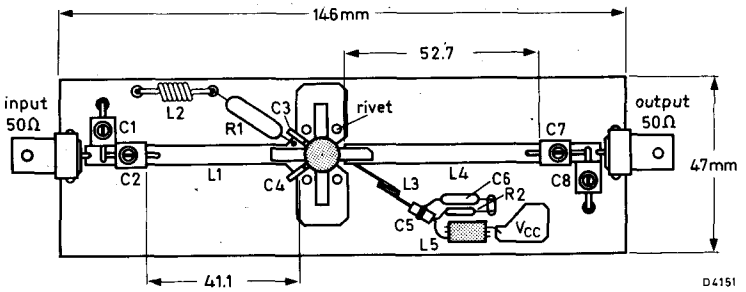
Component values

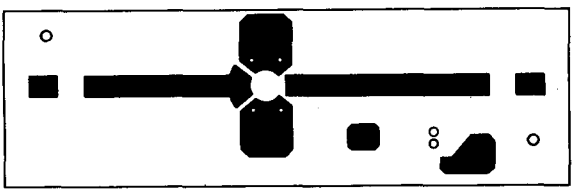
C1 = C2 = C8 = 2 to 9pF film dielectric trimmer
C3 = C4 = 15pF chip capacitor
C5 = 100pF feed-through capacitor
C6 = 33nF polyester capacitor
C7 = 2 to 18pF film dielectric trimmer
R1 = 1Ω carbon resistor
R2 = 10Ω carbon resistor
L1 = strip line (40.8 × 5.0mm)
L2 = 13 turns of closely wound enamelled copper wire (0.5mm), int. dia. 4.0mm
L3 = 2 turns of copper wire (1mm), winding pitch 1.5mm, int. dia. 4.0mm, leads 2 × 5mm
L4 = strip line (52.4 × 5.0mm)
L5 = ferroxcube choke coil. Z (at f = 50MHz) = 750Ω ±20%

L1 and L4 are strip lines on a double copper clad print plate with teflon fibre-glass dielectric (ϵ_r = 2.74), thickness 1.45mm.

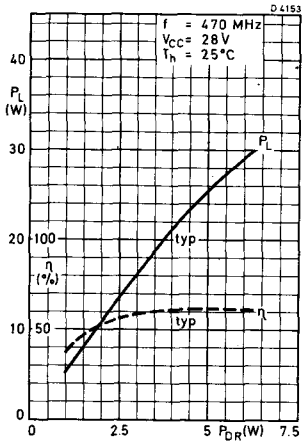
APPLICATION INFORMATION (contd.)

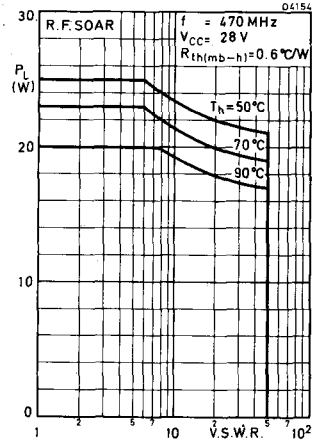
Component layout and printed circuit board for 470MHz test circuit.





The circuit and the components are situated on one side of the teflon fibre-glass board, the other side being fully metallised to serve as earth. Earth connections are made by means of hollow rivets.





For high voltage operation, a stabilised power supply is generally used.
The graph shows the allowable output power under nominal conditions as a function of the V.S.W.R., with heat-sink temperature as parameter.

CAUTION

This device incorporates Beryllium Oxide, the dust of which is toxic. The device is entirely safe provided that it is not dismantled.

Care should be taken to ensure that all those who may handle, use or dispose of this device are aware of its nature and of the necessary safety precautions. In particular, it should never be thrown out with general industrial or domestic waste.

DISPOSAL SERVICE

Devices requiring disposal may be returned to the Mullard Service Department. They must be separately and securely packed and clearly identified. If any are damaged or broken they MUST NOT be sent through the post. In this case, advice is available from:

THE SERVICE DEPARTMENT
MULLARD LIMITED
P.O. BOX 142
NEW ROAD
MITCHAM
SURREY, CR4 4SR.

N-P-N SILICON V.H.F. POWER TRANSISTORS

BLY33 BLY34

TENTATIVE DATA

Silicon n-p-n high frequency medium power transistors primarily intended for class B operation in v.h.f. amplifiers. The collector is electrically connected to case.

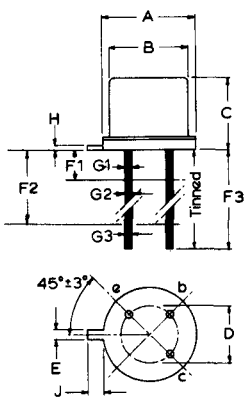
QUICK REFERENCE DATA

		BLY33	BLY34	
V_{CES} max. (peak r.f. ≥1.0MHz)		66	40	V
V_{CEO} max.		33	20	V
I_{CM} max. (peak r.f. ≥1.0MHz)		1.5	1.5	A
P_{tot} max. ($T_{case} \leq 100^{o}C$)		2.0	2.0	W
T_j max.		150	150	^{o}C
f_T min. (I_C=0.2A, V_{CE}=5.0V, f=100MHz)		250	250	MHz
Performance in a 175MHz common emitter amplifier:-				
	Operation:	a.m.	f.m.	
V_{CC}	Supply voltage	13.8	13.8	V
P_o	Output power	2.0	3.0	W
G_p	Typ. power gain	8.0	8.0	dB
η	Typ. efficiency	80	80	%

Unless otherwise stated data is applicable to both types

OUTLINE AND DIMENSIONS

Conforms to B.S. 3934 SO-3/SB3-3B
J.E.D.E.C. TO-39



	Millimetres		
	Min.	Nom.	Max.
A	9.10	-	9.40
B	8.2	-	8.5
C	6.15	-	6.60
D	-	5.08	-
E	0.71	-	0.86
F1	-	-	0.51
F2	12.7	-	-
F3	12.7	-	15
G1	-	-	1.01
G2	0.41	-	0.48
G3	-	-	0.53
H	-	0.4	-
J	0.74	-	1.01

Collector connected to case

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{CES} max. (peak r.f. ≥1.0MHz)	BLY33	66	V
	BLY34	40	V
V_{CEO} max.	BLY33	33	V
	BLY34	20	V
V_{EBO} max.		4.0	V
I_C max.		0.5	A
I_{CM} max. (f≥1.0MHz)		1.5	A
I_{CM} max. (f<1.0MHz)		0.5	A
P_{tot} max. $T_{case}=25^oC$, f≥1.0MHz		5.0	W
$T_{case}=25^oC$, f<1.0MHz		4.0	W

See also curves on pages 5 and 6

Temperature

T_j max.	Continuous operation	150	^oC
	Intermittent operation, total duration 200 hours	200	^oC
T_{stg} min.		-65	^oC
T_{stg} max.		150	^oC

THERMAL CHARACTERISTIC

$R_{th(j-case)}$	25	degC/W

ELECTRICAL CHARACTERISTICS ($T_j=25^oC$ unless otherwise stated)

		Min.	Typ.	Max.	
I_{CES}	Collector-emitter cut-off current				
	$V_{CE}=V_{CES}$ max., $V_{BE}=0$	-	0.10	5.0	mA
	$V_{CE}=V_{CEO}$ max., $V_{BE}=0$	-	0.02	0.5	mA
I_{EBO}	Emitter cut-off current $V_{EB}=4.0V$, $I_C=0$	-	0.2μ	0.5m	A
h_{FE}	Static forward current transfer ratio				
	$I_C=0.2A$, $V_{CE}=5.0V$	10	60	-	

ELECTRICAL CHARACTERISTICS (cont'd)

		Min.	Typ.	Max.	
f_T	Transition frequency I_C=0.2A, V_{CE}=5.0V, f=100MHz, T_{amb}=25°C	250	450	-	MHz
C_{tc}	Collector capacitance V_{CB}=10V, I_E=I_e=0, f=0.5MHz	-	11	15	pF
C_{te}	Emitter capacitance V_{EB}=0, I_C=I_c=0, f=0.5MHz	45	65	90	pF

RECOMMENDED OPERATING CONDITIONS

As a medium power amplifier for the output stage of a small transmitter, or as a driver for larger output stages.

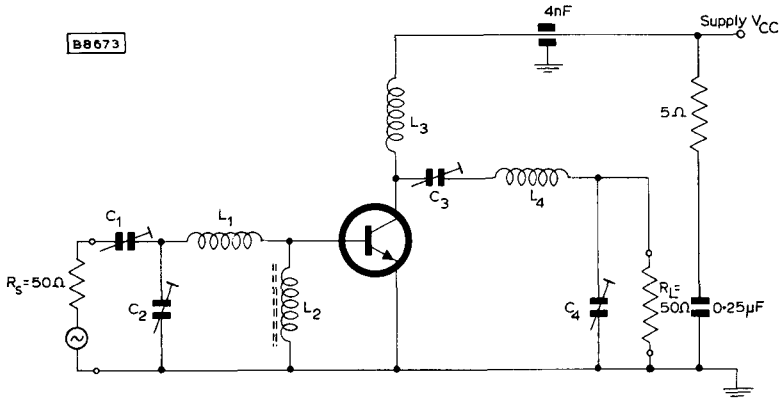
f = 175MHz

			BLY33		BLY34	
		Operation	a.m.	f.m.	f.m.	
V_{CC}	Supply voltage	nom.	13.8	28	13.8	V
		max.	16.5	32	16.5	V
V_B	Base bias voltage		0	0	0	V
P_o	Output power		2.0	3.0	3.0	W
P_i	Input power	typ.	0.32	0.28	0.5	W
		max.	0.40	0.40	0.6	W
I_{CC}	Supply current	typ.	180	160	270	mA
η	Efficiency	typ.	80	65	80	%

NOTES

1. For a.m. telephony, collector modulation of the output and driver stages is recommended.
2. A heatsink of thermal resistance 20degC/W is recommended for operation in ambient temperatures up to 65°C. At temperatures >65°C, derating is necessary.
3. Under the recommended a.m. operating condition and without modulation, the transistor can withstand any load mismatch. With modulation applied, operation into an extreme mismatch may adversely affect the life of the transistor and care should be exercised to keep the device within its ratings.

BASIC V.H.F. AMPLIFIER CIRCUIT

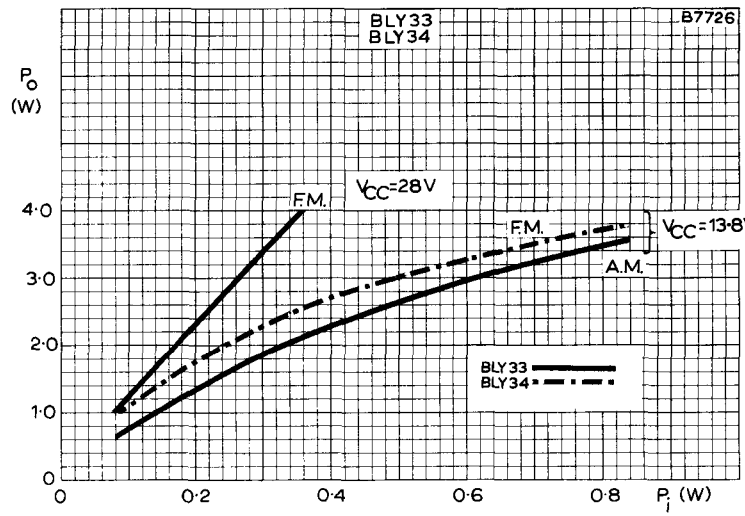


Component values for 175MHz amplifier circuit

C_1	30	pF
C_2	30	pF
C_3	30	pF
C_4	30	pF
L_1	1.0	inch of straight 18 s.w.g.
L_2	3.0	turns of 24 s.w.g. on Ferrite FX1115
L_3	5.0	turns of 18 s.w.g., d=3/8", l=3/8".
L_4	3.0	turns of 18 s.w.g., d=3/8", l=3/8".

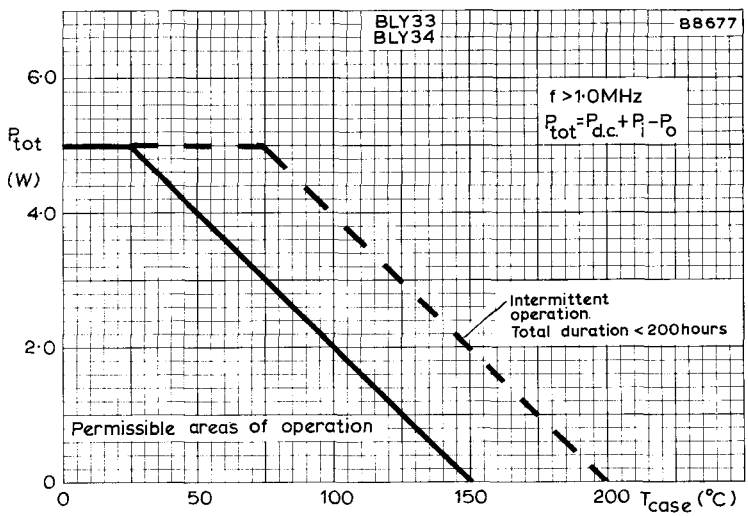
NOTE

To obtain optimum gain performance the emitter lead length should not exceed 1.6mm.

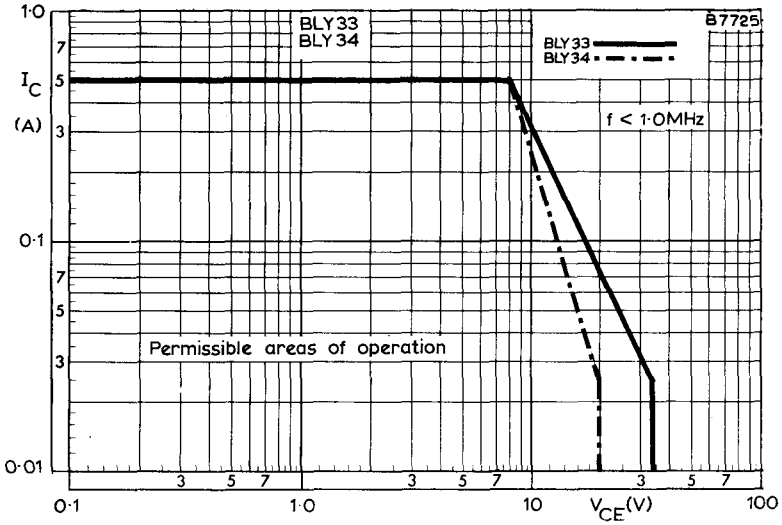


TYPICAL VARIATION OF OUTPUT POWER WITH INPUT POWER FOR V.H.F. AMPLIFIER

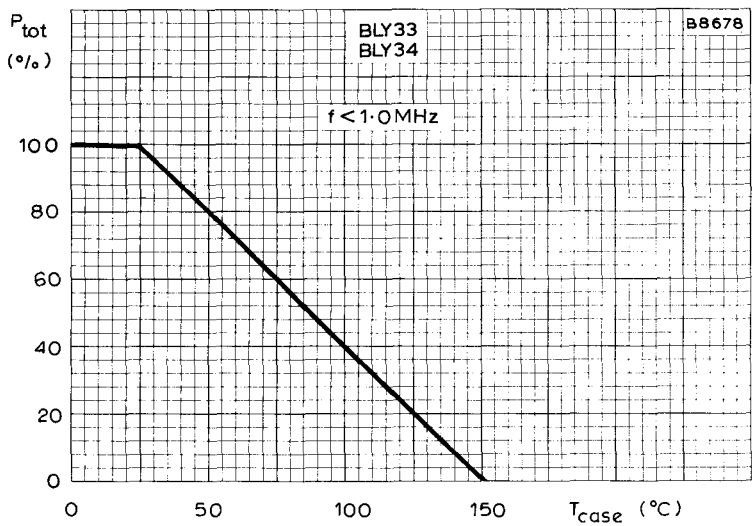
(See Recommended Operating Conditions on page 3)



MAXIMUM PERMISSIBLE POWER DISSIPATION PLOTTED AGAINST CASE TEMPERATURE FOR FREQUENCIES >1.0MHz



PERMISSIBLE AREAS OF OPERATION FOR FREQUENCIES < 1.0MHz



PERCENTAGE POWER DERATING PLOTTED AGAINST CASE TEMPERATURE FOR FREQUENCIES < 1.0MHz

N-P-N SILICON PLANAR V.H.F. TRANSISTORS

BLY35 BLY83

Silicon n-p-n transistors for v.h.f. mobile operation in class B. The BLY35 is mounted in a TO-60 envelope and the BLY83 is mounted in a plastic, capstan strip-line encapsulation.

The transistors are primarily intended for a.m. operation at 13.8V but are also suitable for f.m. operation at 24V.

QUICK REFERENCE DATA

Mode	V_{CC} (V)	f (MHz)	P_{DR} (W)	P_L (carrier) (W)	P_L into 50Ω (W)	η (%)	m (%)	d_{tot} (%)
a.m.	13.8	175	0.35	7.0 typ.	-	77 typ.	80	<5
a.m.	13.8	80	0.06	7.5 typ.	-	77 typ.	80	<5
c.w.	24	175	1.35	-	13 typ.	65 typ.	-	-

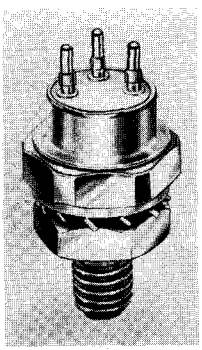
Unless otherwise stated data are applicable to both types

OUTLINE AND DIMENSIONS

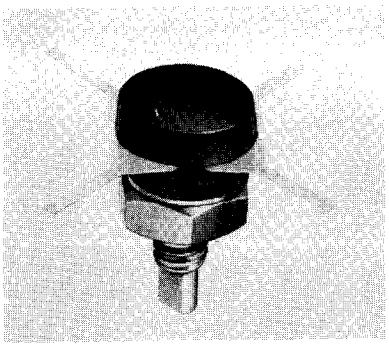
BLY35 J.E.D.E.C. TO-60 (Emitter connected to stud)

BLY83 Capstan strip-line (Stud isolated)

For details see page 2



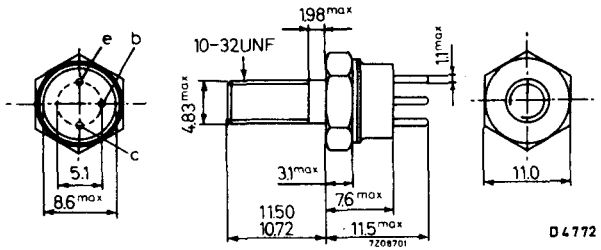
BLY35



BLY83

OUTLINE DRAWINGS (All dimensions in mm)

BLY35

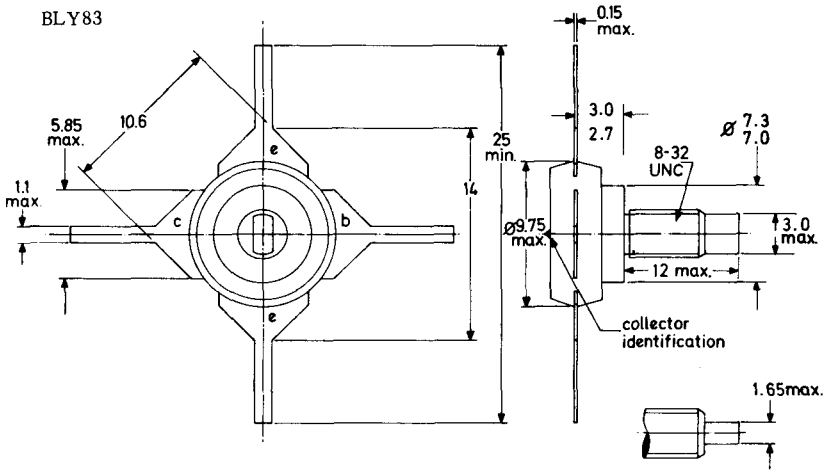


Accessories

Nut and lock-washer supplied with device

Torque on nut: min. 0.8Nm (8kg cm)
max. 1.7Nm (17kg cm)

BLY83



All dimensions in mm

D3370

Accessories

Nut and lock-washer supplied with device

Torque on nut: min. 0.75Nm (7.5kg cm)
max. 0.85Nm (8.5kg cm)

RATINGS

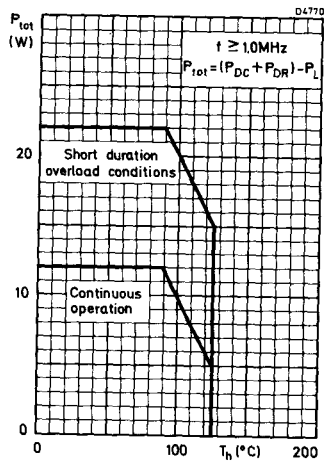
Limiting values of operation according to the absolute maximum system.

Electrical

V_{CBOM} max.		66	V
V_{CESM} max.		66	V
V_{CEO} max.		33	V
V_{EBO} max.		4.0	V
I_C max.		2.5	A
I_{CM} max. (f <1.0MHz)		2.5	A
I_{CM} max. (f ≥1.0MHz)		7.5	A
P_{tot} max. (f ≥1.0MHz, $T_h \leq 90^oC$)		12	W

Temperature

T_{stg}	BLY35	-65 to +200	^oC
	BLY83	-65 to +150	^oC



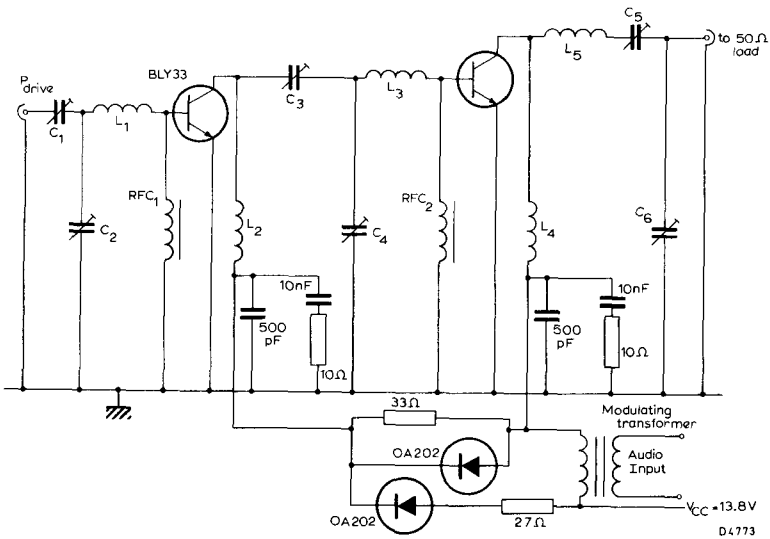
ELECTRICAL CHARACTERISTICS (T_j = 25°C unless otherwise stated)

		Min.	Typ.	Max.	
$V_{(BR)CBO}$	Collector-base breakdown voltage I_C = 10mA	66	-	-	V
$V_{(BR)CES}$	Collector-emitter breakdown voltage I_C = 10mA, R_{BE} = 0	66	-	-	V
$V_{(BR)CEO}$	Collector-emitter breakdown voltage I_C = 50mA	33	-	-	V
$V_{(BR)EBO}$	Emitter-base breakdown voltage I_E = 1.0mA	4.0	-	-	V
h_{FE}	Static forward current transfer ratio I_C = 1.0A, V_{CE} = 5.0V	10	60	220	
f_T	Transition frequency I_C = 1.0A, V_{CE} = 5.0V f = 100MHz, T_{amb} = 25°C	250	450	-	MHz
C_{Tc}	Collector capacitance V_{CB} = 10V, $I_E = I_e$ = 0, f = 1.0MHz	-	34	45	pF
C_{Te}	Emitter capacitance V_{EB} = 0, $I_C = I_c$ = 0, f = 1.0MHz	100	155	-	pF

APPLICATIONS INFORMATION

R. F. performance in a 7.0W a.m. transmitter at f = 175MHz, f mod. = 1kHz

V_{CC} (V)	P_{DR} (W)	P_L (carrier) (W)	I_C (driver) (A)	I_C (amplifier) (A)	G_p (dB)	η (%)	m (%)	d_{tot} (%)
13.8	0.35	7.0 typ.	0.22 typ.	0.66 typ.	13	77 typ.	80	5 max.



Component values for 175MHz transmitter circuit: -

C_1 to C_6 = 4 to 29pF concentric trimmer capacitors

$L_1 = L_3$ = 3 turns of 1.2mm en.Cu wire, int.diam. = 6.4mm, length = 5.0mm

$L_2 = L_4$ = 5 turns of 1.2mm en.Cu wire, int.diam. = 6.4mm, length = 10mm

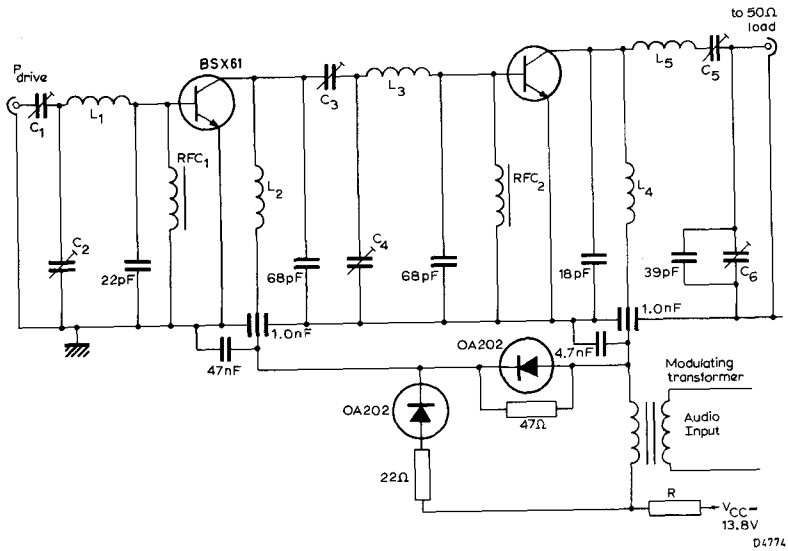
L_5 = 3 turns of 1.7mm en.Cu wire, int.diam. = 10mm, length = 10mm

$RFC_1 = RFC_2$ = 2 turns of 0.4mm en.Cu wire on Ferrite FX1115.

APPLICATIONS INFORMATION (contd.)

R.F. performance in a 7.0W a.m. transmitter at f = 80MHz,
f mod. = 1kHz

V_{CC} (V)	P_{DR} (W)	P_L (carrier) (W)	I_C (driver) (A)	I_C (amplifier) (A)	G_p (dB)	η (%)	m (%)	d_{tot} (%)
13.8	0.06	7.5 typ.	0.06 typ.	0.7 typ.	21	70 typ.	80	5 max.



Component values for 80MHz transmitter circuit: -

C_1 to C_6 = 4 to 29pF concentric trimmer capacitors

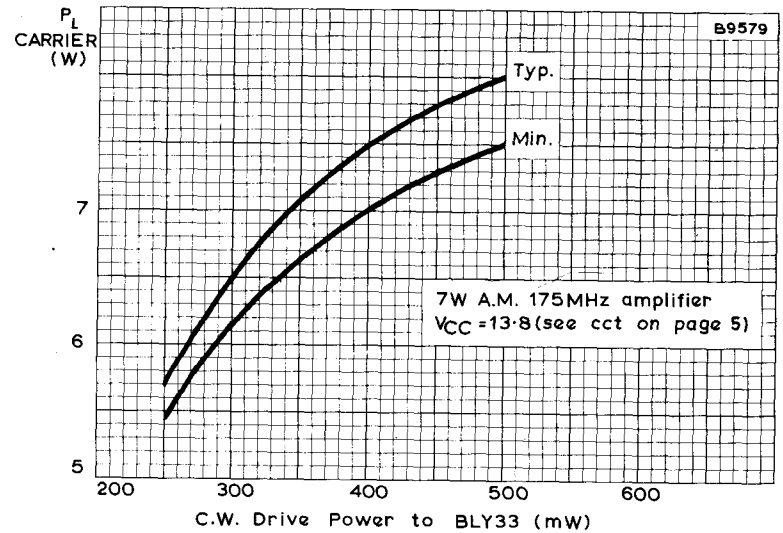
$L_1 = L_4$ = 5 turns of 1.2mm en.Cu wire, int.diam. = 6.3mm, length = 9.0mm

$L_3 = L_6$ = 3 turns of 1.2mm en.Cu wire, int.diam. = 7.0mm, length = 6.0mm

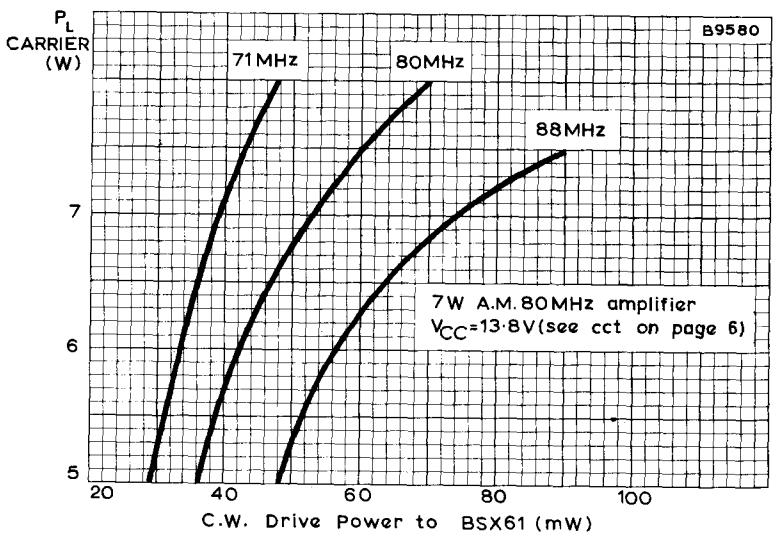
L_7 = 6 turns of 2.0mm en.Cu wire, int.diam. = 10mm, length = 13mm

$L_2 = L_5$ = 1 turn of 0.4mm en.Cu wire on Ferrite FX1115

R This resistor is incorporated to reduce the carrier level to 8W or below.



AERIAL CARRIER POWER PLOTTED AGAINST C.W. DRIVE POWER FOR THE 7W A.M. 175MHz AMPLIFIER (see page 5)

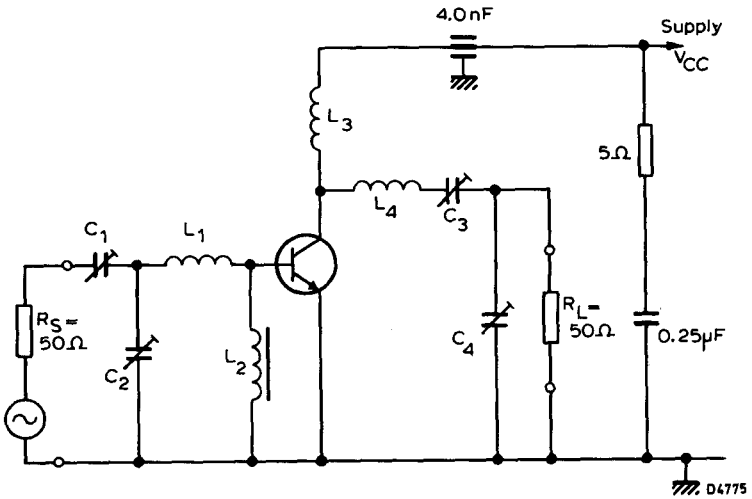


AERIAL CARRIER POWER PLOTTED AGAINST C.W. DRIVE POWER FOR THE 7W A.M. 80MHz AMPLIFIER (see page 6)

APPLICATIONS INFORMATION (contd.)

R.F. performance in c.w. operation at f = 175MHz, $T_h \leq 40^{\circ}C$

V_{CC} (V)	P_{DR} (W)	P_L into 50Ω (W)	η (%)	G_p (dB)
24	1.35	13 typ.	65 typ.	9.8
13.8	1.35	7.5 typ.	-	-



Component values for 175MHz amplifier circuit: -

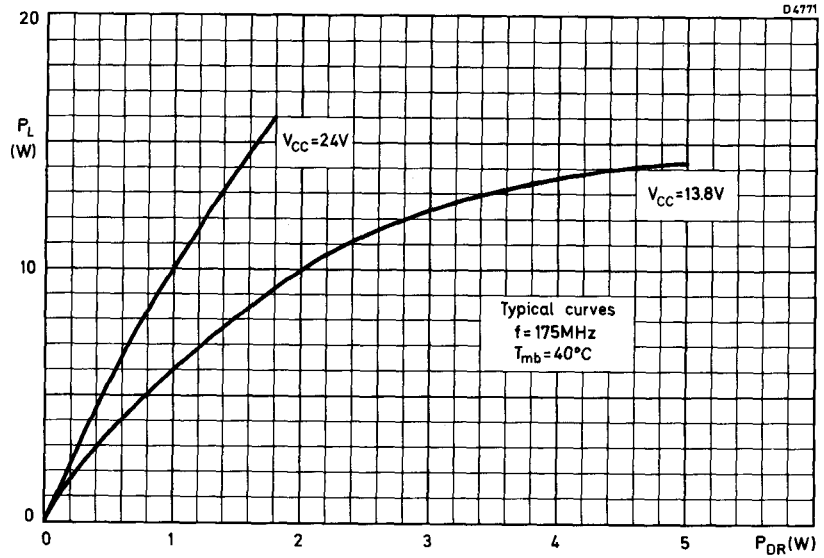
$C_1 = C_3 = C_4$ = 30pF max.
C_2 = 60pF max.
} concentric trimmer capacitors

L_1 = 25.4mm of straight 1.7mm Cu wire

L_2 = 3 turns of 0.5mm Cu wire on Ferrite FX1115

L_3 = 3 turns of 1.7mm Cu wire, int.diam. = 9.5mm, length = 9.5mm

L_4 = 2 turns of 2.0mm Cu wire, int.diam. = 12.7mm, length = 9.5mm

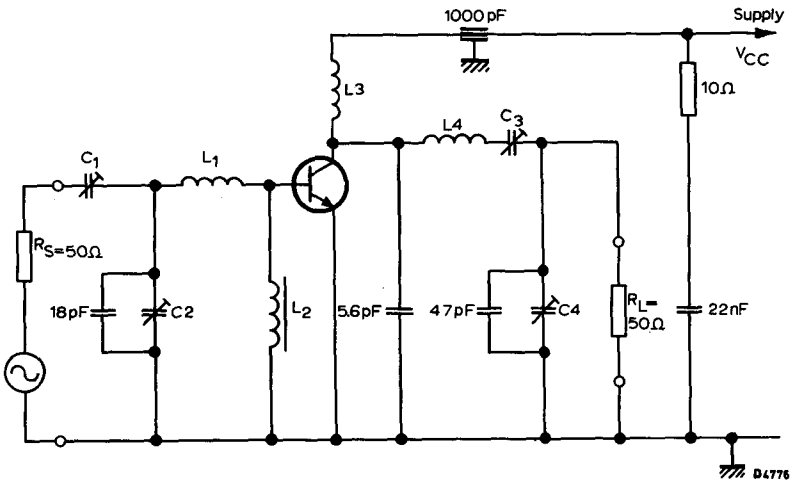


LOAD POWER PLOTTED AGAINST DRIVE POWER

APPLICATIONS INFORMATION (contd.)

R. F. performance in c.w. operation at f = 80MHz, $T_h \leq 40^{\circ}C$

V_{CC} (V)	P_{DR} (W)	P_L into 50Ω (W)
13.8	0.5	12.5 typ.
6.9	0.5	5.0 typ.



Component values for 80MHz amplifier circuit: -

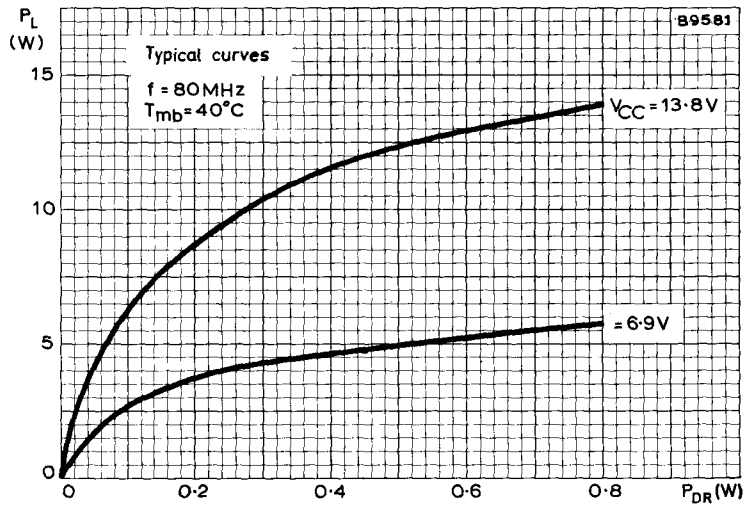
$C_1 = C_2 = C_3 = C_4$ = 4 to 29pF concentric trimmer capacitors

L_1 = 4 turns of 1.2mm Cu wire, int. diam. = 6.3mm, length = 8.0mm

L_2 = 2 turns of 0.35mm Cu wire, on Ferrite FX1115

L_3 = 5 turns of 1.2mm Cu wire, int. diam. = 6.3mm, CLOSE WOUND

L_4 = 5 turns of 1.7mm Cu wire, int. diam. = 9.6mm, length, = 12mm



LOAD POWER PLOTTED AGAINST DRIVE POWER

CAUTION

This device incorporates Beryllium Oxide, the dust of which is toxic. The device is entirely safe provided that it is not dismantled.

Care should be taken to ensure that all those who may handle, use or dispose of this device are aware of its nature and of the necessary safety precautions. In particular, it should never be thrown out with general industrial or domestic waste.

DISPOSAL SERVICE

Devices requiring disposal may be returned to the Mullard Service Department. They must be separately and securely packed and clearly identified. If any are damaged or broken they MUST NOT be sent through the post. In this case, advice is available from:

THE SERVICE DEPARTMENT
MULLARD LIMITED
P.O. BOX 142
NEW ROAD
MITCHAM
SURREY, CR4 4SR.

N-P-N SILICON PLANAR V.H.F. TRANSISTORS

BLY36 BLY84

Silicon n-p-n transistors for v.h.f. mobile operation in class B. The BLY36 is mounted in a TO-60 envelope and the BLY84 is mounted in a plastic, capstan strip-line encapsulation.

The transistors are primarily intended for f.m. operation at 13.8V.

QUICK REFERENCE DATA					
V_{CC} (V)	f (MHz)	P_{DR} (W)	P_L into 50Ω (W)	η (%)	Circuit
13.8	175	1.2	7.0 typ.	77 typ.	Un-neutralised
13.8	175	3.4	13.2 typ.	79 typ.	common-emitter
13.8	80	0.5	13.5 typ.	80 typ.	class B.

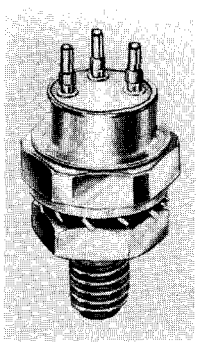
Unless otherwise stated data are applicable to both types

OUTLINE AND DIMENSIONS

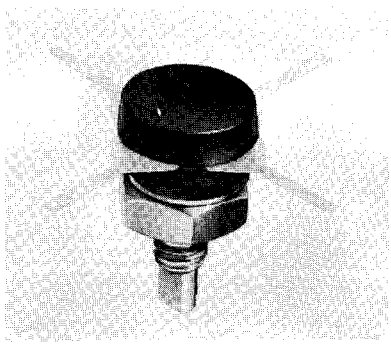
BLY36 J.E.D.E.C. TO-60 (Emitter connected to stud)

BLY84 Capstan strip-line (Stud isolated)

For details see page 2



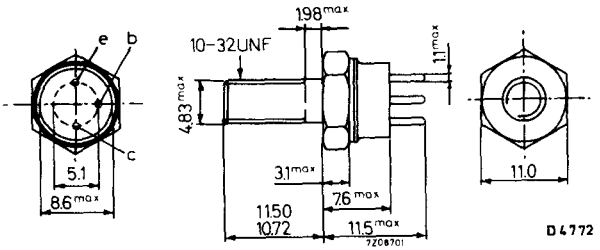
BLY36



BLY84

OUTLINE DRAWINGS (All dimensions in mm)

BLY36

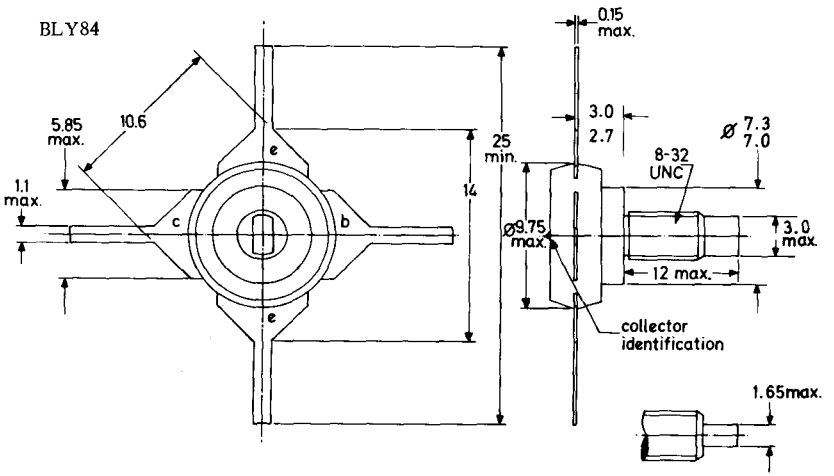


Accessories

Nut and lock-washer supplied with device

Torque on nut: min. 0.8Nm (8kg cm)
max. 1.7Nm (17kg cm)

BLY84



All dimensions in mm

Accessories

Nut and lock-washer supplied with device

Torque on nut: min. 0.75Nm (7.5kg cm)
max. 0.85Nm (8.5kg cm)

RATINGS

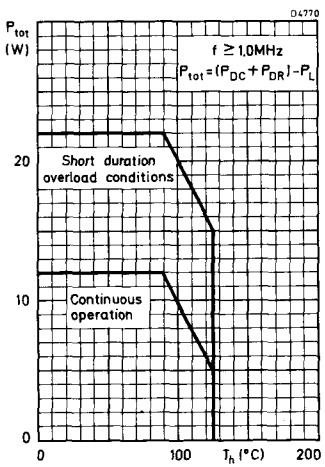
Limiting values of operation according to the absolute maximum system.

Electrical

V_{CBOM} max.	40	V
V_{CESM} max. (R_{BE} = 0)	40	V
V_{CEO} max.	20	V
V_{EBO} max.	4.0	V
I_C max.	2.5	A
I_{CM} max. (f <1.0MHz)	2.5	A
I_{CM} max. (f ≥1.0MHz)	7.5	A
P_{tot} max. (f ≥1.0MHz, $T_h \leq 90^oC$)	12	W

Temperature

T_{stg}	BLY36	-65 to +200	^oC
	BLY84	-65 to +150	^oC



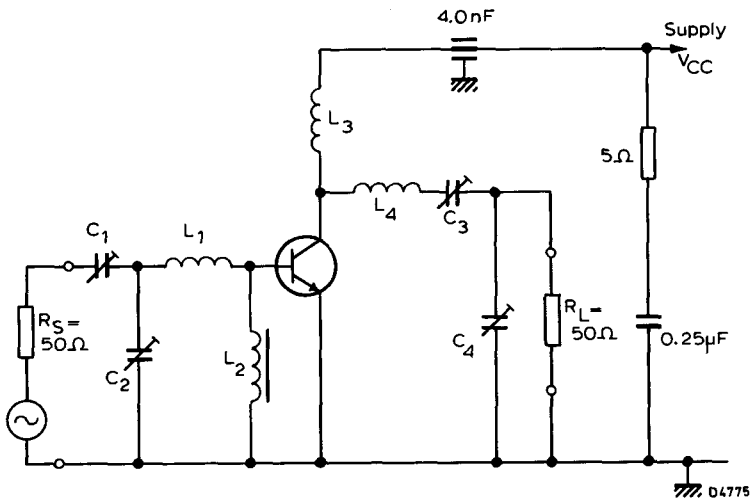
ELECTRICAL CHARACTERISTICS ($T_j = 25^oC$ unless otherwise stated)

		Min.	Typ.	Max.	
$V_{(BR)CBO}$	Collector-base breakdown voltage I_C = 10mA	40	-	-	V
$V_{(BR)CES}$	Collector-emitter breakdown voltage I_C = 10mA, R_{BE} = 0	40	-	-	V
$V_{(BR)CEO}$	Collector-emitter breakdown voltage I_C = 50mA	20	-	-	V
$V_{(BR)EBO}$	Emitter-base breakdown voltage I_E = 1.0mA	4.0	-	-	V
h_{FE}	Static forward current transfer ratio I_C = 1.0A, V_{CE} = 5.0V	10	60	-	
f_T	Transition frequency I_C = 1.0A, V_{CE} = 5.0V f = 100MHz, $T_{amb} = 25^oC$	250	450	-	MHz
C_{Tc}	Collector capacitance V_{CB} = 10V, $I_E = I_e$ = 0, f = 1.0MHz	-	37	45	pF
C_{Te}	Emitter capacitance V_{EB} = 0, $I_C = I_c$ = 0, f = 1.0MHz	100	155	-	pF

APPLICATIONS INFORMATION

R. F. *performance in c.w. operation at* f = 175MHz, $T_h \leq 40^{\circ}C$

V_{CC} (V)	P_{DR} (W)	P_L into 50Ω (W)	η (%)	G_p (dB)
13.8	1.2	7.0 typ.	77 typ.	7.6
13.8	3.4	13.2 typ.	79 typ.	5.8



Component values for 175MHz amplifier circuit: -

$C_1 = C_3 = C_4$ = 30pF max. concentric trimmer capacitors

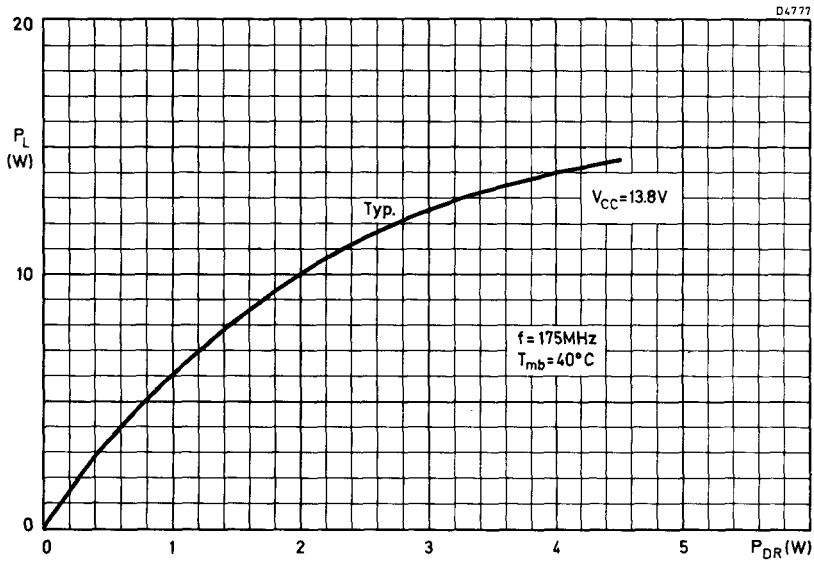
C_2 = 60pF max. concentric trimmer capacitor

L_1 = 25.4mm of straight 1.7mm Cu wire

L_2 = 3 turns of 0.5mm Cu wire on Ferrite FX1115

L_3 = 3 turns of 1.7mm Cu wire, int. diam. = 9.5mm, length = 9.5mm

L_4 = 2 turns of 2.0mm Cu wire, int. diam. = 12.7mm, length = 9.5mm

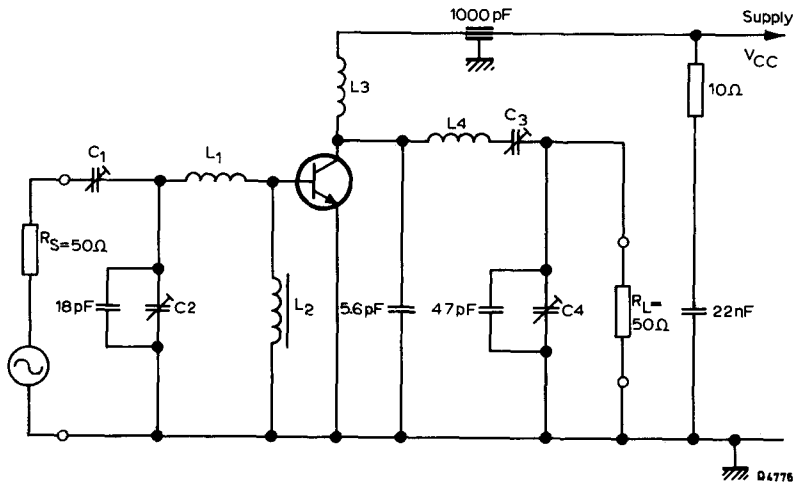


LOAD POWER PLOTTED AGAINST DRIVE POWER

APPLICATIONS INFORMATION (contd.)

R.F. performance in c.w. operation at f = 80MHz, $T_h \leq 40^{\circ}C$

V_{CC} (V)	P_{DR} (W)	P_L into 50Ω (W)	η (%)	G_p (dB)
13.8	0.5	13.5 typ.	80 typ.	14.2
6.9	0.5	5.5 typ.	80 typ.	10.3



Component values for 80MHz amplifier circuit: -

$C_1 = C_2 = C_3 = C_4$ = 4 to 29pF concentric trimmer capacitors

L_1 = 4 turns of 1.2mm Cu wire, int. diam. = 6.3mm, length = 8.0mm

L_2 = 2 turns of 0.35mm Cu wire, on Ferrite FX1115

L_3 = 5 turns of 1.2mm Cu wire, int. diam. = 6.3mm, CLOSE WOUND

L_4 = 5 turns of 1.7mm Cu wire, int. diam. = 9.6mm, length = 12mm

N-P-N SILICON PLANAR V.H.F./U.H.F. TRANSISTOR

BLY53A

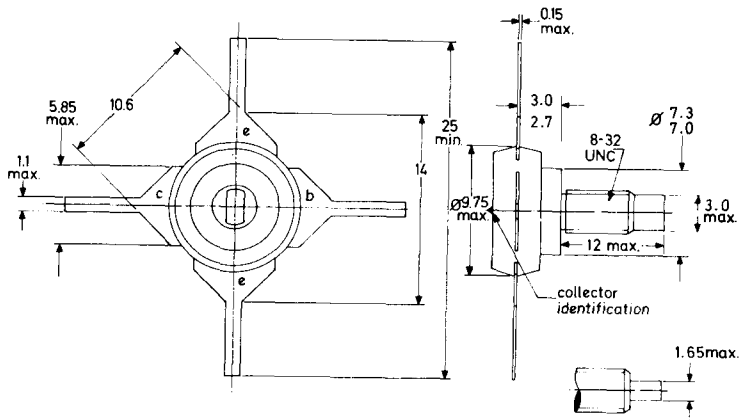
Silicon n-p-n transistor for v.h.f./u.h.f. mobile applications. The device is mounted in a plastic, capstan strip-line encapsulation.

With a supply voltage of 13.8V and a signal frequency of 470MHz, the BLY53A will produce 7.0W output into a 50Ω load.

QUICK REFERENCE DATA

V_{CC} (V)	f (MHz)	P_{DR} (W)	P_L into 50Ω (W)	η (%)	T_h (^oC)	Circuit
12.5	470	2.2	7.0 min.	65 min.	25	Un-neutralised common-emitter class B
13.8	470	2.0	7.0 min.	65 min.	25	
13.8	470	2.0	7.8 typ.	70 typ.	25	
12.5	175	0.4	7.2 typ.	66 typ.	25	

OUTLINE AND DIMENSIONS



All dimensions in mm

D3370

ACCESSORIES

Nut and lock-washer supplied with device

Torque on nut: min. 0.75Nm (7.5kg cm)

max. 0.85Nm (8.5kg cm)

RATINGS

Limiting values of operation according to the absolute maximum system.

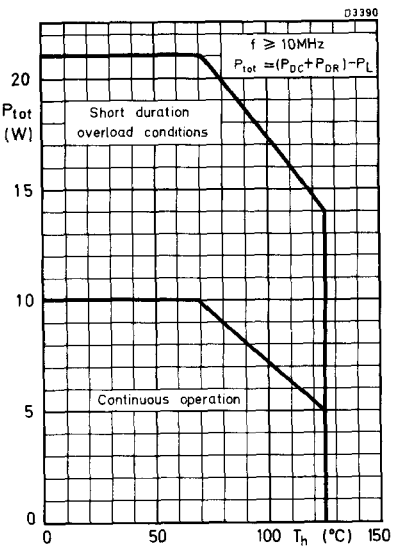
Electrical

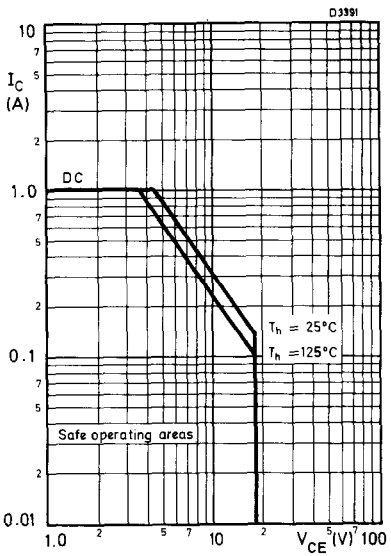
V_{CBOM} max.	36	V
V_{CESM} max. ($R_{BE} = 0$)	36	V
V_{CEO} max.	18	V
V_{EBO} max.	4.0	V
I_C max.	1.0	A
I_{CM} max. ($f \geq 10MHz$)	4.0	A
P_{tot} max. ($f \geq 10MHz$, $T_h \leq 70^oC$)	10	W

See also graph below

Temperature

T_{stg}	-65 to +150	^oC

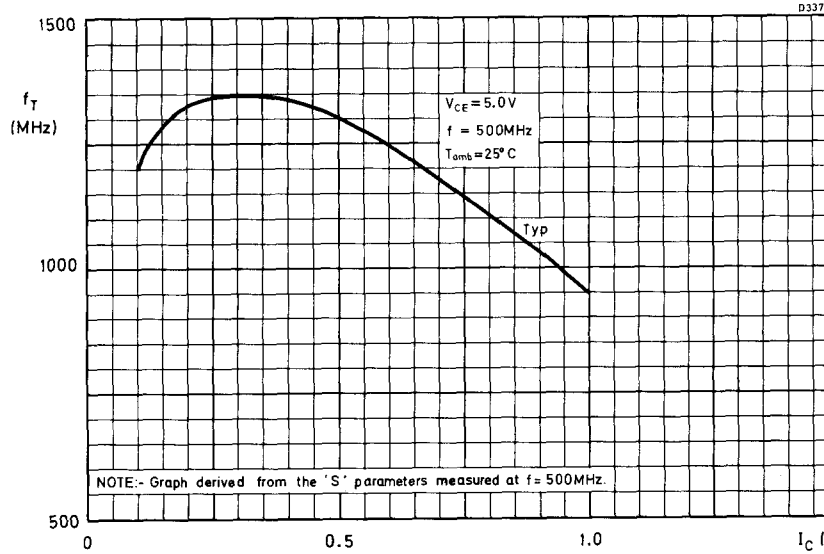


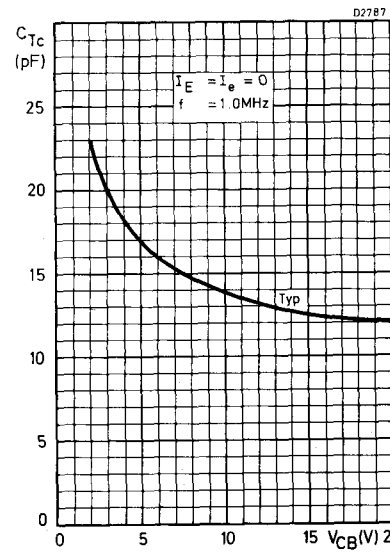


ELECTRICAL CHARACTERISTICS (T_j = 25°C unless otherwise stated)

		Min.	Typ.	Max.	
$V_{(BR)CBO}$	Collector-base breakdown voltage I_C = 10mA	36	-	-	V
$V_{(BR)CES}$	Collector-emitter breakdown voltage I_C = 10mA, R_{BE} = 0	36	-	-	V
$V_{(BR)CEO}$	Collector-emitter breakdown voltage I_C = 25mA	18	-	-	V
$V_{(BR)EBO}$	Emitter-base breakdown voltage I_E = 1.0mA	4.0	-	-	V
$V_{CE(sat)}$	Collector-emitter saturation voltage I_C = 0.5A, I_B = 0.1A	-	0.2	-	V
h_{FE}	Static forward current transfer ratio I_C = 0.5A, V_{CE} = 5.0V	10	40	-	
*f_T	Transition frequency I_C = 0.5A, V_{CE} = 5.0V, f = 500MHz	-	1300	-	MHz
C_{Tc}	Collector capacitance V_{CB} = 10V, $I_E = I_e$ = 0, f = 1.0MHz	-	14	20	pF
C_{Te}	Emitter capacitance V_{EB} = 0, $I_C = I_c$ = 0, f = 1.0MHz	-	65	-	pF
C_{cs}	Collector-stud capacitance	-	2.0	-	pF

*Derived from the 'S' parameters measured at f = 500MHz, T_{amb} = 25°C.


D3371
1500
f_T
(MHz)
1000
500
0
0.5
1.0
I_C (A)
V_{CE} = 5.0 V
f = 500MHz
T_{amb} = 25°C
Typ
NOTE:- Graph derived from the 'S' parameters measured at f = 500MHz.


D2787
C_{Tc}
(pF)
25
20
15
10
5
0
0
5
10
15
V_{CB}(V) 20
$I_E = I_e = 0$
f = 1.0MHz
Typ

APPLICATION INFORMATION

R.F. Performance in c.w. operation (T_h = 25°C)

V_{CC} (V)	f (MHz)	P_{DR} (W)	P_L into 50Ω (W)	η (%)	$\overline{z_i}$ (Ω)	$\overline{Y_L}$ (mmho)
12.5	470	2.2	7.0 min.	65 min.	-	-
13.8	470	2.0	7.0 min.	65 min.	-	-
13.8	470	2.0	7.8 typ.	70 typ.	2.3+j 6.3	50-j 36
12.5	175	0.4	7.2 typ.	66 typ.	3+j 0.5	90-j 40

At P_L = 7.0W and V_{CC} = 12.5V, the output power at heatsink temperatures between 25 and 90°C relative to that at 25°C is diminished typically by 10mW/°C.

The transistor is designed to withstand full load mismatch in the test circuit under the following conditions: -

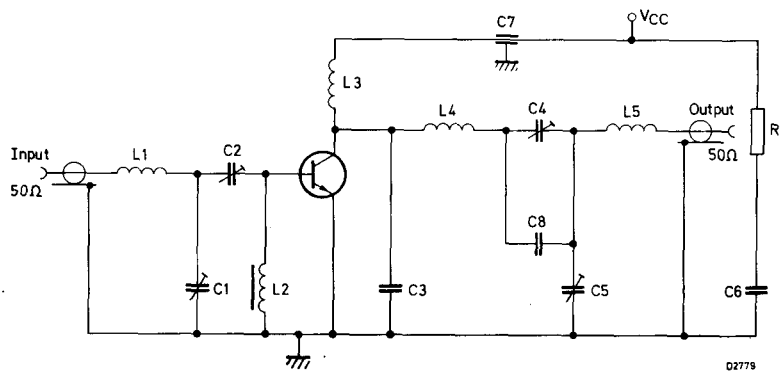
V_{CC} = 16.5V f = 470MHz T_h = 70°C

V.S.W.R. = 50: 1 at any phase

$P_{DR} = P_{DR}$ *nom.* +20%

Where P_{DR} nom. = P_{DR} for 7.0W transistor output into 50Ω load at V_{CC} = 13.8V.

470MHz Amplifier circuit

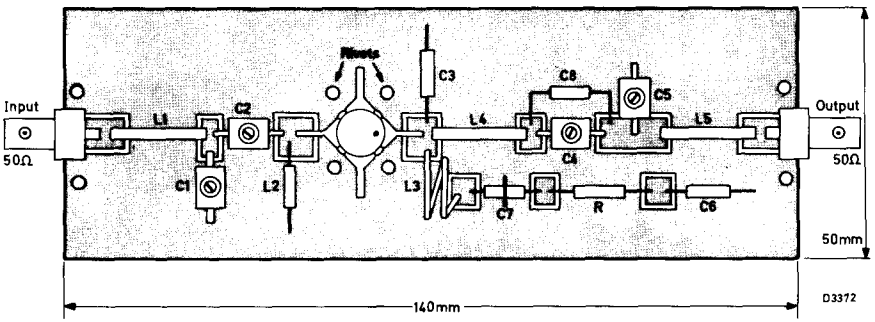


APPLICATION INFORMATION (contd.)

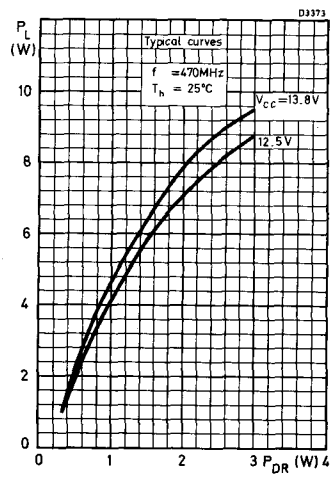
Component values for 470MHz amplifier circuit

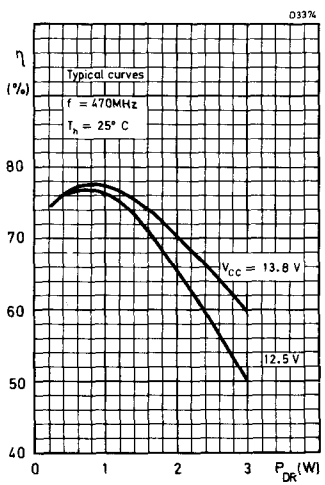
C1 = C2 = C4 = C5 = 1.8 to 18pF film dielectric trimmer capacitors
C3 = 6.8pF ceramic capacitor
C6 = 0.1μF ceramic capacitor
C7 = 4000pF feed-through capacitor
C8 = 10pF ceramic capacitor
L1 = L4 = L5 = 20mm of straight 1.2mm copper wire. Height above board = 2mm
L2 = 0.47μH choke
L3 = 1 turn of 1.7mm copper wire, int. dia. 10mm, lead length = 5mm
R = 10Ω - carbon

Component layout on 1.5mm double copper clad fibre-glass board



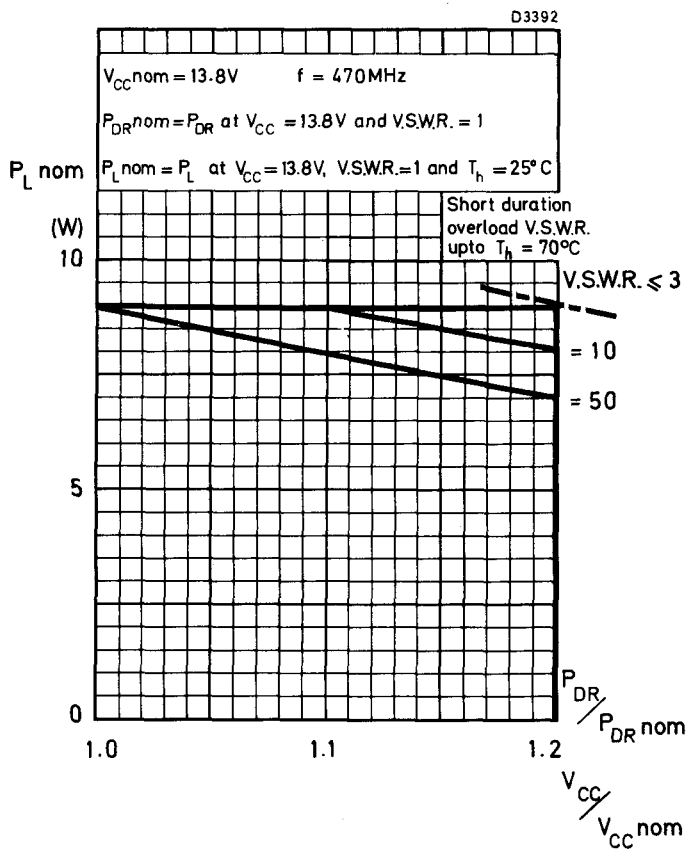
Shaded area copper
Underside area completely copper clad





TYPICAL VARIATION OF LOAD POWER AND EFFICIENCY WITH DRIVE POWER

APPLICATION INFORMATION (contd.)

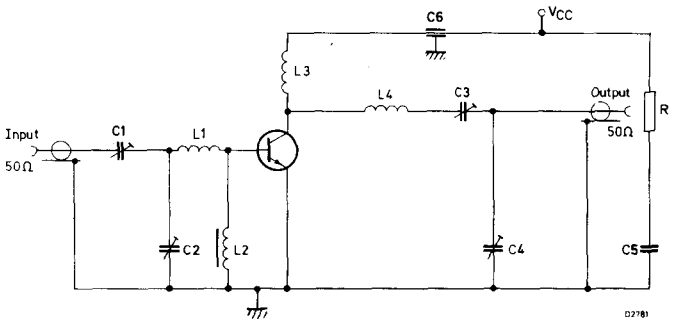


INDICATED LOAD POWER AS A FUNCTION OF OVERLOAD

The transistor is suitable for use with unstabilised supply voltages. The above graph has been derived from an evaluation of the performance of transistors matched up to 9 watts load power in the circuit on page 5, and subsequently subjected to various voltage overloads and mismatch conditions with v.s.w.r. up to 50: 1 at a heatsink temperature of 70°C. This indicates a restriction to the load power matched under nominal conditions with varying supply voltages and v.s.w.r. in the recommended circuit.

APPLICATION INFORMATION (contd.)

175MHz Amplifier circuit

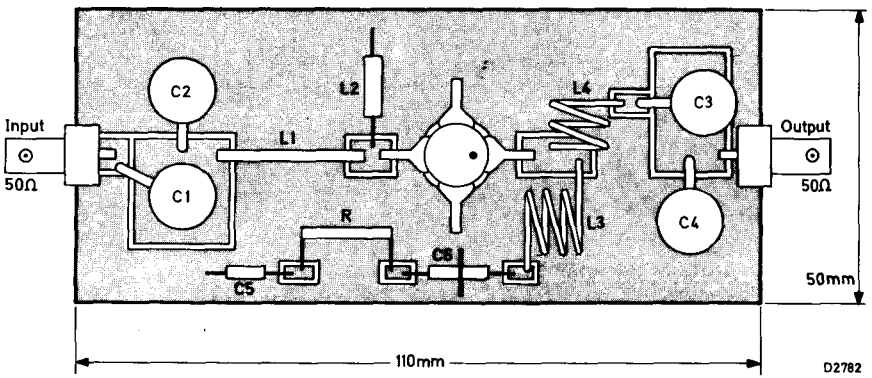


Component values for 175MHz amplifier circuit

C1 = 30pF
C2 = 60pF
C3 = 30pF
C4 = 30pF
} concentric trimmer capacitors

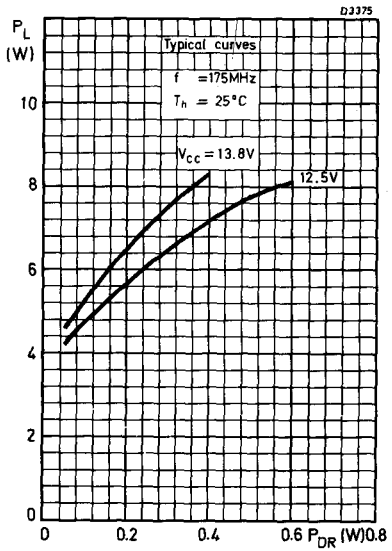
C5 = 0.25μF ceramic capacitor
C6 = 4.0nF feed-through capacitor
L1 = 25mm of straight 1.2mm copper wire. Height above board = 3mm
L2 = 3 turns of 0.5mm copper wire on Ferrite FX1115
L3 = 5 turns of 1.2mm copper wire d = 10mm. Close wound, lead length = 5mm
L4 = 3 turns of 1.2mm copper wire d = 10mm. Close wound, lead length = 5mm
R = 10Ω - carbon

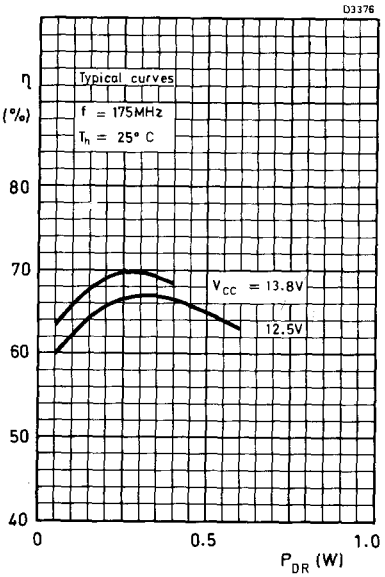
Component layout on 1.5mm single copper clad fibre-glass board



Shaded area copper

APPLICATION INFORMATION (contd.)





TYPICAL VARIATION OF LOAD POWER AND EFFICIENCY WITH DRIVE POWER

CAUTION

This device incorporates Beryllium Oxide, the dust of which is toxic. The device is entirely safe provided that it is not dismantled.

Care should be taken to ensure that all those who may handle, use or dispose of this device are aware of its nature and of the necessary safety precautions. In particular, it should never be thrown out with general industrial or domestic waste.

DISPOSAL SERVICE

Devices requiring disposal may be returned to the Mullard Service Department. They must be separately and securely packed and clearly identified. If any are damaged or broken they MUST NOT be sent through the post. In this case, advice is available from:

THE SERVICE DEPARTMENT
MULLARD LIMITED
P.O. BOX 142
NEW ROAD
MITCHAM
SURREY, CR4 4SR.

N-P-N SILICON V.H.F. POWER TRANSISTOR

BLY55

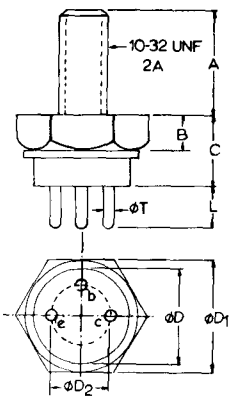
TENTATIVE DATA

Silicon n-p-n high frequency medium power transistor primarily intended for class B operation in v.h.f. amplifiers. The emitter is electrically connected to the envelope.

QUICK REFERENCE DATA			
V_{CES} max. (peak r.f. ≥1.0MHz)		40	V
V_{CEO} max.		20	V
I_{CM} max. (peak r.f. ≥1.0MHz)		3.0	A
P_{tot} max. ($T_{mb} \leq 100^{o}C$)		4.0	W
T_j max.		150	^{o}C
f_T min. (I_C=0.2A, V_{CE}=5.0V, f=100MHz)		250	MHz
Performance in a 175MHz common emitter amplifier:			
	Operation:	f.m.	
V_{CC}	Supply voltage	13.8	V
P_o	Output power	4.0	W
G_p	Power gain (typ.)	10	dB
η	Efficiency (typ.)	70	%

OUTLINE AND DIMENSIONS

Conforms to J.E.D.E.C. TO-60



	Millimetres	
	Min.	Max.
A	9.53	11.56
B	2.29	3.43
C	5.46	8.13
ØD	8.13	9.14
ØD1	10.77	11.10
ØD2	4.58	5.58
L	3.56	4.06
ØT	0.76	1.17

Emitter electrically connected to envelope

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{CES} max.	(peak r.f. ≥1.0MHz)	40	V
V_{CEO} max.		20	V
V_{EBO} max.		4.0	V
I_C max.		1.0	A
I_{CM} max.	(peak r.f. ≥1.0MHz)	3.0	A
I_{CM} max.	(peak r.f. <1.0MHz)	1.0	A
P_{tot} max.	$T_{mb}=25^oC$, f≥1.0MHz	10	W
	$T_{mb}=25^oC$, f<1.0MHz	8.0	W

See also pages 5 and 6

Temperature

T_{stg} range		-65 to +150	^oC
T_j max.	Continuous operation	150	^oC
	Intermittent operation, total duration 200 hours	200	^oC

THERMAL CHARACTERISTIC

$R_{th(j-mb)}$	12.5	degC/W

ELECTRICAL CHARACTERISTICS ($T_j=25^oC$ unless otherwise stated)

		Min.	Typ.	Max.	
I_{CES}	Collector-emitter cut-off current				
	$V_{CE}=40V$, $V_{EB}=0$	-	0.10	5.0	mA
	$V_{CE}=20V$, $V_{EB}=0$	-	0.02	0.5	mA
I_{EBO}	Emitter cut-off current $V_{EB}=4.0V$, $I_C=0$	-	0.1μ	0.5m	A
h_{FE}	Static forward current transfer ratio				
	$I_C=0.2A$, $V_{CE}=5.0V$	10	60	-	

ELECTRICAL CHARACTERISTICS (cont'd)

		Min.	Typ.	Max.	
f_T	Transition frequency I_C=0.2A, V_{CE}=5.0V, f=100MHz, T_{amb}=25°C	250	450	-	MHz
C_{tc}	Collector capacitance V_{CB}=10V, I_E=I_e=0, f=0.5MHz	-	11	15	pF
C_{te}	Emitter capacitance V_{EB}=0, I_C=I_c=0, f=0.5MHz	45	65	90	pF

RECOMMENDED OPERATING CONDITIONS

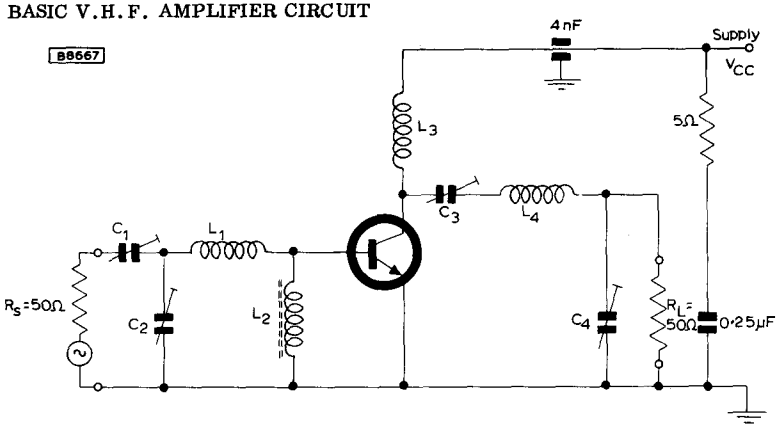
As a medium power amplifier for the output stage of a small transmitter or as a driver for larger output stages.

F.M. Operation

f	Operating frequency		175	MHz
V_{CC}	Supply voltage	nom.	13.8	V
		max.	16.5	V
V_B	Base bias voltage		0	V
P_o	Output power		4.0	W
P_i	Input power	typ.	0.4	W
		max.	0.6	W
I_{CC}	Supply current	typ.	420	mA
η	Efficiency	typ.	70	%

A heatsink of thermal resistance 10degC/W is recommended for operation in ambient temperatures up to 65°C. At temperatures >65°C, derating is necessary.

BASIC V.H.F. AMPLIFIER CIRCUIT



The emitter is earthed via the case and the emitter pin is not connected

Component values for 175MHz amplifier circuit:-

C_1	30	pF
C_2	60	pF
C_3	30	pF
C_4	30	pF
L_1	1.0	inch of straight 18 s.w.g.
L_2	3.0	turns of 24 s.w.g. on Ferrite FX1115
L_3	5.0	turns of 18 s.w.g., d=3/8", l=3/8".
L_4	3.0	turns of 18 s.w.g., d=3/8", l=3/8".

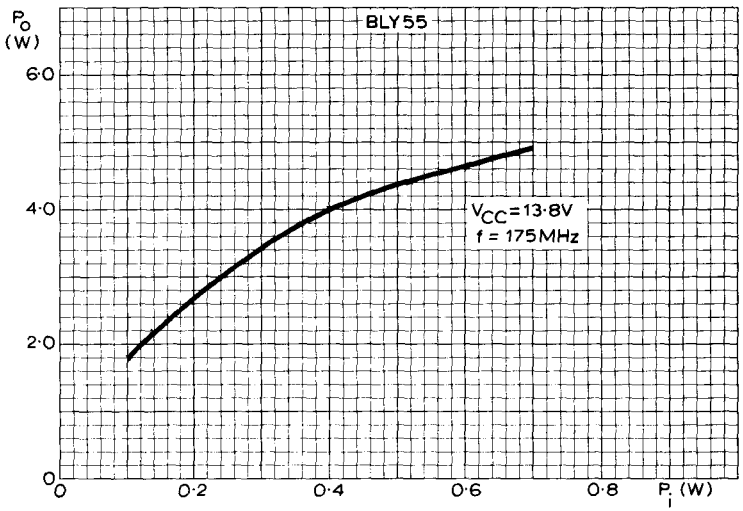
CAUTION

This device incorporates Beryllium Oxide, the dust of which is toxic. The device is entirely safe provided that it is not dismantled.

Care should be taken to ensure that all those who may handle, use or dispose of this device are aware of its nature and of the necessary safety precautions. In particular, it should never be thrown out with general industrial or domestic waste.

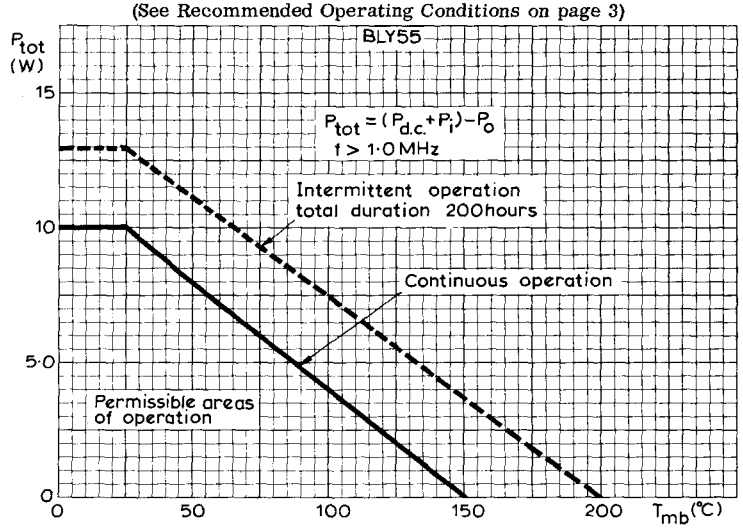
DISPOSAL SERVICE

Devices requiring disposal may be returned to Mullard Service Department. They must be separately and securely packed and clearly identified. If any are damaged or broken they MUST NOT be sent through the post. In this case advice is available from the Service Department, Mullard Ltd. New Road, Mitcham, Surrey.

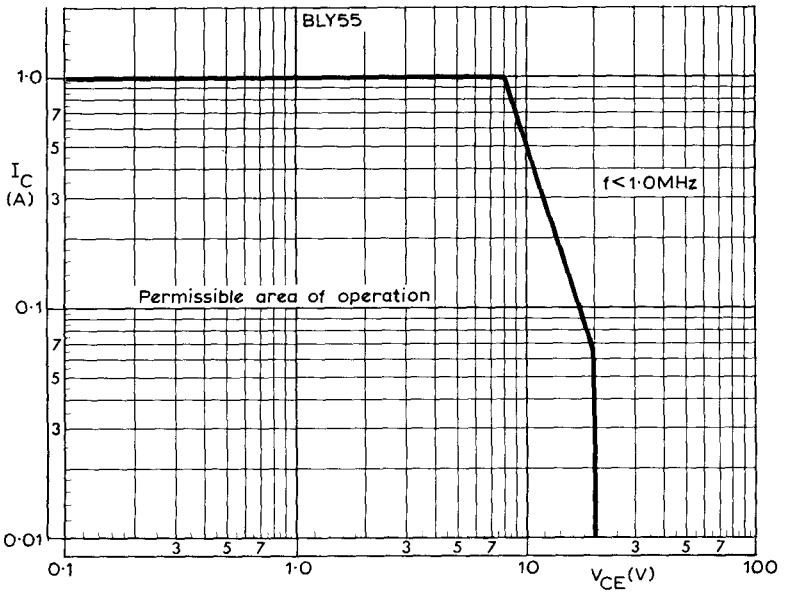


TYPICAL VARIATION OF OUTPUT POWER WITH INPUT POWER FOR V.H.F. AMPLIFIER

(See Recommended Operating Conditions on page 3)



MAXIMUM PERMISSIBLE POWER DISSIPATION PLOTTED AGAINST MOUNTING-BASE TEMPERATURE FOR FREQUENCIES > 1.0MHz



PERMISSIBLE AREA OF OPERATION FOR FREQUENCIES < 1.0MHz

PERCENTAGE POWER DERATING PLOTTED AGAINST MOUNTING-BASE TEMPERATURE FOR FREQUENCIES < 1.0MHz

N-P-N SILICON PLANAR V.H.F. TRANSISTORS

BLY83
BLY84

For details see data sheets for types BLY35, BLY36 respectively

N-P-N SILICON PLANAR V.H.F. TRANSISTORS

BLY85 BLY97

TENTATIVE DATA

The BLY85 and BLY97 are primarily intended for class B operation in the v.h.f. driver stages of mobile transmitters. The BLY85 is designed for 4W f.m. operation at 13.8V supply and the BLY97 for 4W f.m. operation at 24V supply.

QUICK REFERENCE DATA

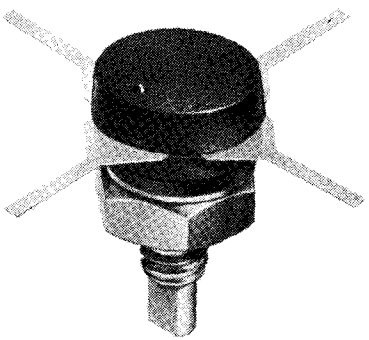
Typical c.w. performance at $T_{mb} \leq 40^{o}C$

Type No.	V_{CC} (V)	f (MHz)	P_{DR} (W)	P_L (W)	η (%)
BLY85	13.8	175	0.2	4.0	64
BLY97	24	175	0.14	4.0	52

Unless otherwise stated data are applicable to both types

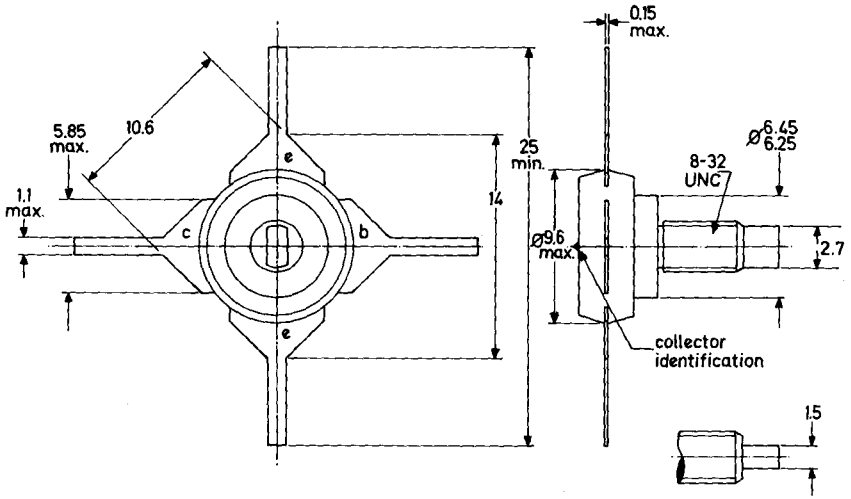
OUTLINE AND DIMENSIONS

For details see page 2



Mullard

OUTLINE AND DIMENSIONS



All dimensions in mm.

D1928

ACCESSORIES

Nut and lock-washer supplied with device
Torque on nut: min. 0.75Nm (7.5kg cm)
max. 0.85Nm (8.5kg cm)

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical		BLY85	BLY97	
V_{CES}	max. ($f \geq 1.0$MHz)	40	66	V
V_{CEO}	max.	20	33	V
V_{EBO}	max.	4.0	4.0	V
I_C	max.	1.0	1.0	A
I_{CM}	max. ($f < 1.0$MHz)	1.0	1.0	A
I_{CM}	max. ($f \geq 1.0$MHz)	3.0	3.0	A
P_{tot}	max. ($f \geq 1.0$MHz, $T_{mb} \leq 25^oC$)	10	10	W
P_{tot}	max. ($f < 1.0$MHz, $T_{mb} \leq 25^oC$)	8.0	8.0	W

Temperature			
T_{stg}	range	-30 to +150	^oC
T_j	max. (continuous operation)	150	^oC
T_j	max. (short duration overload conditions)	200	^oC

THERMAL CHARACTERISTIC

$R_{th(j-mb)}$		12.5	degC/W

ELECTRICAL CHARACTERISTICS ($T_j = 25^oC$ unless otherwise stated)

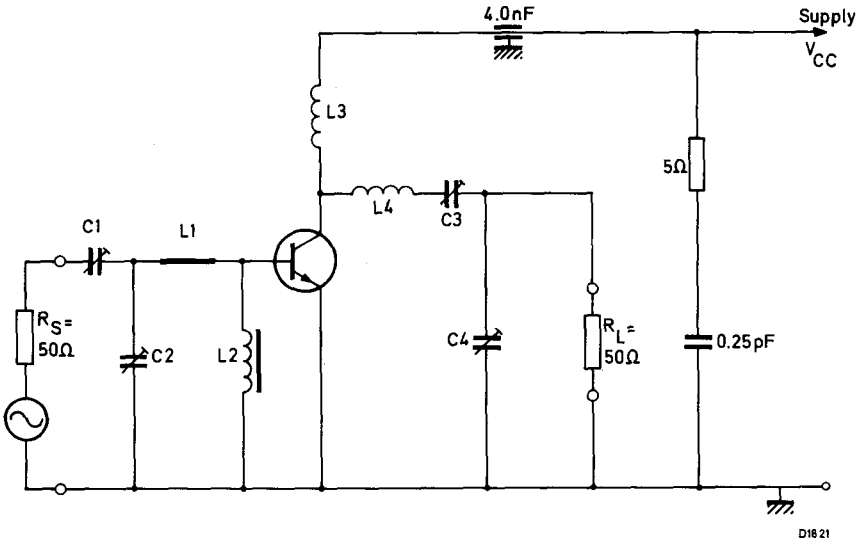
		Min.	Max.	
I_{CES}	Collector cut-off current			
	$V_{CE} = V_{CES}$ max., $V_{BE} = 0$	-	5.0	mA
	$V_{CE} = 20V$, $V_{BE} = 0$	-	0.5	mA
I_{EBO}	Emitter cut-off current $V_{EB} = 4.0V$, $I_C = 0$	-	0.5	mA
h_{FE}	Static forward current transfer ratio $I_C = 0.2A$, $V_{CE} = 5.0V$	10	-	
f_T	Transition frequency $I_C = 0.2A$, $V_{CE} = 5.0V$ $f = 100MHz$, $T_{amb} = 25^oC$	250	-	MHz
C_{Tc}	Collector capacitance $V_{CB} = 10V$, $I_E = I_e = 0$, $f = 0.5MHz$	-	15	pF
C_{Te}	Emitter capacitance $V_{EB} = 0$, $I_C = I_c = 0$, $f = 0.5MHz$	45	90	pF

R.F. Performance in c.w. operation

$T_{mb} \leq 40^oC$

Type number	V_{CC} (V)		f (MHz)	V_{CC} = nom. P_{DR} (W)	P_L (W)	I_C (mA)	G_p (dB)	η (%)
	nom.	max.			min.	max.	min.	min.
BLY85	13.8	16.5	175	0.4	4.0	480	10	60
BLY97	24	28	175	0.2	4.0	278	13	50

BASIC V.H.F. AMPLIFIER CIRCUIT



Component values for 175MHz amplifier circuit

C1 = 30pF	L1 = 1.0 inch of straight 18 s.w.g.
C2 = 60pF	L2 = 3.0 turns of 24 s.w.g. on Ferrite FX1115
C3 = 30pF	L3 = 5.0 turns of 18 s.w.g., d = 3/8", ℓ = 3/8"
C4 = 30pF	L4 = 3.0 turns of 18 s.w.g., d = 3/8", ℓ = 3/8"

CAUTION

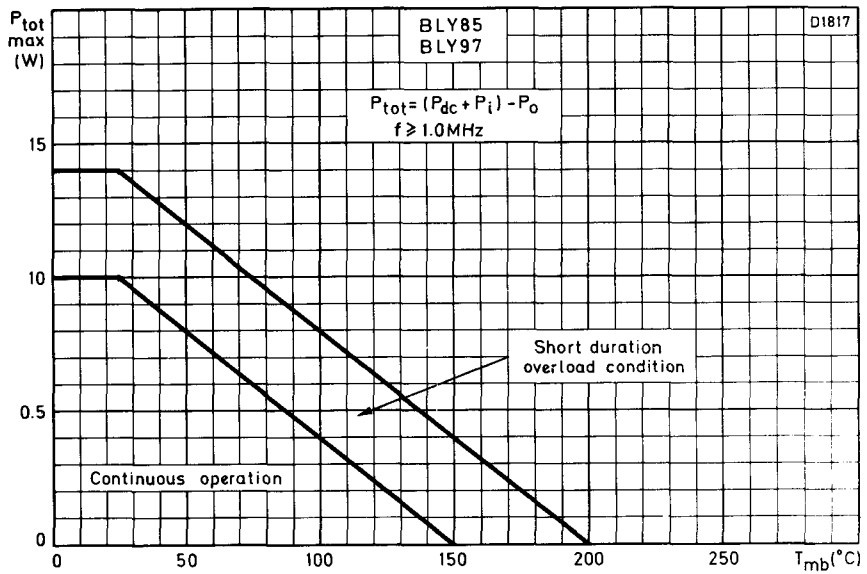
This device incorporates Beryllium Oxide, the dust of which is toxic. The device is entirely safe provided that it is not dismantled.

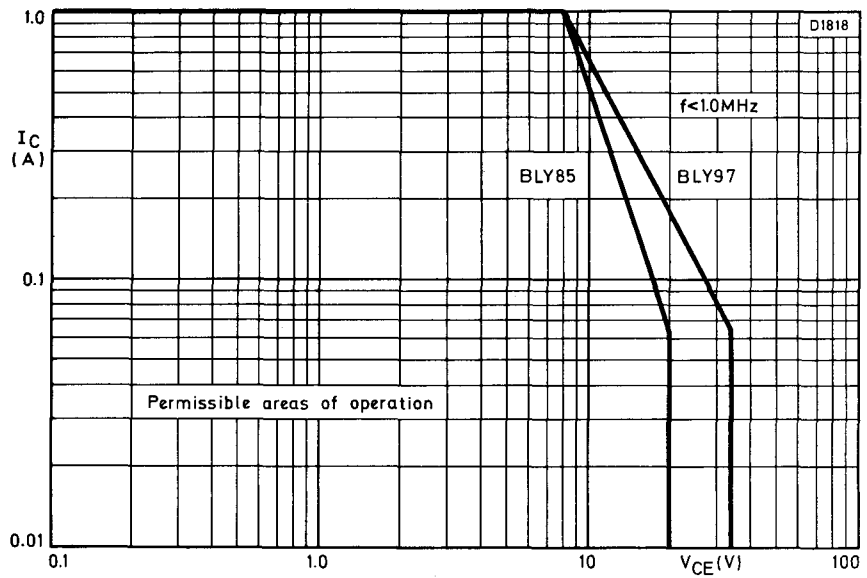
Care should be taken to ensure that all those who may handle, use or dispose of this device are aware of its nature and of the necessary safety precautions. In particular, it should never be thrown out with general industrial or domestic waste.

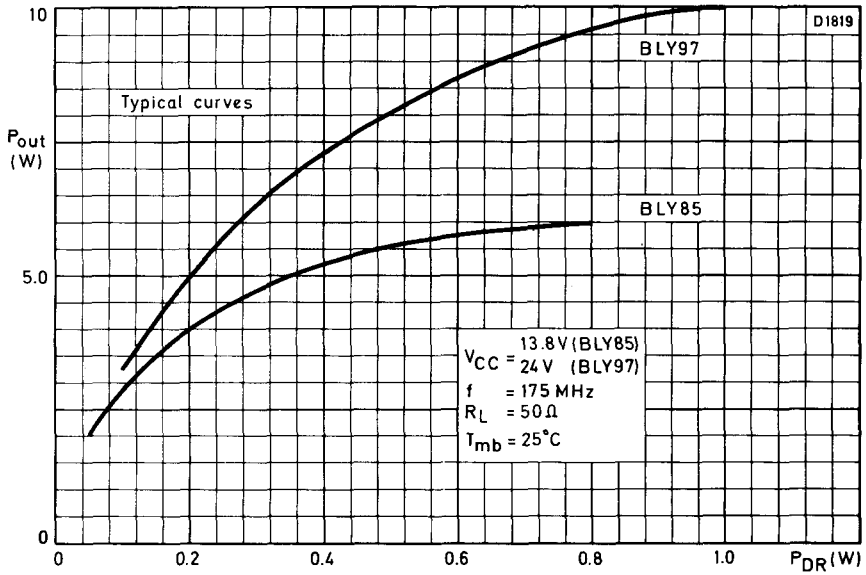
DISPOSAL SERVICE

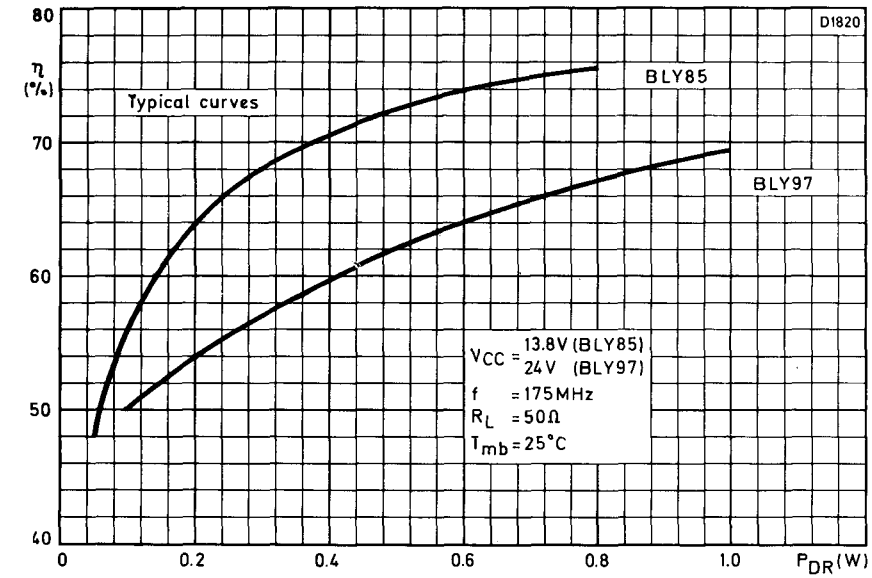
Devices requiring disposal may be returned to the Mullard Service Department. They must be separately and securely packed and clearly identified. If any are damaged or broken they MUST NOT be sent through the post. In this case, advice is available from:

THE SERVICE DEPARTMENT
MULLARD LIMITED
2.NEW ROAD, MITCHAM JUNCTION
SURREY, CR4 4XY.


P_{tot} max (W)
BLY85
BLY97
D1817
$P_{tot} = (P_{dc} + P_i) - P_o$
$f \geq 1.0$MHz
15
10
0.5
0
Short duration overload condition
Continuous operation
0
50
100
150
200
250
T_{mb}(°C)


1.0
I_C (A)
0.1
0.01
D1818
f<1.0MHz
BLY85
BLY97
Permissible areas of operation
0.1
1.0
10
V_{CE}(V)
100


D1819
BLY97
Typical curves
BLY85
P_{out} (W)
10
5.0
0
V_{CC} = 13.8V (BLY85) 24V (BLY97)
f = 175 MHz
R_L = 50Ω
T_{mb} = 25°C
0
0.2
0.4
0.6
0.8
1.0
P_{DR} (W)


D1820
η (%)
Typical curves
BLY85
BLY97
80
70
60
50
40
V_{CC} = 13.8V (BLY85) 24V (BLY97)
f = 175MHz
R_L = 50Ω
T_{mb} = 25°C
0
0.2
0.4
0.6
0.8
1.0
P_{DR} (W)

N-P-N SILICON PLANAR EPITAXIAL V.H.F. TRANSISTOR

BLY89A

N-P-N epitaxial planar transistor intended for use in class A, B and C operated mobile, industrial and military transmitters with a supply voltage of 13.5 V. The transistor is resistance stabilized. Every transistor is tested under severe load mismatch conditions with a supply overvoltage to 16.5 V. It has a $\frac{1}{4}$" capstan envelope with a moulded cap. All leads are isolated from the stud.

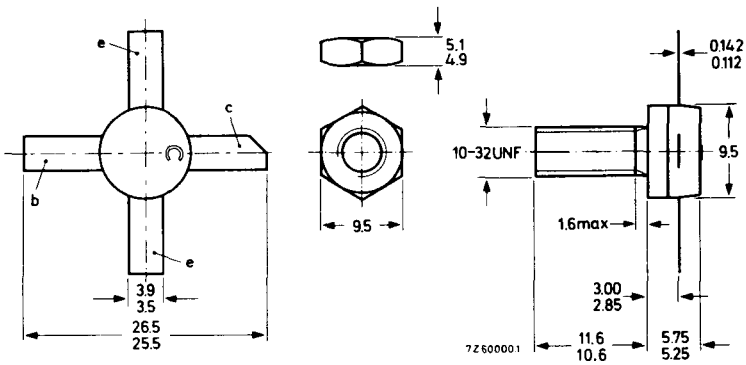
QUICK REFERENCE DATA

R. F. performance up to T_{mb} = 25 °C in an unneutralised common-emitter class B circuit.

Mode of operation	V_{CC} (V)	f (MHz)	P_S (W)	P_L (W)	I_C (A)	G_p (dB)	η (%)	$\overline{z}_i$ (Ω)	$\overline{Y}_L$ (mA/V)
c.w.	13.5	175	< 6.25	25	< 2.64	> 6	> 70	1.7+j1.4	209+j13.7

MECHANICAL DATA

Dimensions in mm



Torque on nut: min. 15 kg cm (1.5 Newton metres)
max. 17 kg cm (1.7 Newton metres)

Diameter of clearance hole in heatsink: max. 5.0 mm.
Mounting hole to have no burrs at either end. De-burring must leave surface flat; do not chamfer or countersink either end of hole.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages

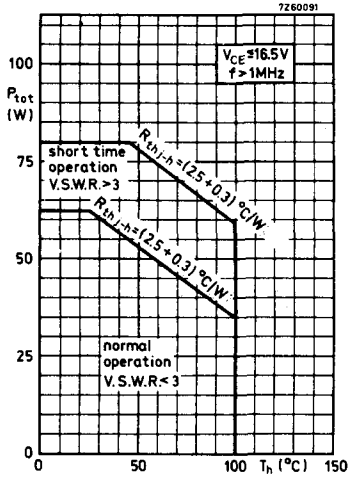
Collector-base voltage (open emitter) peak value	V_{CBOM}	max.	36	V
Collector-emitter voltage (open base)	V_{CEO}	max.	18	V
Emitter-base voltage (open collector)	V_{EBO}	max.	4	V

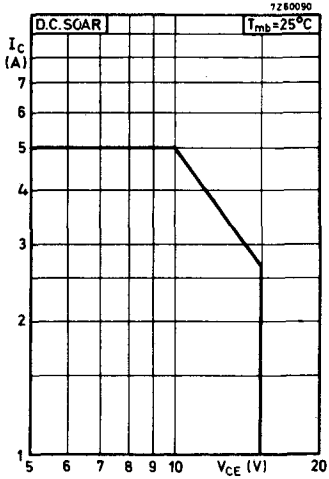
Currents

Collector current (average)	$I_{C(AV)}$	max.	5	A
Collector current (peak value) f > 1 MHz	I_{CM}	max.	10	A

Power dissipation

Total power dissipation up to T_{mb} = 25 °C f > 1 MHz	P_{tot}	max.	70	W





Temperature

Storage temperature	T_{stg}		−30 to +200	°C
Operating junction temperature	T_j	max.	200	°C

THERMAL RESISTANCE

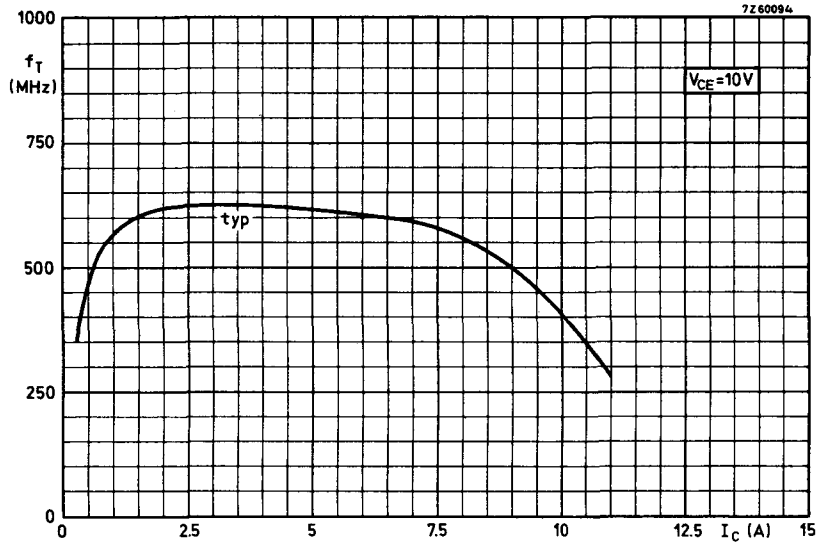
From junction to mounting base	$R_{th\ j-mb}$	=	2.5	°C/W
From mounting base to heatsink	$R_{th\ mb-h}$	=	0.3	°C/W

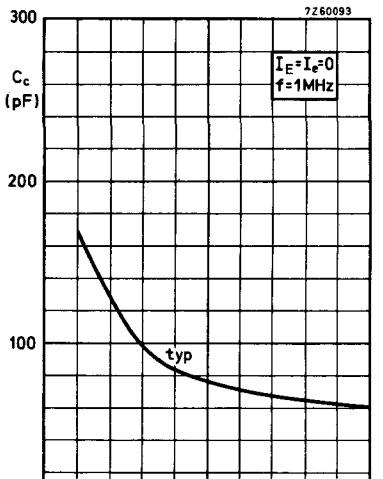
N-P-N SILICON PLANAR EPITAXIAL V.H.F. TRANSISTOR

BLY89A

CHARACTERISTICS $T_j = 25\,^{o}C$ unless otherwise specified

Breakdown voltages				
Collector-base voltage open emitter, I_C = 50 mA	$V_{(BR)CBO}$	>	36	V
Collector-emitter voltage open base, I_C = 50 mA	$V_{(BR)CEO}$	>	18	V
Emitter-base voltage open collector; I_E = 10 mA	$V_{(BR)EBO}$	>	4	V
Transient energy				
L = 25 mH; f = 50 Hz				
open base	E	>	8	mWs
$-V_{BE}$ = 1.5 V; R_{BE} = 33 Ω	E	>	8	mWs
D.C. current gain				
I_C = 1 A; V_{CE} = 5 V	h_{FE}	typ. 10 to	50 120	
Transition frequency				
I_C = 4 A; V_{CE} = 10 V	f_T	typ.	650	MHz
Collector capacitance at f = 1 MHz				
$I_E = I_e$ = 0; V_{CB} = 15 V	C_c	typ. <	65 90	pF pF
Feedback capacitance at f = 1 MHz				
I_C = 100 mA; V_{CE} = 15 V	$-C_{re}$	typ.	41	pF
Collector-stud capacitance	C_{cs}	typ.	2	pF


7Z60094
1000
f_T (MHz)
750
500
250
0
V_{CE}=10V
typ
0
2.5
5
7.5
10
12.5
I_C (A)
15


7Z60093
300
C_c (pF)
200
100
0
I_E=I_e=0
f=1MHz
typ
0
10
V_{CB} (V)
20

N-P-N SILICON PLANAR EPITAXIAL V.H.F. TRANSISTOR

BLY89A

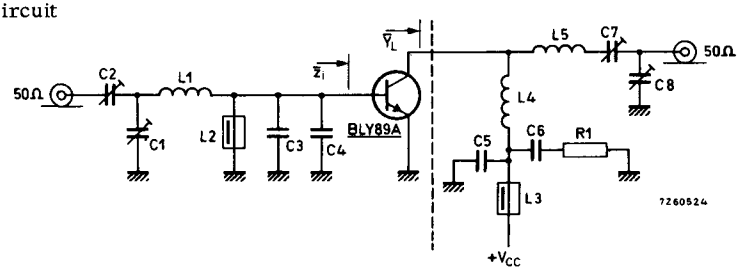
APPLICATION INFORMATION

R. F. performance in c.w. operation (unneutralised common-emitter class B circuit)

V_{CC} = 13.5 V; T_{mb} up to 25 °C

f(MHz)	P_S (W)	P_L (W)	I_C (A)	G_p (dB)	η (%)	$\bar{z}_i$ (Ω)	$\bar{Y}_L$ (mA/V)
175	< 6.25	25	< 2.64	> 6	> 70	1.7+j1.4	209+j13.7

Test circuit



C1 = 4 to 44 pF film dielectric trimmer
C2 = 2 to 22 pF film dielectric trimmer
C3 = C4 = 47 pF ceramic
C5 = 100 pF ceramic
C6 = 150 nF polyester
C7 = 4 to 104 pF film dielectric trimmer
C8 = 4 to 64 pF film dielectric trimmer

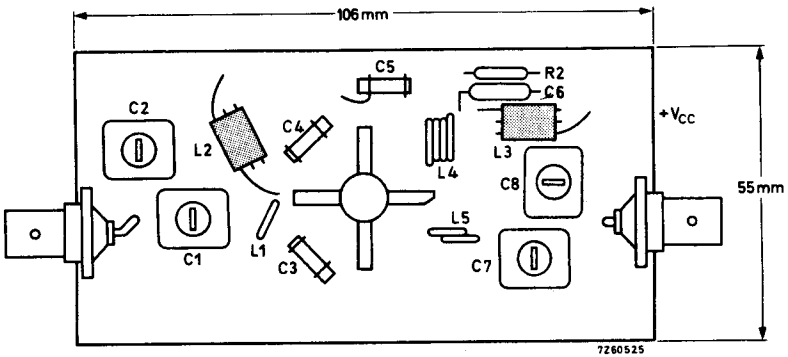
L1 = 0.5 turn enamelled Cu wire (1.5 mm); int.diam. 6 mm; leads 2x6 mm
L2 = L3 = ferroxcube choke
L4 = 3.5 turns closely wound enamelled Cu wire (1.5 mm); int.diam. 6 mm; leads 2x6 mm
L5 = 1 turn enamelled Cu wire (1.5 mm); int.diam. 6 mm; leads 2x6 mm

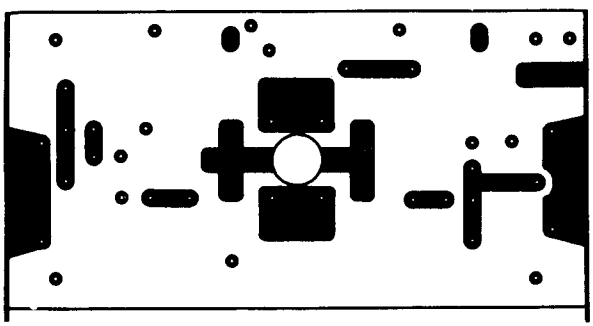
R1 = 10 Ω carbon

Component lay-out for 175 MHz see page 6.

APPLICATION INFORMATION (continued)

Component lay-out and printed circuit board for 175 MHz test circuit.

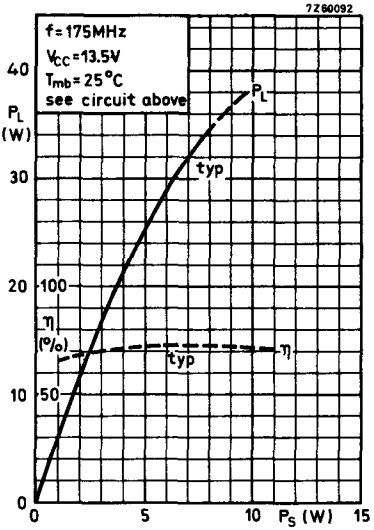




The circuit and the components are situated on one side of the epoxy fibre-glass board, the other side being fully metallised to serve as earth. Earth connections are made by means of hollow rivets.

N-P-N SILICON PLANAR EPITAXIAL V.H.F. TRANSISTOR

BLY89A



CAUTION

This device incorporates Beryllium Oxide, the dust of which is toxic. The device is entirely safe provided that it is not dismantled.

Care should be taken to ensure that all those who may handle, use or dispose of this device are aware of its nature and of the necessary safety precautions. In particular, it should never be thrown out with general industrial or domestic waste.

DISPOSAL SERVICE

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THE SERVICE DEPARTMENT
MULLARD LIMITED
2.NEW ROAD, MITCHAM JUNCTION
SURREY, CR4 4XY.

N-P-N SILICON PLANAR EPITAXIAL V.H.F. TRANSISTOR

BLY90

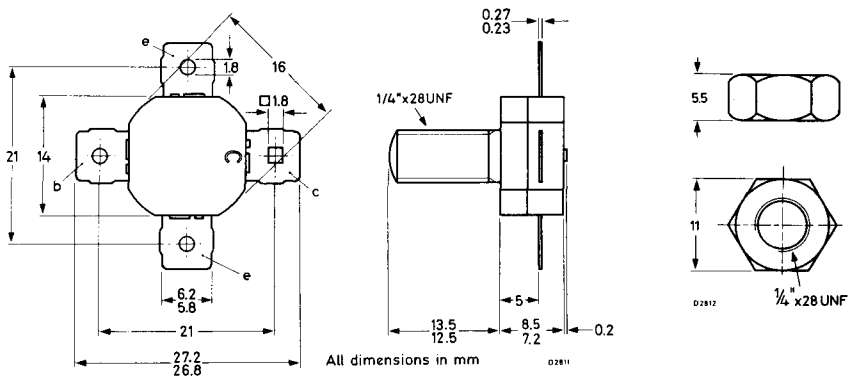
N-P-N silicon planar epitaxial v.h.f. power transistor for use in class A, B and C operated mobile transmitters with a 12.5V supply. It can withstand severe load mismatch conditions with a supply overvoltage up to 15V.
The BLY90 has a plastic encapsulated stripline package with all leads isolated from the stud.

QUICK REFERENCE DATA

R.F. performance in an un-neutralised common-emitter class B circuit, $T_h \leq 25^oC$.

Operation	V_{CC} (V)	f (MHz)	P_{DR} (W)	P_L (W)	I_C (A)	G_p (dB)	η (%)	$\overline{z_i}$ (Ω)	$\overline{Y_L}$ (mA/V)
c.w.	12.5	175	<15.8	50	<5.33	>5.0	>75	1.3 + j1.6	270 + j160

OUTLINE AND DIMENSIONS



Torque on nut: min. 23kg cm (2.3N m), max. 27kg cm (2.7N m)

Diameter of clearance hole in heatsink: max. 6.5mm

Note: Do not chamfer the edges of the mounting hole when removing burrs.

RATINGS

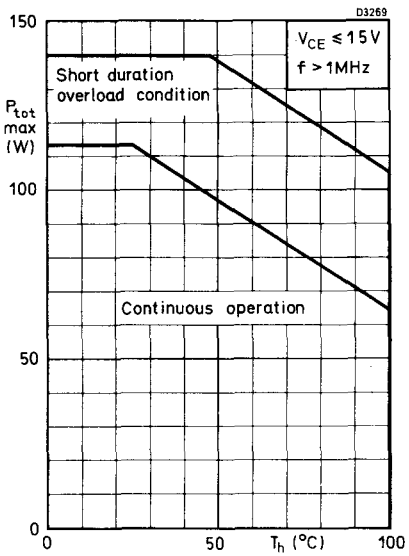
Limiting values of operation according to the absolute maximum system.

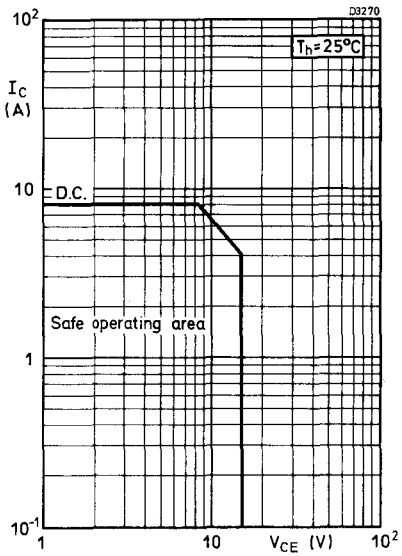
Electrical

V_{CBOM} max.	36	V
V_{CEO} max.	18	V
V_{EBO} max.	4.0	V
$I_{C(AV)}$ max.	8.0	A
I_{CM} max. (f >1MHz)	20	A
P_{tot} max. (f >1MHz, $T_h \leq 25^oC$)	130	W

Temperature

T_{stg}	-65 to +200	^oC



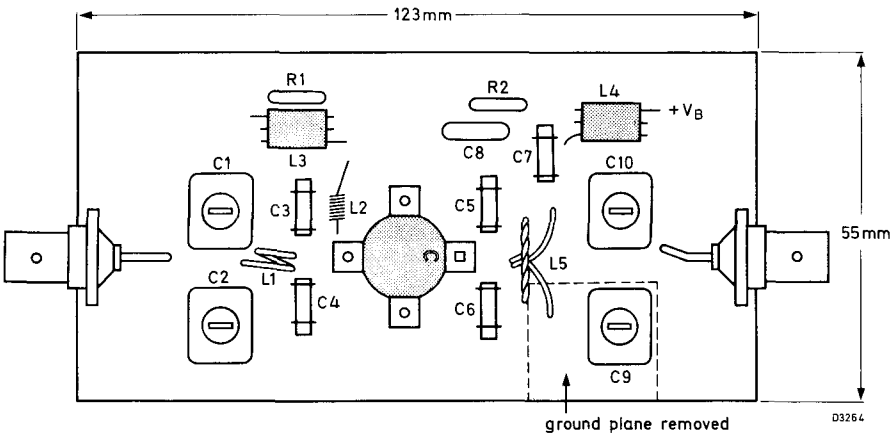


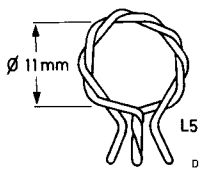
ELECTRICAL CHARACTERISTICS (T_j = 25°C unless otherwise stated)

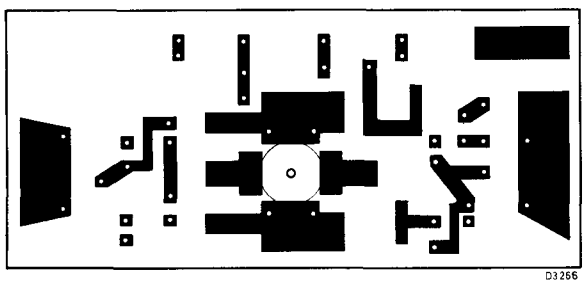
		Min.	Typ.	Max.	
$V_{(BR)CBO}$	Collector-base breakdown voltage open emitter, I_C = 100mA	36	-	-	V
$V_{(BR)CEO}$	Collector-emitter breakdown voltage open base, I_C = 100mA	18	-	-	V
$V_{(BR)EBO}$	Emitter-base breakdown voltage open collector, I_E = 25mA	4.0	-	-	V
E	Transient energy L = 25mH, f = 50Hz				
	open base	8.0	-	-	mWs
	$-V_{BE}$ = 1.5V, R_{BE} = 33Ω	8.0	-	-	mWs
h_{FE}	Static forward current transfer ratio I_C = 1.0A, V_{CE} = 5.0V	10	50	-	
f_T	Transition frequency I_C = 6.0A, V_{CE} = 10V	-	550	-	MHz
C_{Tc}	Collector capacitance $I_E = I_e$ = 0, V_{CB} = 15V, f = 1MHz	-	130	160	pF
$-C_{re}$	Feedback capacitance I_C = 200mA, V_{CE} = 15V	-	82	-	pF
C_{cs}	Collector-stud capacitance	-	3.5	-	pF

APPLICATION INFORMATION (contd.)

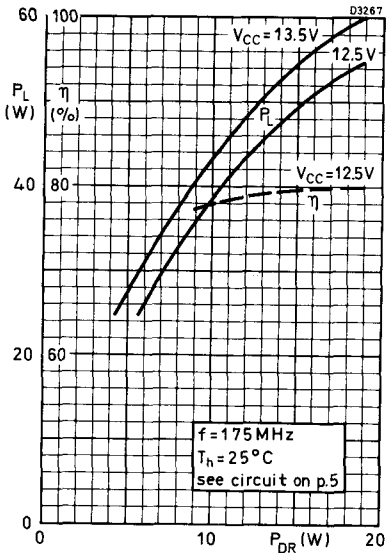
Component layout and printed circuit board for 175MHz test circuit

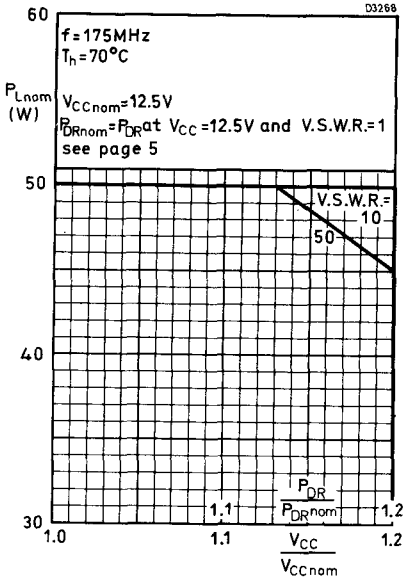






The circuit and the components are situated on one side of the epoxy fibre-glass board, the other side being fully metallised to serve as earth. Earth connections are made by means of hollow rivets.





INDICATED LOAD POWER
AS A FUNCTION OF OVERLOAD
(see note below)

NOTE

The transistor is developed for use with unstabilised supply voltages. The above graph has been derived from an evaluation of the performance of transistors matched up to 50 watts load power in the circuit on page 5, and subsequently subjected to various voltage overloads and mismatch conditions with V.S.W.R. up to 50: 1 at a heatsink temperature of 70°C. This indicates a restriction to the load power matched under nominal conditions with varying supply voltages and V.S.W.R. in the recommended circuit.

CAUTION

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THE SERVICE DEPARTMENT
MULLARD LIMITED
2 NEW ROAD, MITCHAM JUNCTION
SURREY, CR4 4XY.

N-P-N SILICON PLANAR EPITAXIAL V.H.F. TRANSISTOR

BLY93A

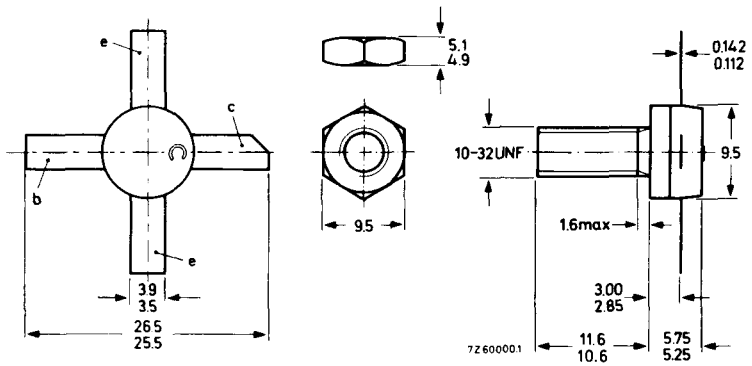
N-P-N epitaxial planar transistor intended for use in class A, B and C operated mobile, industrial and military transmitters with a supply voltage of 28 V. The transistor is resistance stabilized. Every transistor is tested under severe load mismatch conditions. It has a $\frac{1}{4}$" capstan envelope with a moulded cap. All leads are isolated from the stud.

QUICK REFERENCE DATA

R.F. performance up to T_{mb} = 25 °C in an unneutralised common-emitter class B circuit.

Mode of operation	V_{CC} (V)	f (MHz)	P_S (W)	P_L (W)	I_C (A)	G_p (dB)	η (%)	$\overline{z}_i$ (Ω)	$\overline{Y}_L$ (mA/V)
c.w.	28	175	< 3.1	25	< 1.5	> 9	> 60	1.0+j1.2	57.7-j52.7

MECHANICAL DATA Dimensions in mm



Torque on nut: min. 15 kg cm
(1.5 Newton metres)
max. 17 kg cm
(1.7 Newton metres)

Diameter of clearance hole in heatsink: max. 5.0 mm.
Mounting hole to have no burrs at either end. De-burring must leave surface flat; do not chamfer or countersink either end of hole.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltages

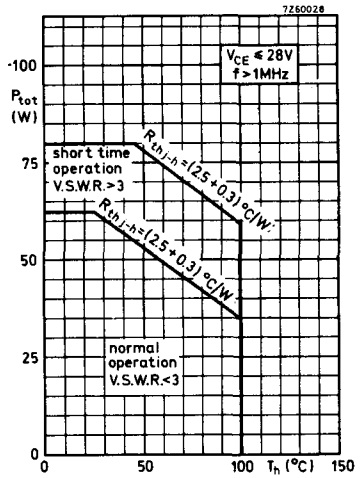
Collector-base voltage (open emitter) peak value	V_{CBOM}	max.	65	V
Collector-emitter voltage (open base)	V_{CEO}	max.	36	V
Emitter-base voltage (open collector)	V_{EBO}	max.	4	V

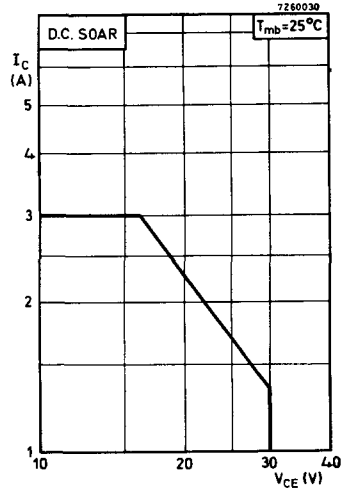
Currents

Collector current (average)	$I_{C(AV)}$	max.	3	A
Collector current (peak value) f > 1 MHz	I_{CM}	max.	9	A

Power dissipation

Total power dissipation up to T_{mb} = 25 °C f > 1 MHz	P_{tot}	max.	70	W





Temperature

Storage temperature	T_{stg}		−30 to +200	°C
Operating junction temperature	T_j	max.	200	°C

THERMAL RESISTANCE

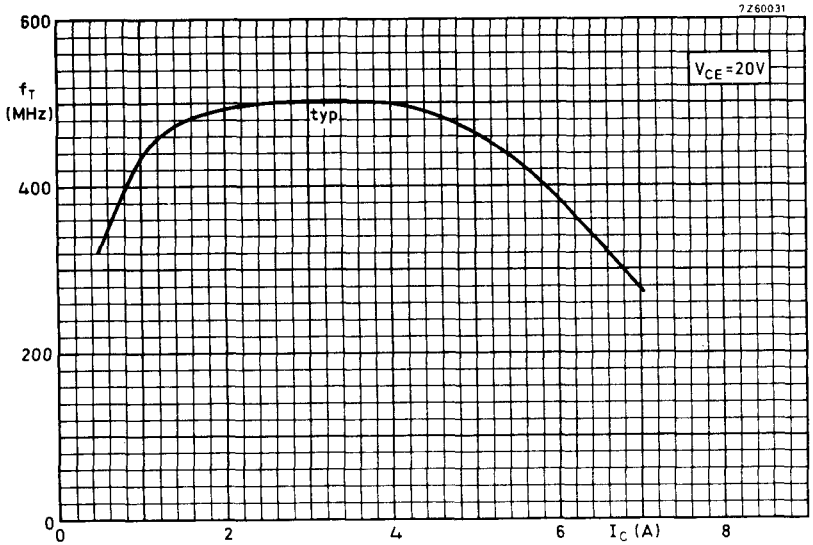
From junction to mounting base	$R_{th\ j-mb}$	=	2.5	°C/W
From mounting base to heatsink	$R_{th\ mb-h}$	=	0.3	°C/W

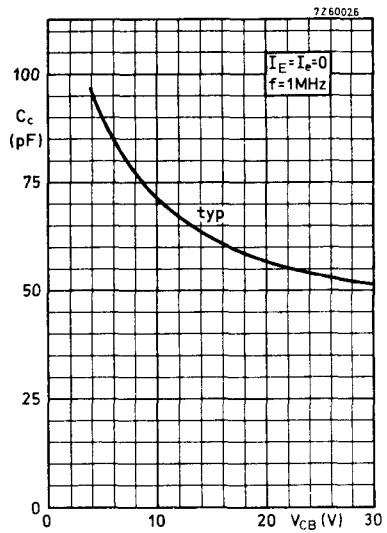
N-P-N SILICON PLANAR EPITAXIAL V.H.F. TRANSISTOR

BLY93A

CHARACTERISTICS $T_j = 25\ ^oC$ unless otherwise specified

Breakdown voltages				
Collector-base voltage open emitter, $I_C = 50$ mA	$V_{(BR)CBO}$	>	65	V
Collector-emitter voltage open base, $I_C = 50$ mA	$V_{(BR)CEO}$	>	36	V
Emitter-base voltage open collector; $I_E = 10$ mA	$V_{(BR)EBO}$	>	4	V
Transient energy				
$L = 25$ mH; $f = 50$ Hz				
open base	E	>	8	mWs
$-V_{BE} = 1.5$ V; $R_{BE} = 33\ \Omega$	E	>	8	mWs
D.C. current gain				
$I_C = 1$ A; $V_{CE} = 5$ V	h_{FE}	typ. 10 to	50 120	
Transition frequency				
$I_C = 3$ A; $V_{CE} = 20$ V	f_T	typ.	500	MHz
Collector capacitance at $f = 1$ MHz				
$I_E = I_e = 0$; $V_{CB} = 30$ V	C_c	typ. <	50 65	pF pF
Feedback capacitance at $f = 1$ MHz				
$I_C = 100$ mA; $V_{CE} = 30$ V	$-C_{re}$	typ.	31	pF
Collector-stud capacitance	C_{cs}	typ.	2	pF


7Z60031
600
f_T
(MHz)
400
200
0
0
2
4
6
I_C (A)
8
typ
V_{CE}=20V


7Z60028
100
C_c
(pF)
75
50
25
0
0
10
20
V_{CB} (V)
30
typ
$I_E = I_e = 0$
f=1MHz

N-P-N SILICON PLANAR EPITAXIAL V.H.F. TRANSISTOR

BLY93A

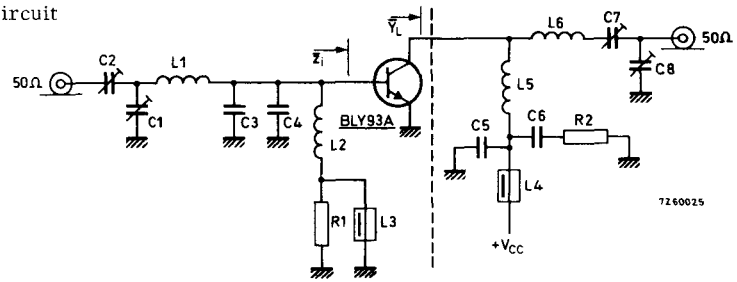
APPLICATION INFORMATION

R. F. performance in c. w. operation (unneutralised common-emitter class B circuit)

V_{CC} = 28 V; T_{mb} = 25 °C

f(MHz)	P_S (W)	P_L (W)	I_C (A)	G_p (dB)	η (%)	$\bar{z}_i$ (Ω)	$\bar{Y}_L$ (mA/V)
175	< 3.1	25	< 1.5	> 9	> 60	1.0+j1.2	57.7-j52.7

Test circuit



C1 = 4 to 44 pF film dielectric trimmer
C2 = 2 to 22 pF film dielectric trimmer
C3 = C4 = 47 pF ceramic
C5 = 100 pF ceramic
C6 = 150 nF polyester
C7 = 4 to 104 pF film dielectric trimmer
C8 = 4 to 64 pF film dielectric trimmer

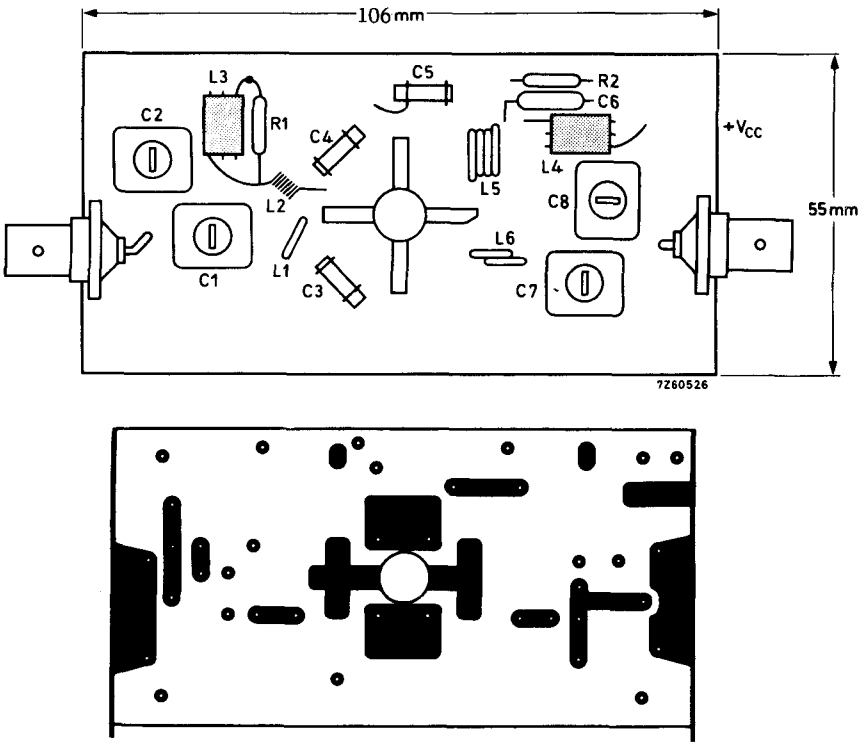
L1 = 0.5 turn enamelled Cu wire (1.5 mm); int.diam.6 mm; leads 2x6 mm
L2 = 6 turns closely wound enamelled Cu wire (0.7 mm); int.diam.4 mm; leads 2x4 mm
L3 = L4 = ferroxcube choke
L5 = 3.5 turns enamelled Cu wire (1.5 mm); int.diam. 6 mm; leads 2x6 mm
L6 = 1.5 turns enamelled Cu wire (1.5 mm); int.diam. 6 mm; leads 2x6 mm

R1 = R2 = 10 Ω carbon

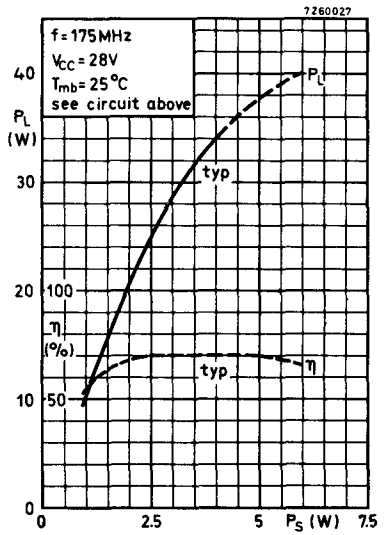
Component lay-out for 175 MHz see page 6.

APPLICATION INFORMATION (continued)

Component lay-out and printed circuit board for 175 MHz test circuit.



The circuit and the components are situated on one side of the epoxy fibre-glass board, the other side being fully metallised to serve as earth. Earth connections are made by means of hollow rivets.



CAUTION

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SURREY, CR4 4XY.

N-P-N SILICON PLANAR EPITAXIAL V.H.F. TRANSISTOR

BLY94

Silicon n-p-n planar epitaxial transistor intended for use in class A, B and C operated mobile transmitters with a 28V supply. It is designed to withstand severe load mismatch conditions.

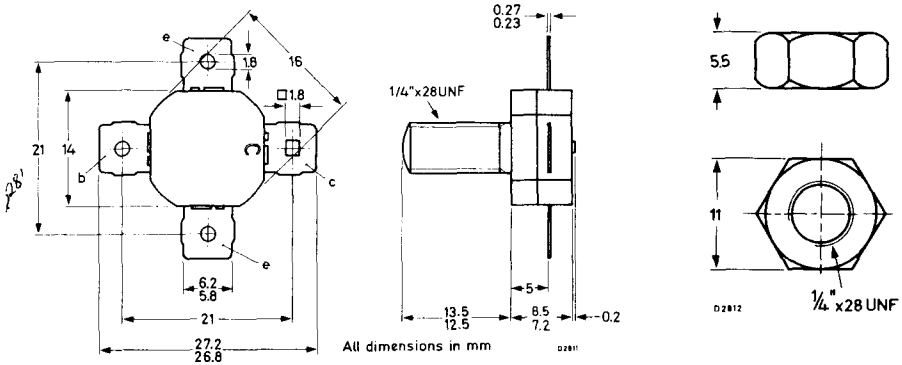
The BLY94 is in a plastic-encapsulated stripline package with all leads isolated from the stud.

QUICK REFERENCE DATA

R.F. performance up to $T_h = 25^oC$ in an un-neutralised common-emitter class B circuit.

Operation	V_{CC} (V)	f (MHz)	P_{DR} (W)	P_L (W)	I_C (A)	G_p (dB)	η (%)	$\overline{z_i}$ (Ω)	$\overline{Y_L}$ (mA/V)
c.w.	28	175	< 10	50	< 2.75	> 7	> 65	0.7+j1.45	120-j70

OUTLINE AND DIMENSIONS



Torque on nut: min. 23 kg cm (2.3 N m)
max. 27 kg cm (2.7 N m)

Diameter of clearance hole in heatsink: max. 6.5mm

Note: Do not chamfer the edges of the mounting holes when removing burrs.

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

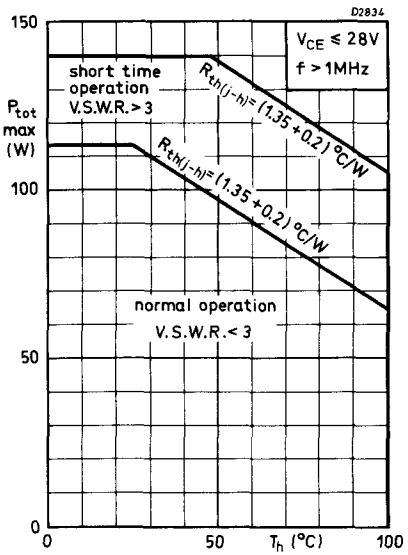
V_{CBOM} max.	65	V
V_{CEO} max.	36	V
V_{EBO} max.	4.0	V
$I_{C(AV)}$ max.	6.0	A
I_{CM} max. (f > 1MHz)	12	A
P_{tot} max. ($T_h \leq 25^oC$, f > 1MHz)	130	W

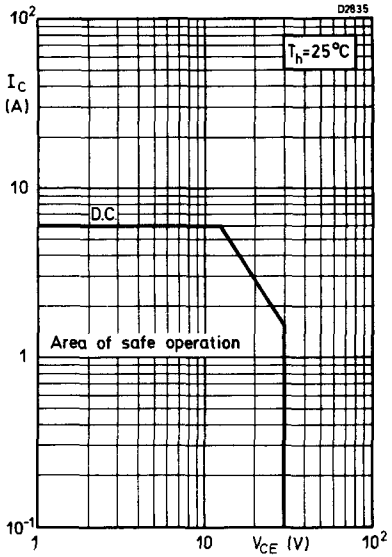
Temperature

T_{stg}	-65 to +200	^oC
T_j max.	200	^oC

THERMAL CHARACTERISTICS

$R_{th(j-mb)}$	1.35	degC/W
$R_{th(mb-h)}$	0.2	degC/W



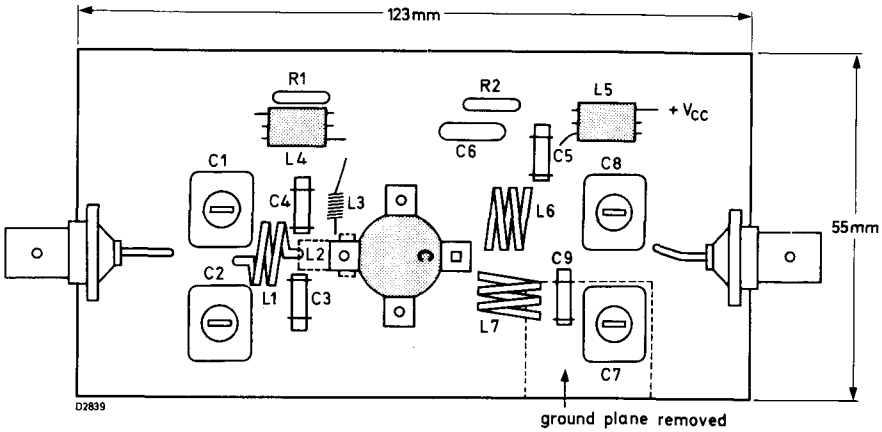


ELECTRICAL CHARACTERISTICS ($T_j = 25^oC$ unless otherwise stated)

		Min.	Typ.	Max.	
$V_{(BR)CBO}$	Collector-base breakdown voltage open emitter, $I_C = 100mA$	65	-	-	V
$V_{(BR)CEO}$	Collector-emitter breakdown voltage open base, $I_C = 100mA$	36	-	-	V
$V_{(BR)EBO}$	Emitter-base breakdown voltage open collector, $I_E = 25mA$	4.0	-	-	V
E	Transient energy $L = 25mH$, $f = 50Hz$				
	open base	8.0	-	-	mWs
	$-V_{BE} = 1.5V$, $R_{BE} = 33\Omega$	8.0	-	-	mWs
h_{FE}	Static forward current transfer ratio $I_C = 1.0A$, $V_{CE} = 5V$	10	-	120	
f_T	Transition frequency $I_C = 6.0A$, $V_{CE} = 20V$	-	500	-	MHz
C_{Tc}	Collector capacitance $I_E = I_e = 0$, $V_{CB} = 30V$, $f = 1.0MHz$	-	75	130	pF
$-C_{re}$	Feedback capacitance $I_C = 100mA$, $V_{CE} = 30V$	-	47	-	pF
C_{cs}	Collector-stud capacitance	-	3.5	-	pF

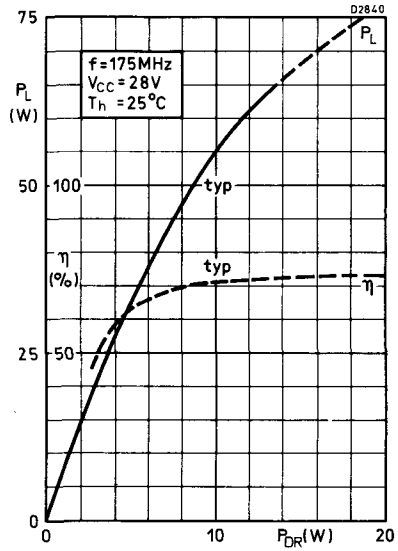
APPLICATION INFORMATION (contd.)

Component layout on a printed circuit board for 175MHz test circuit



The underside of the epoxy fibre-glass board is completely metallised and serves as earth.

Earth connections are made by means of hollow rivets.



CAUTION

This device incorporates Beryllium Oxide, the dust of which is toxic. The device is entirely safe provided that it is not dismantled.

Care should be taken to ensure that all those who may handle, use or dispose of this device are aware of its nature and of the necessary safety precautions. In particular, it should never be thrown out with general industrial or domestic waste.

DISPOSAL SERVICE

Devices requiring disposal may be returned to the Mullard Service Department. They must be separately and securely packed and clearly identified. If any are damaged or broken they MUST NOT be sent through the post. In this case, advice is available from:

THE SERVICE DEPARTMENT
MULLARD LIMITED
2 NEW ROAD, MITCHAM JUNCTION
SURREY, CR4 4XY.

N-P-N SILICON PLANAR V.H.F. TRANSISTOR

BLY97

For details see data sheet for type BLY85

SILICON P-N-P-N PLANAR TRANSISTOR

BRY39

For use as a PROGRAMMABLE UNIJUNCTION TRANSISTOR

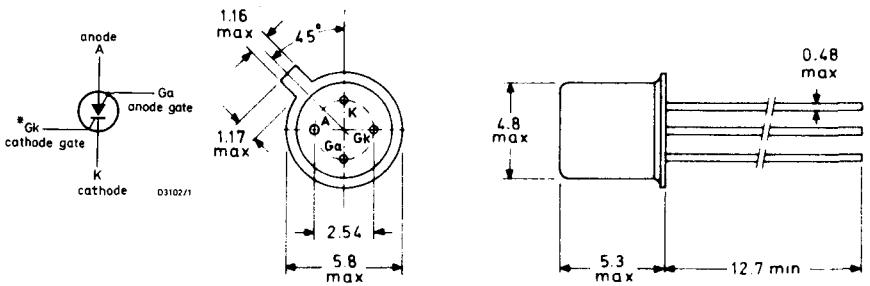
The BRY39 is a planar p-n-p-n trigger device in a TO-72 metal envelope, intended for use in switching applications such as motor control, oscillators, relay replacement, timers, pulse shaper, trigger device, etc.

See also data on BRY39 as a Silicon Controlled Switch and as a Thyristor Tetrode.

QUICK REFERENCE DATA			
V_{GaA} max.	Anode gate to anode voltage	70	V
I_A max.	Anode current, d.c. ($T_{case} \leq 85^oC$)	250	mA
T_j max.	Junction temperature	150	^oC
I_P	Peak point current ($V_S = 10V$, $R_G = 10k\Omega$)	<5.0	μA
I_V	Valley point current ($V_S = 10V$, $R_G = 10k\Omega$)	>50	μA

OUTLINE AND DIMENSIONS

Conforming to B.S. 3934 SO-12A/SB4-3
J.E.D.E.C. TO-72



All dimensions in mm

03073

Anode gate connected to case

*For the application of the BRY39 as a programmable unijunction transistor, cathode gate is not used.

Accessories available: 56246 (distance disc) and 56263 (cooling clip)

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{GaA} max.	Anode gate to anode voltage	70	V
I_A max.	Anode current (d.c.) $T_{amb} \leq 25^oC$	175	mA
	$T_{case} \leq 85^oC$	250	mA
I_{ARM} max.	Repetitive peak anode current $t = 10\mu s$, $d = 0.01$	2.5	A
I_{ASM} max.	Non-repetitive peak anode current $t = 10\mu s$, $T_j = 150^oC$	3.0	A
$\frac{dI_A}{dt}$	Rate of rise of anode current up to $I_A = 2.5A$	20	A/μs

Temperature

T_{stg}	Storage temperature	-65 to +200	^oC
T_j max.	Junction temperature	150	^oC

THERMAL CHARACTERISTICS

$R_{th(j\text{-}amb)}$	Thermal resistance from junction to ambient, in free air	0.45	$^oC/mW$
$R_{th(j\text{-}case)}$	Thermal resistance from junction to case	0.15	$^oC/mW$

ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^oC$ unless otherwise stated)

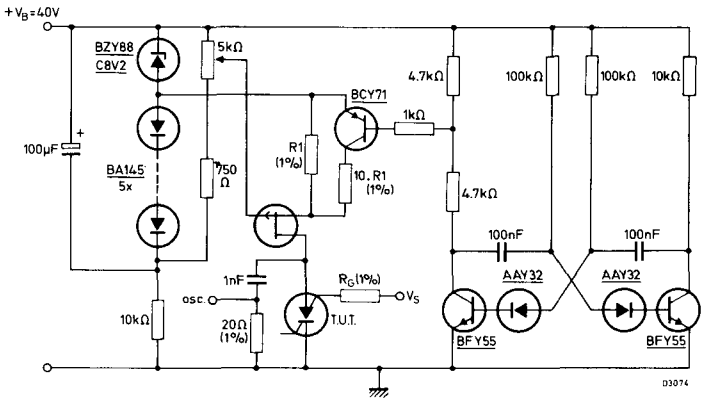
		Min.	Typ.	Max.	
I_P	Peak point current				
	$V_S = 10V$; $R_G = 10k\Omega$	-	-	5.0	μA
	$V_S = 10V$, $R_G = 1M\Omega$	-	-	1.0	μA
I_V	Valley point current				
	$V_S = 10V$, $R_G = 10k\Omega$	50	-	-	μA
	$V_S = 10V$, $R_G = 1M\Omega$	-	-	50	μA

ELECTRICAL CHARACTERISTICS (contd.)

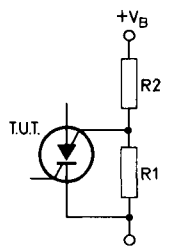
Practical test circuit

(1) Remove BCY71 for measurement of I_P

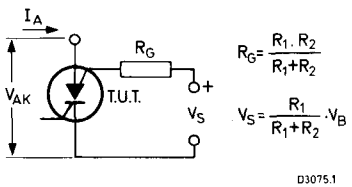
(2) The value of R1 depends on the voltage range of the voltmeter used.



Equivalent test circuit



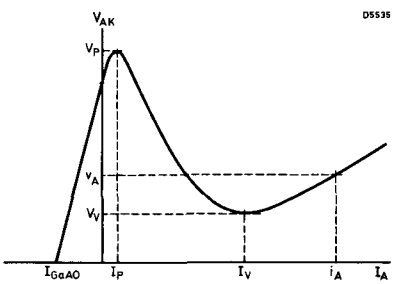
BRY39 with "program" resistors R1 and R2



Equivalent test circuit for characteristics testing

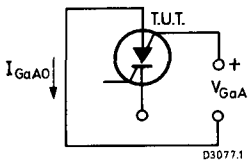
Offset voltage (see graph on page 6)

$$V_{offset} = V_P - V_S \ (I_A = 0)$$

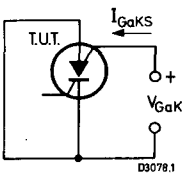


ELECTRICAL CHARACTERISTICS (contd.)

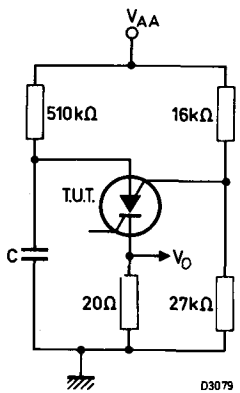
		Min.	Typ.	Max.	
I_{GaAO}	Anode gate to anode leakage current $I_K = 0$, $V_{GaA} = 70V$	-	-	10	nA

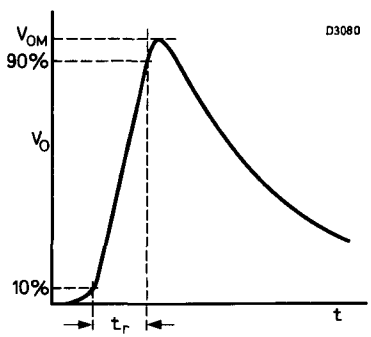


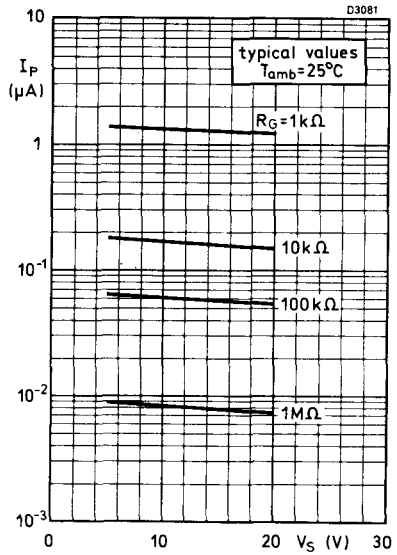
I_{GaKS}	Anode gate to cathode leakage current $V_{AK} = 0$, $V_{GaK} = 70V$	-	-	100	nA

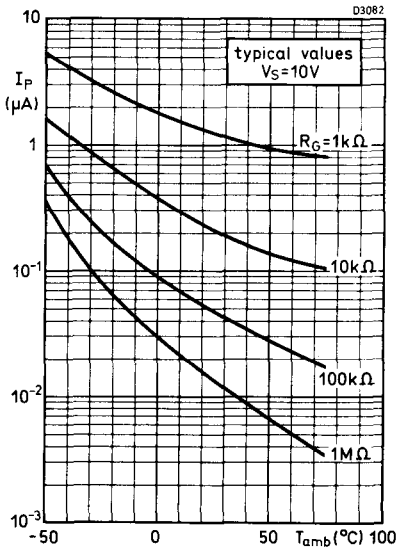


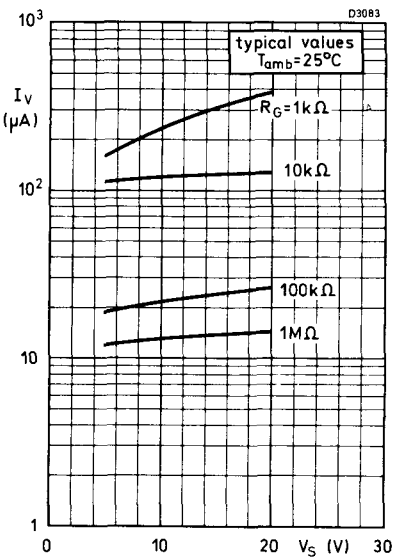
V_A	Anode voltage $I_A = 100mA$	-	-	1.4	V
V_{OM}	Peak output voltage $V_{AA} = 20V$, $C = 0.2\mu F$	6.0	-	-	V
t_r	Rise time $V_{AA} = 20V$, $C = 10nF$	-	-	80	ns

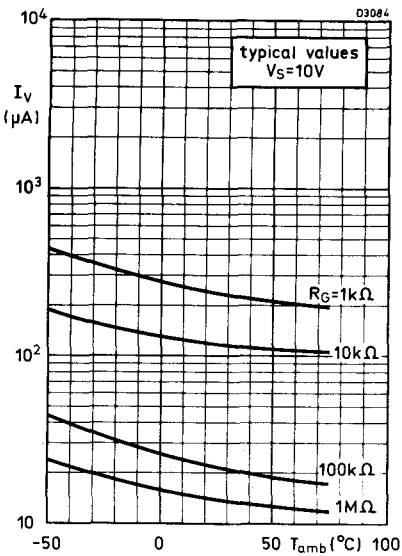


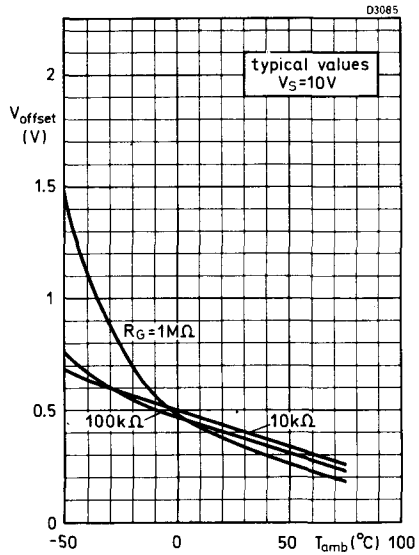


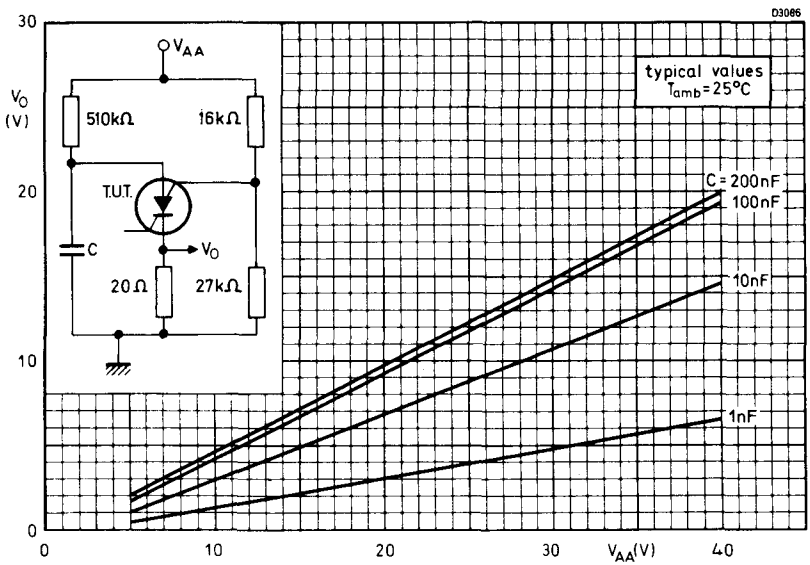

D3081
typical values
Tamb=25°C
RG=1kΩ
10kΩ
100kΩ
1MΩ
IP (μA)
10
1
10-1
10-2
10-3
0
10
20
VS (V)
30


D3082
typical values
VS=10V
RG=1kΩ
10kΩ
100kΩ
1MΩ
IP (μA)
10
1
10-1
10-2
10-3
-50
0
50
Tamb(°C)
100


D3083
typical values
Tamb=25°C
RG=1kΩ
10kΩ
100kΩ
1MΩ
IV (μA)
10³
10²
10
1
0
10
20
VS (V)
30


D3084
typical values
VS=10V
RG=1kΩ
10kΩ
100kΩ
1MΩ
IV (μA)
10⁴
10³
10²
10
-50
0
50
Tamb(°C)
100


D3085
typical values
V_S=10V
V_{offset} (V)
2
1.5
1
0.5
0
R_G=1MΩ
100kΩ
10kΩ
-50
0
50
T_{amb}(°C)
100


D3086
typical values
T_{amb}=25°C
V_O (V)
30
20
10
0
V_{AA}
510kΩ
16kΩ
T.U.T.
C
V_O
20Ω
27kΩ
C = 200nF
100nF
10nF
1nF
0
10
20
30
V_{AA}(V)
40

SILICON P-N-P-N PLANAR TRANSISTOR

BRY39

For use as a SILICON CONTROLLED SWITCH

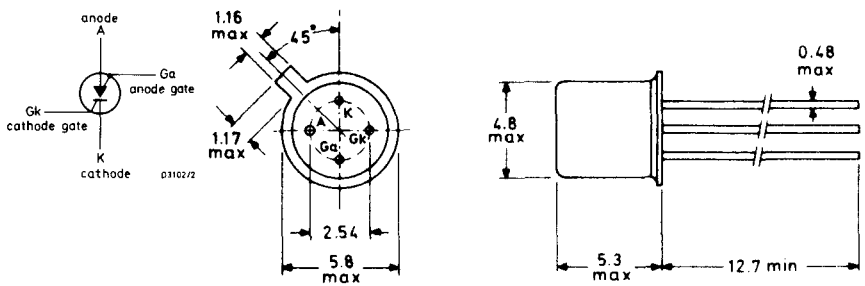
The BRY39 is a silicon planar p-n-p-n switch in a TO-72 metal envelope, intended as a driver for numerical indicator tubes and other switching applications. It is an integrated pnp-npn transistor pair, with all electrodes accessible. See also data on BRY39 as a Thyristor Tetrode and as a Programmable Unijunction Transistor.

QUICK REFERENCE DATA

$-V_{EBO}$	Max. emitter-base voltage of the P-N-P transistor (open collector)	70	V
V_{CBO}	Max. collector-base voltage of the N-P-N transistor (open emitter)	70	V
$-I_{ERM}$	Max. repetitive peak emitter current	2.5	A
P_{tot}	Max. total dissipation ($T_{amb} \leq 25^{o}C$)	275	mW
T_j	Max. operating junction temperature	150	^{o}C
V_{AK}	Forward on-state voltage $I_A = 50mA$, $I_{Ga} = 0$, $R_{GkK} = 10k\Omega$	<1.4	V
I_H	Holding current $I_{Ga} = 10mA$, $-V_{BB} = 2.0V$, $R_{GkK} = 10k\Omega$	<1.0	mA
t_{on}	Turn-on time	<0.25	μs
t_q	Turn-off time	<5.0	μs

OUTLINE AND DIMENSIONS

Conforming to B.S. 3934 SO-12A/SB4-3
J.E.D.E.C. TO-72



All dimensions in mm

D3073

The collector of the n-p-n transistor (anode gate) is connected to the case
Accessories available: 56246 (distance disc) and 56263 (cooling clip)

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

	p-n-p	n-p-n	
V_{CBO} max. (open emitter)	-70	70*	V
V_{CER} max. (R_{BE} = 10kΩ)	-	70*	V
V_{CEO} max. (open base)	-70	-	V
V_{EBO} max. (open collector)	-70*	5.0†	V
I_E max. (d.c.)	175	-175	mA
I_{ERM} max. (repetitive peak value, t_p = 10μs, d = 0.01)	2.5	-2.5	A
I_C max. (d.c.)	-	175**	mA
I_{CM} max. (peak value)	-	175‡	mA
P_{tot} max. ($T_{amb} \leq 25^oC$)	275		mW

Temperature

T_j max.	150	^oC
T_{stg} range	-65 to +200	^oC

THERMAL CHARACTERISTIC

$R_{th\ (j\text{-}amb)}$	0.45	$^oC/mW$

*In numerical indicator tube driver circuits higher voltages are allowed, provided the collector current does not exceed a d.c. value of 1.0mA.

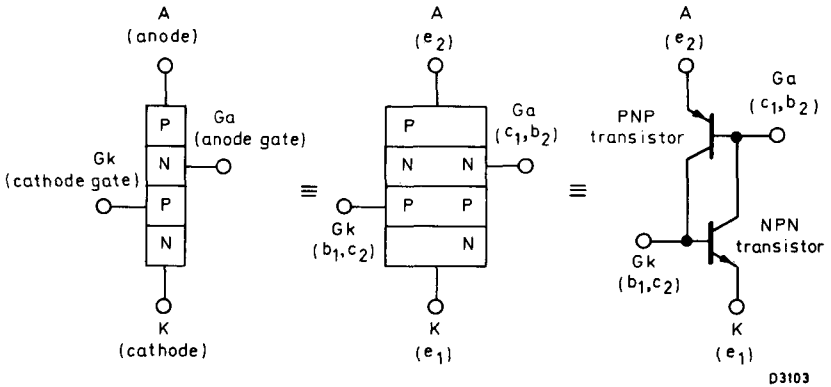
†In numerical indicator tube driver circuits higher voltages are allowed during the discharge of a capacitor of a maximum value of 390pF, provided the charge does not exceed 50nC.

**Provided the I_E rating is not exceeded.

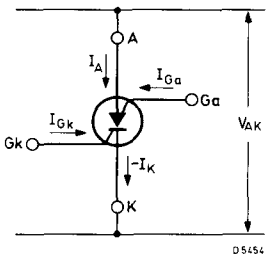
‡During switching on, the device can withstand the discharge of a capacitor of maximum value of 500pF. This capacitor is charged when the transistor is in cut-off condition, with a collector supply voltage of 160V and a series resistance of 100kΩ.

SYMBOLS AND EQUIVALENT CIRCUITS

P-N-P-N structure and a two transistor equivalent circuit



Silicon controlled switch



ELECTRICAL CHARACTERISTICS ($T_j = 25^oC$ unless otherwise stated)

INDIVIDUAL N-P-N TRANSISTOR		Min.	Typ.	Max.	
I_{CER}	Collector cut-off current				
	$V_{CE} = 70V$, $R_{BE} = 10k\Omega$	-	-	100	nA
	$V_{CE} = 70V$, $R_{BE} = 10k\Omega$, $T_j = 150^oC$	-	-	10	μA
I_{EBO}	Emitter cut-off current				
	$I_C = 0$, $V_{EB} = 5.0V$, $T_j = 150^oC$	-	-	10	μA

ELECTRICAL CHARACTERISTICS (Contd.)

INDIVIDUAL N-P-N TRANSISTOR

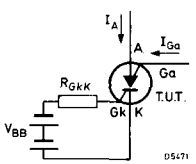
		Min.	Typ.	Max.	
$V_{CE(sat)}$	Collector-emitter saturation voltage I_C = 10mA, I_B = 1.0mA	-	-	500	mV
$V_{BE(sat)}$	Base-emitter saturation voltage I_C = 10mA, I_B = 1.0mA	-	-	900	mV
h_{FE}	D.C. current gain I_C = 10mA, V_{CE} = 2.0V	50	-	-	
f_T	Transition frequency I_C = 10mA, V_{CE} = 2.0V	-	300	-	MHz
C_{Tc}	Collector capacitance $I_E = I_e$ = 0, V_{CB} = 20V	-	-	5.0	pF
C_{Te}	Emitter capacitance $I_C = I_c$ = 0, V_{EB} = 1.0V	-	-	25	pF

INDIVIDUAL P-N-P TRANSISTOR

$-I_{CEO}$	Collector cut-off current I_B = 0, $-V_{CE}$ = 70V, T_j = 150°C	-	-	10	μA
$-I_{EBO}$	Emitter cut-off current I_C = 0, $-V_{EB}$ = 70V, T_j = 150°C	-	-	10	μA
h_{FE}	D.C. current gain I_E = 1.0mA, V_{CB} = 0	0.25	-	2.5	

COMBINED DEVICE

V_{AK}	Forward on-state voltage (R_{GkK} = 10kΩ) I_A = 50mA, I_{Ga} = 0	-	-	1.4	V
	I_A = 50mA, I_{Ga} = 0, T_j = -55°C	-	-	1.9	V
	I_A = 1.0mA, I_{Ga} = 10mA	-	-	1.2	V
I_H	Holding current I_{Ga} = 10mA, $-V_{BB}$ = 2.0V, R_{GkK} = 10kΩ	-	-	1.0	mA

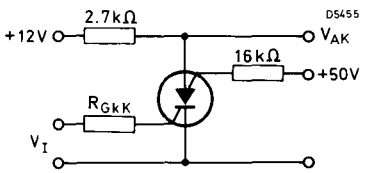


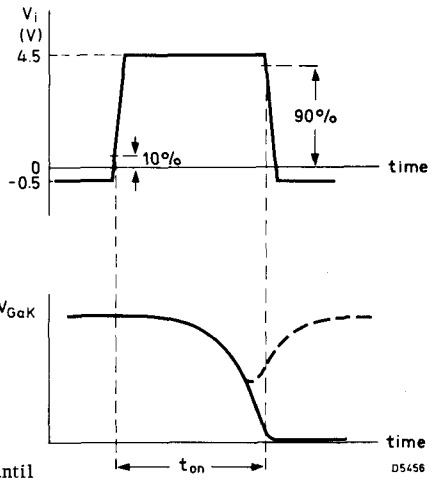
ELECTRICAL CHARACTERISTICS (Contd.) ($T_j = 25^oC$ unless otherwise stated)

Switching times (see also page 7)

t_{on} Turn-on time when switched from $-V_{GkK} = 0.5V$ to $+V_{GkK} = 4.5V$; $R_{GkK} = 1.0k\Omega$ <0.25 μs

$R_{GkK} = 10k\Omega$ <1.5 μs





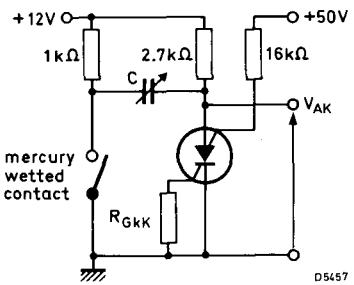
Pulse duration increased until dashed curve disappears

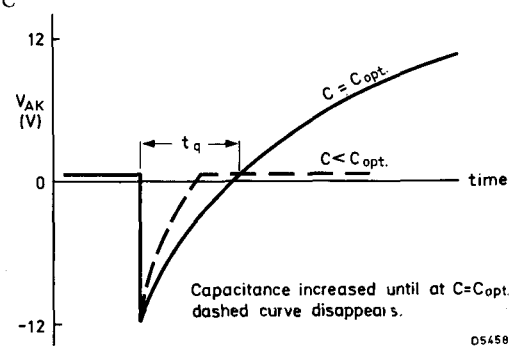
t_q Turn-off time

$R_{GkK} = 1.0k\Omega$ <5.0 μs

$R_{GkK} = 10k\Omega$ <8.0 μs

$R_{GkK} = 10k\Omega$, $T_j = 125^oC$

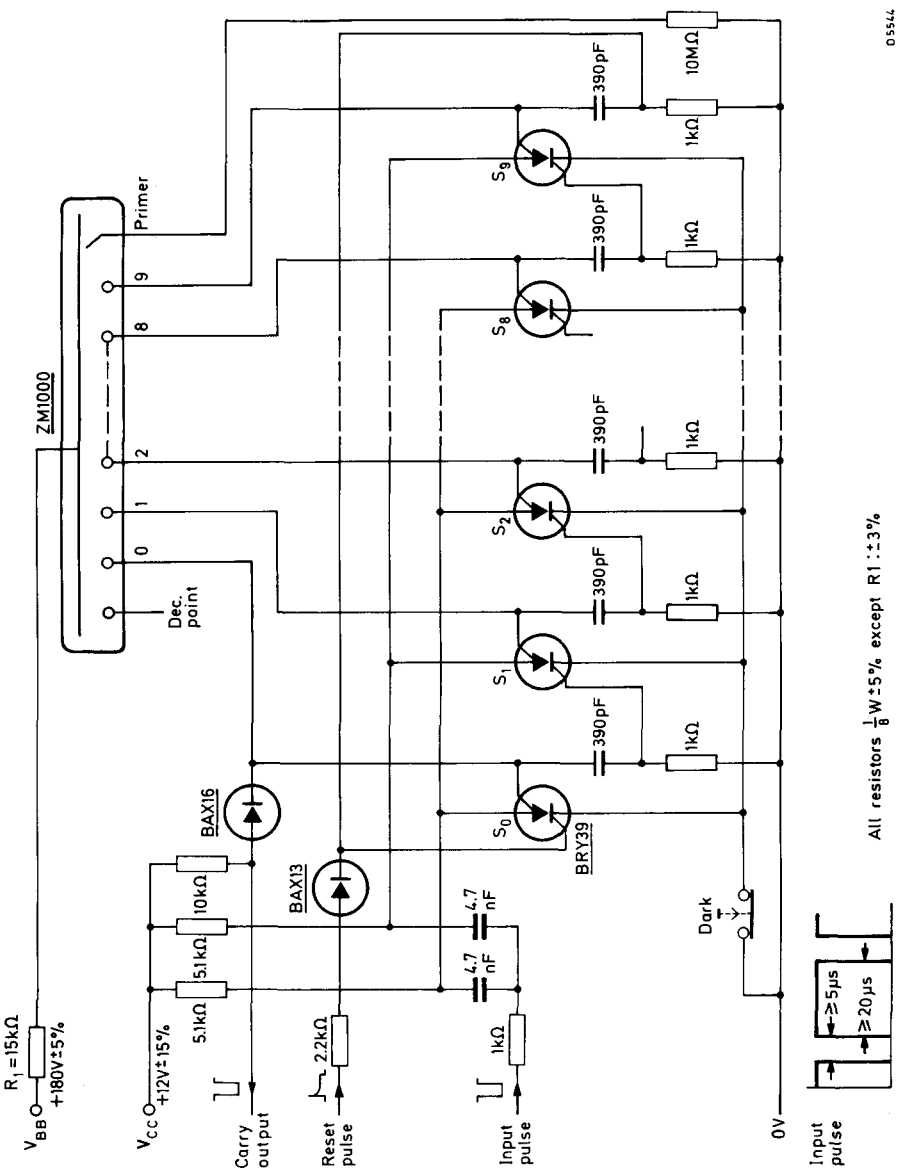


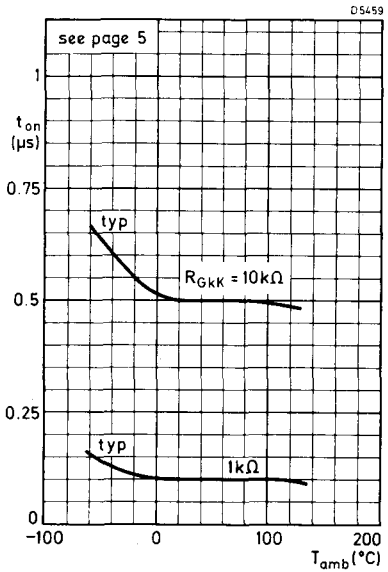


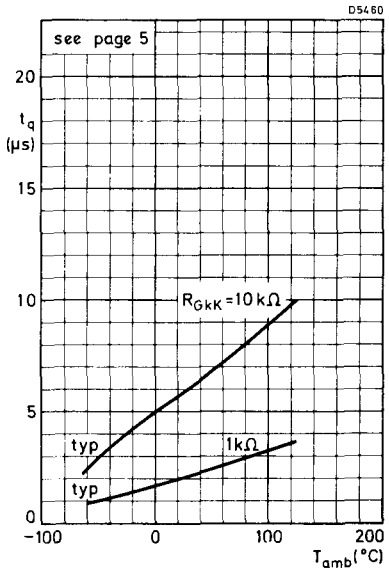
APPLICATION INFORMATION

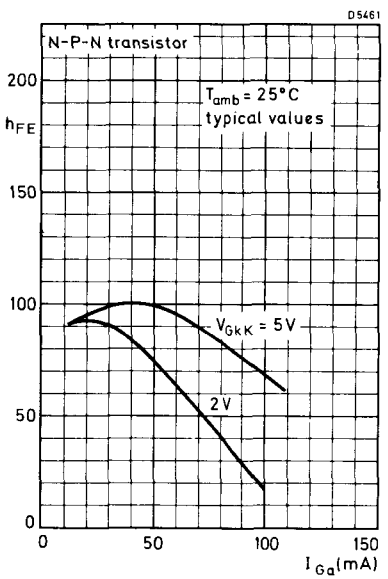
Decade ring counter circuit with display (f ≤ 40kHz)

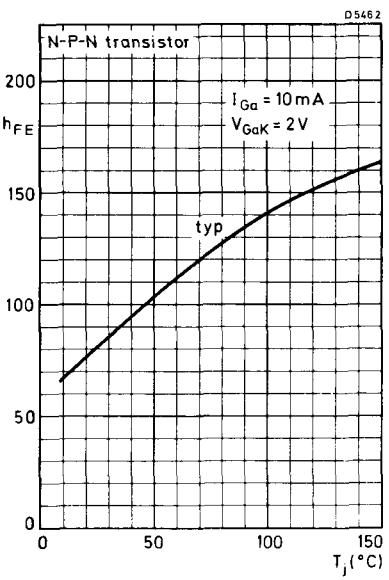
Operating ambient temperature T_{amb} = 0 to 70°C

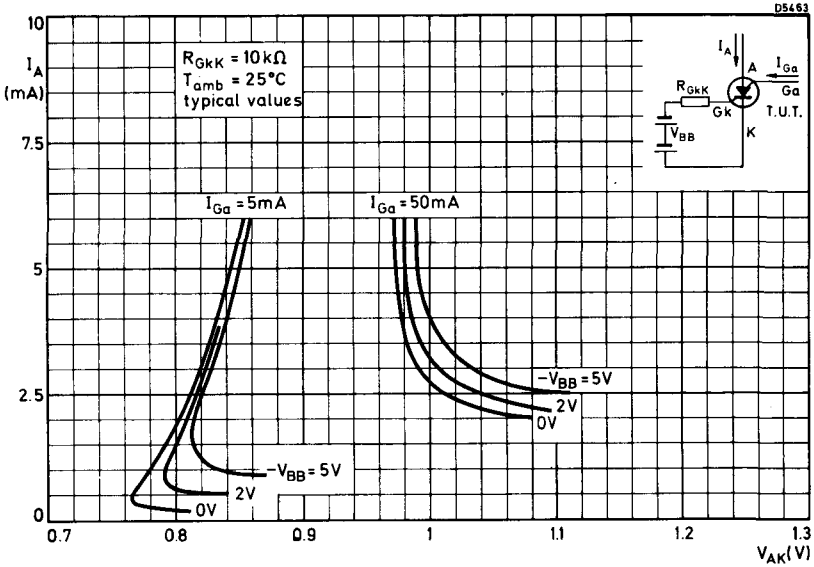


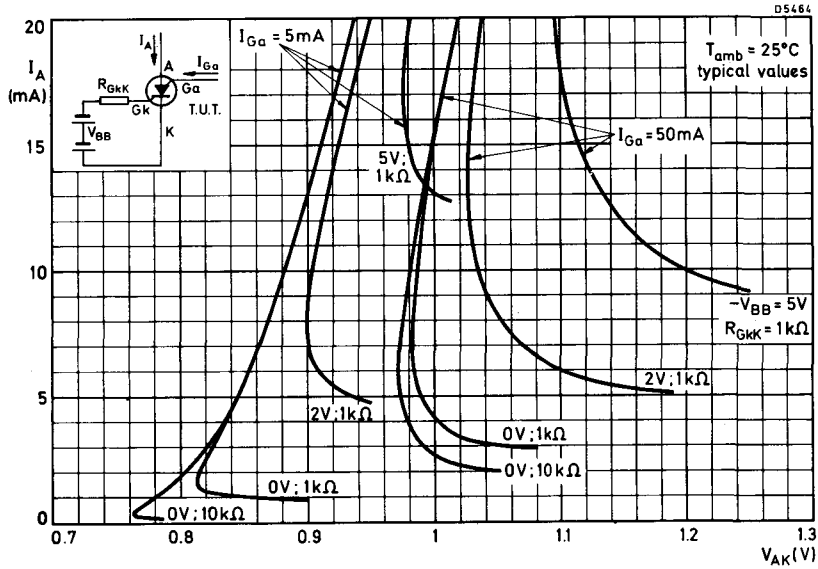

D5459
see page 5
1
0.75
0.5
0.25
0
t_{on} (µs)
typ
R_{GkK} = 10kΩ
typ
1kΩ
−100
0
100
200
T_{amb}(°C)

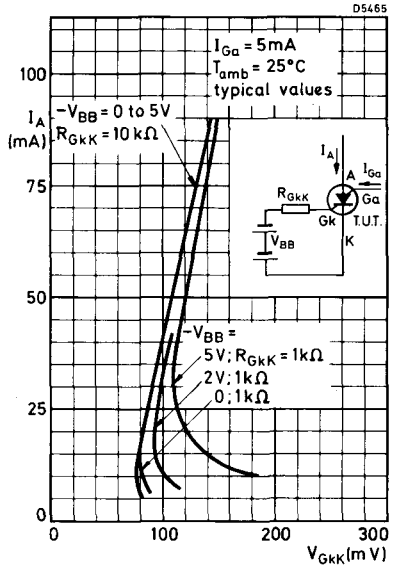

D5460
see page 5
20
15
10
5
0
t_q (µs)
R_{GkK}=10kΩ
typ
1kΩ
typ
−100
0
100
200
T_{amb}(°C)

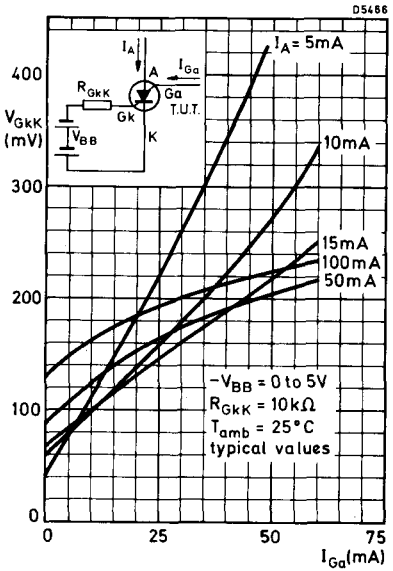

D5461
N-P-N transistor
T_{amb} = 25°C
typical values
200
150
100
50
0
h_{FE}
V_{GkK} = 5V
2V
0
50
100
150
I_{Ga}(mA)

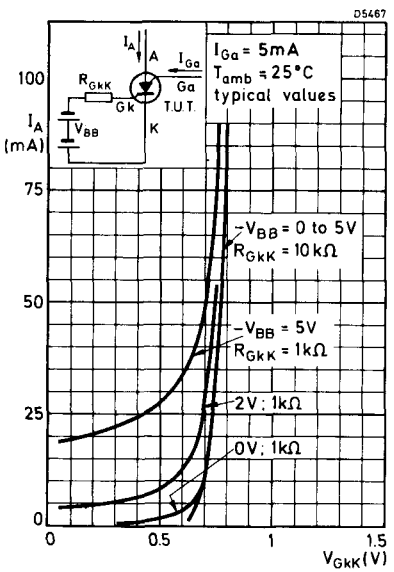

D5462
N-P-N transistor
I_{Ga} = 10mA
V_{GaK} = 2V
200
150
100
50
0
h_{FE}
typ
0
50
100
150
T_j(°C)

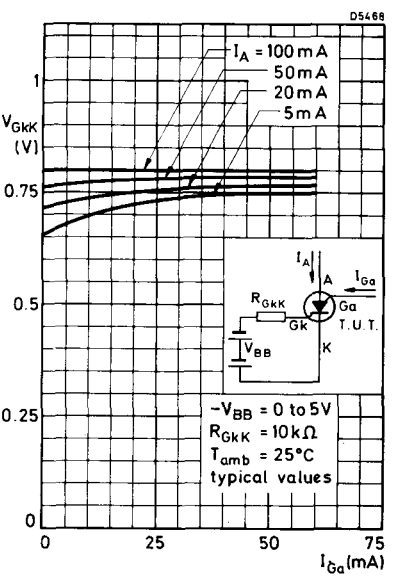

D5463
I_A (mA)
R_{GkK} = 10kΩ
T_{amb} = 25°C
typical values
I_A
A
I_{Ga}
Ga
R_{GkK}
Gk
T.U.T.
V_{BB}
K
I_{Ga} = 5mA
I_{Ga} = 50mA
$-V_{BB}$ = 5V
2V
0V
10
7.5
5
2.5
0
0.7
0.8
0.9
1
1.1
1.2
1.3
V_{AK} (V)

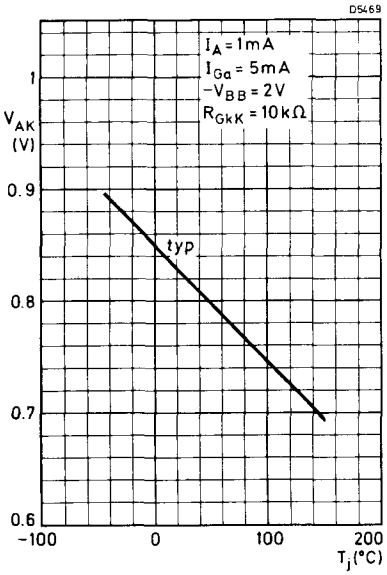

D5464
I_A (mA)
I_{Ga} = 5mA
I_{Ga} = 50mA
T_{amb} = 25°C
typical values
R_{GkK}
Gk
T.U.T.
V_{BB}
K
5V; 1kΩ
$-V_{BB}$ = 5V
R_{GkK} = 1kΩ
2V; 1kΩ
0V; 1kΩ
0V; 10kΩ
20
15
10
5
0
0.7
0.8
0.9
1
1.1
1.2
1.3
V_{AK} (V)

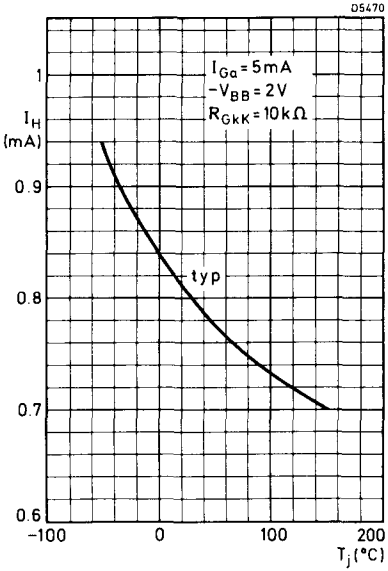

D5465
I_{Ga} = 5mA
T_{amb} = 25°C
typical values
$-V_{BB}$ = 0 to 5V
R_{GkK} = 10kΩ
$-V_{BB}$ =
5V; R_{GkK} = 1kΩ
2V; 1kΩ
0; 1kΩ
I_A (mA)
V_{GkK} (mV)
A
Ga
Gk
K
T.U.T.

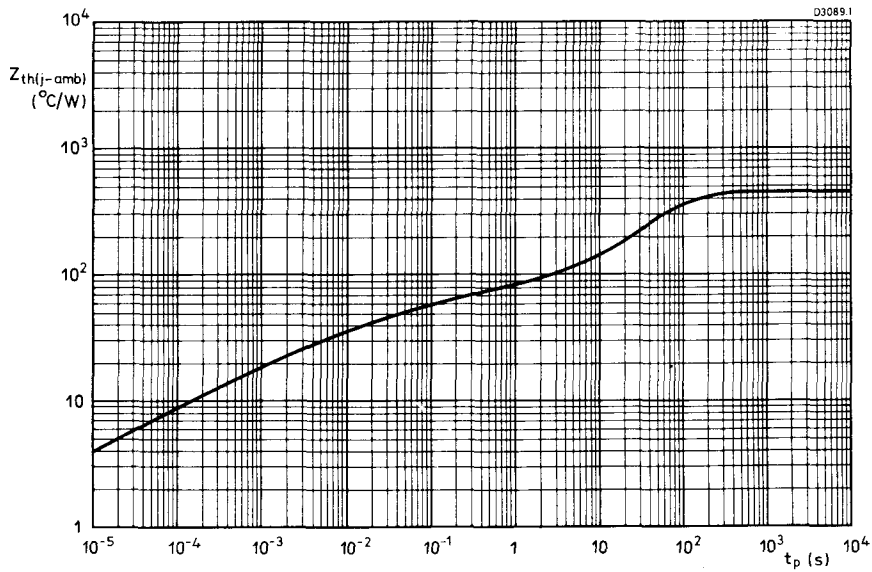

D5466
I_A = 5mA
10mA
15mA
100mA
50mA
$-V_{BB}$ = 0 to 5V
R_{GkK} = 10kΩ
T_{amb} = 25°C
typical values
V_{GkK} (mV)
I_{Ga} (mA)
A
Ga
Gk
K
T.U.T.

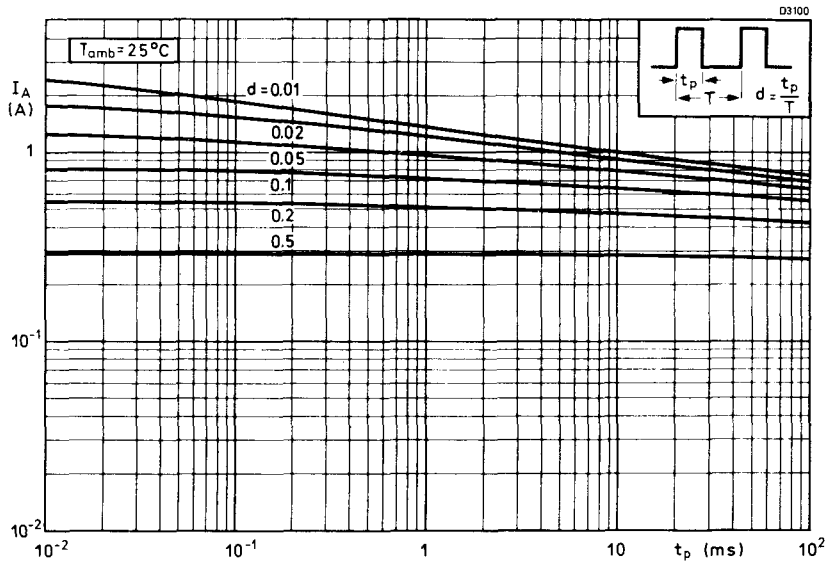

D5467
I_{Ga} = 5mA
T_{amb} = 25°C
typical values
$-V_{BB}$ = 0 to 5V
R_{GkK} = 10kΩ
$-V_{BB}$ = 5V
R_{GkK} = 1kΩ
2V; 1kΩ
0V; 1kΩ
I_A (mA)
V_{GkK} (V)
A
Ga
Gk
K
T.U.T.

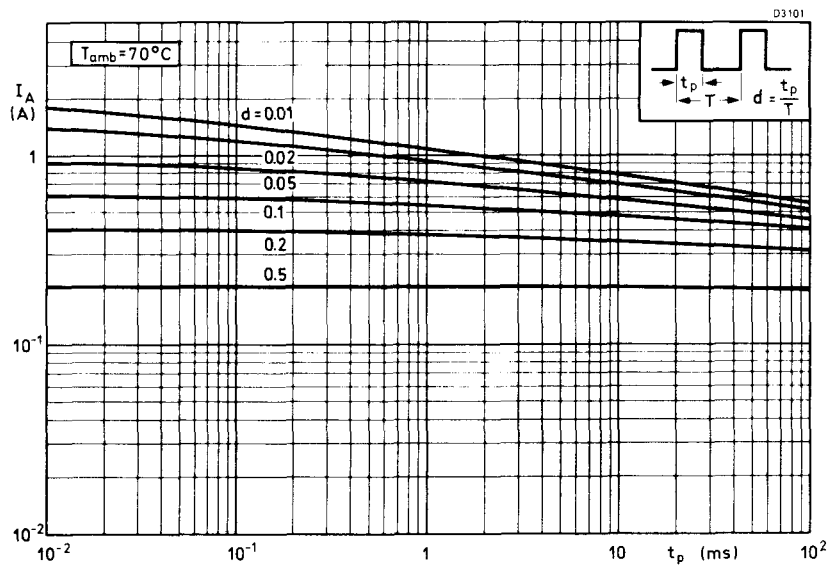

D5468
I_A = 100mA
50mA
20mA
5mA
$-V_{BB}$ = 0 to 5V
R_{GkK} = 10kΩ
T_{amb} = 25°C
typical values
V_{GkK} (V)
I_{Ga} (mA)
A
Ga
Gk
K
T.U.T.


D5469
I_A = 1mA
I_{Ga} = 5mA
$-V_{BB}$ = 2V
R_{GkK} = 10kΩ
typ
V_{AK} (V)
1
0.9
0.8
0.7
0.6
−100
0
100
200
T_j(°C)


D5470
I_{Ga} = 5mA
$-V_{BB}$ = 2V
R_{GkK} = 10kΩ
typ
I_H (mA)
1
0.9
0.8
0.7
0.6
−100
0
100
200
T_j(°C)


D3089.1
$Z_{th(j-amb)}$ (°C/W)
10^4
10^3
10^2
10
1
10^{-5}
10^{-4}
10^{-3}
10^{-2}
10^{-1}
1
10
10^2
10^3
10^4
t_p (s)


D3100
T_{amb} = 25 °C
I_A (A)
d = 0.01
0.02
0.05
0.1
0.2
0.5
1
10^{-1}
10^{-2}
10^{-2}
10^{-1}
1
10
t_p (ms)
10^2
t_p
T
$d = \frac{t_p}{T}$


D3101
T_{amb} = 70 °C
I_A (A)
d = 0.01
0.02
0.05
0.1
0.2
0.5
1
10^{-1}
10^{-2}
10^{-2}
10^{-1}
1
10
t_p (ms)
10^2
t_p
T
$d = \frac{t_p}{T}$

SILICON P-N-P-N PLANAR TRANSISTOR

BRY39

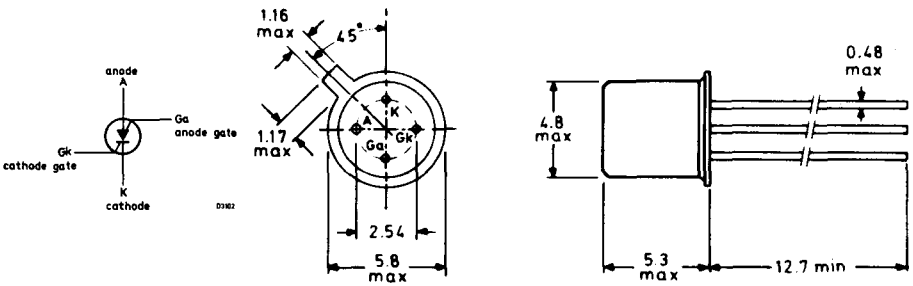
For use as a THYRISTOR TETRODE

The BRY39 is a planar p-n-p-n device in a TO-72 metal envelope, intended for use in switching applications such as relay and lamp drivers, sensing network for temperature, etc.
See also data on BRY39 as a Silicon Controlled Switch and as a Programmable Uni-junction Transistor.

QUICK REFERENCE DATA		
$V_D = V_R$ max.	70	V
$V_{DRM} = V_{RRM}$ max.	70	V
I_T max. ($T_{case} \leq 85^oC$)	250	mA
I_{TSM} max. ($t = 10\mu s$, $T_j = 150^oC$)	3.0	A
T_j max.	150	^oC
$\frac{dI_T}{dt}$ max.	20	$A/\mu s$

OUTLINE AND DIMENSIONS

Conforming to B.S. 3934 SO-12A/SB4-3
J.E.D.E.C. TO-72



All dimensions in mm

03073

Anode gate connected to case

Accessories available: 56246 (distance disc) and 56263 (cooling clip)

RATINGS

Limiting values of operation according to the absolute maximum system.

Anode to cathode

$V_D = V_R$ max.	Continuous voltage	70*	V
$V_{DRM} = V_{RRM}$ max.	Repetitive peak voltage	70*	V
$V_{DSM} = V_{RSM}$ max.	Non-repetitive peak voltage	70*	V
I_T max.	On-state current, d.c.		
	$T_{amb} \leq 25^oC$	175	mA
	$T_{case} \leq 85^oC$	250	mA
I_{TRM} max.	Repetitive peak on-state current, $t = 10\mu s$, $d = 0.01$	2.5	A
I_{TSM} max.	Non-repetitive peak on-state current, $t = 10\mu s$, $T_j = 150^oC$ prior to surge	3.0	A
$\frac{dI_T}{dt}$ max.	Rate of rise of on-state current after triggering to $I_T = 2.5A$	20	$A/\mu s$

Cathode gate to cathode

V_{GkM} max.	Reverse peak voltage	5.0	V
I_{GkM} max.	Forward peak current	100	mA

Anode gate to anode

V_{GaM}	Reverse peak voltage	70	V
I_{GaM}	Forward peak current	100	mA

Temperature

T_{stg}	Storage temperature	-65 to +200	^oC
T_j	Junction temperature	150	^oC

THERMAL CHARACTERISTICS

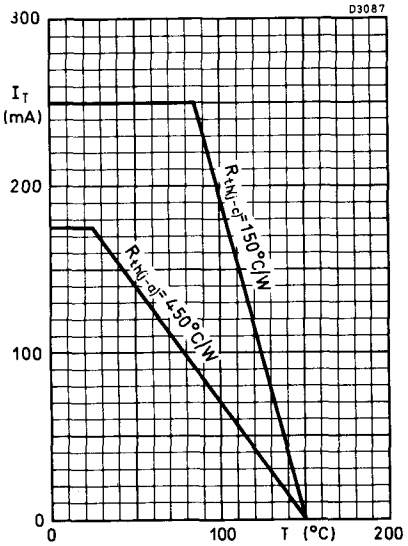
$R_{th(j\text{-}amb)}$	Thermal resistance from junction to ambient in free air	0.45	$^oC/mW$
$R_{th(j\text{-}case)}$	Thermal resistance from junction to case	0.15	$^oC/mW$

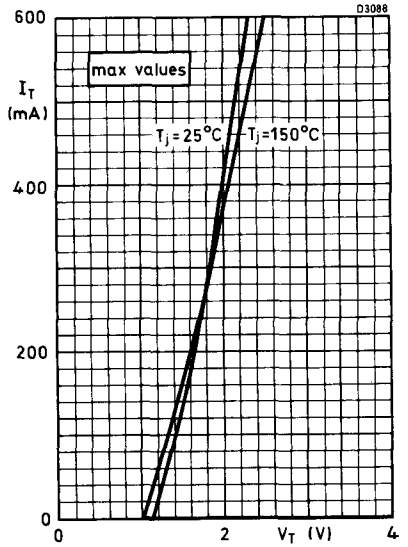
*These ratings apply for zero or negative bias on the cathode gate with respect to the cathode, and when a resistor $R \leq 10k\Omega$ is connected between cathode gate and cathode.

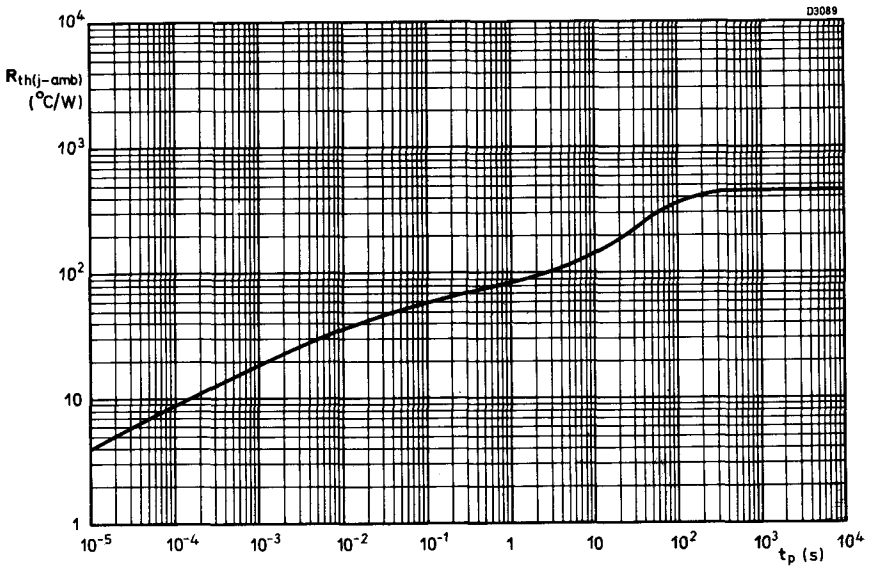
ELECTRICAL CHARACTERISTICS ($T_j = 25^oC$ unless otherwise stated)

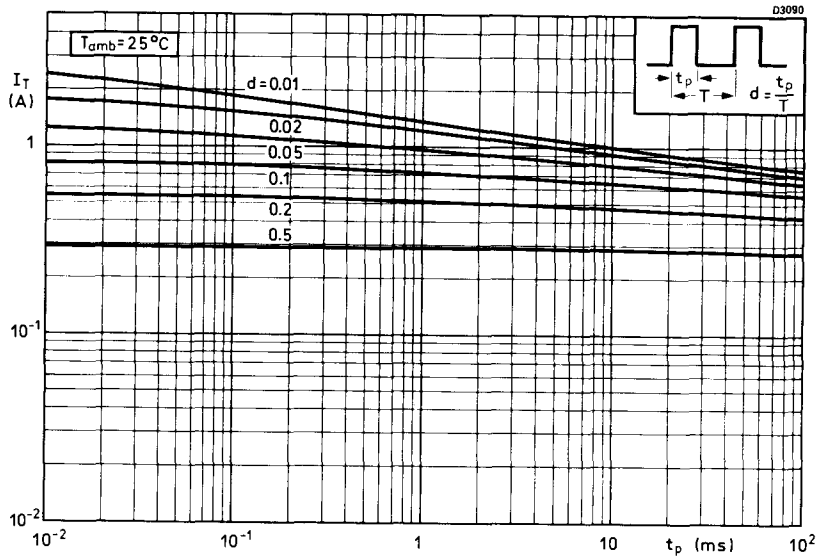
		Min.	Typ.	Max.	
Anode to cathode					
V_T	On-state voltage $I_T = 100mA$	-	-	1.4	V
$\frac{dV_D}{dt}$	Rate of rise of off-state voltage that will not trigger any device			See note below	
I_{RM}	Peak reverse current $V_{RM} = 70V$	-	1.0	100	nA
	$V_{RM} = 70V$, $T_j = 150^oC$	-	-	2.0	μA
I_{DM}	Peak off-state current $V_{DM} = 70V$	-	1.0	100	nA
	$V_{DM} = 70V$, $T_j = 150^oC$	-	-	2.0	μA
I_H	Holding current $R_{GkK} = 10k\Omega$, $R_{GaA} = 220k\Omega$	-	-	250	μA
Cathode gate to cathode					
V_{GkT}	Voltage that will trigger all devices $V_D = 6V$	0.5	-	-	V
I_{GkT}	Current that will trigger all devices $V_D = 6V$	1.0	-	-	μA
Anode gate to anode					
V_{GaT}	Voltage that will trigger all devices $V_D = 6V$	1.0	-	-	V
I_{GaT}	Current that will trigger all devices $V_D = 6V$, $R_{GkK} = 10k\Omega$	100	-	-	μA
Switching characteristics					
t_{on}	Turn-on time ($t_{on} = t_d + t_r$) $V_D = 15V$, $I_T = 150mA$, $R_{GkK} = 10k\Omega$	-	-	300	ns
t_{off}	Circuit-commutated turn-off time $V_D = V_R = 15V$, $I_T = 150mA$, $R_{GkK} = 10k\Omega$	-	-	3.0	μs

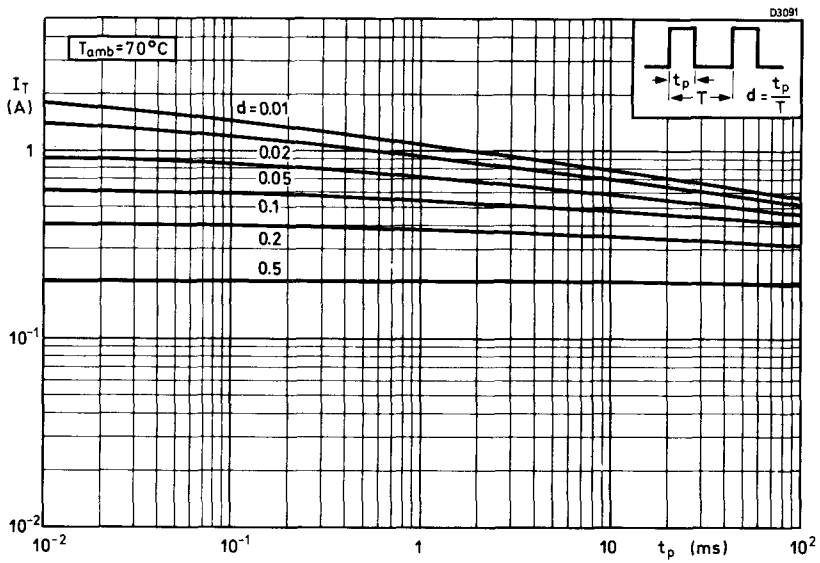
Note: - The dV_D/dt is unlimited when the anode gate lead is returned to the anode supply voltage through a current limiting resistor.

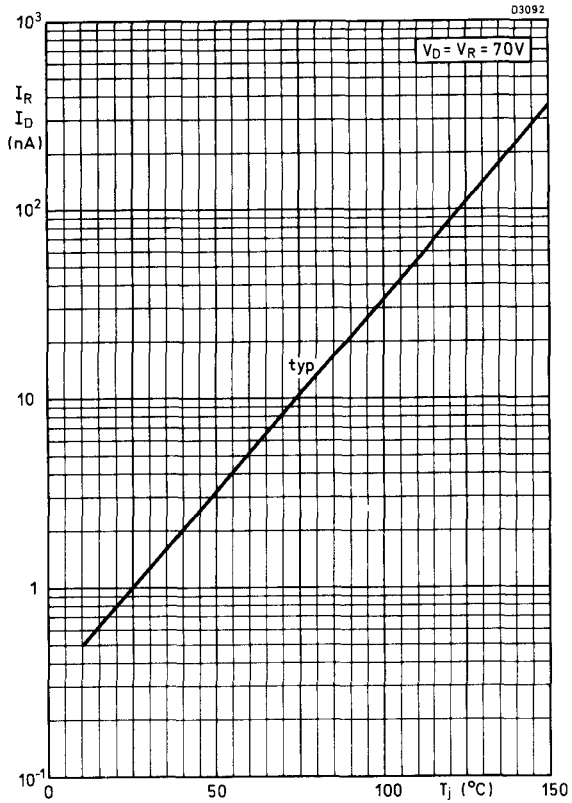

D3087
300
I_T (mA)
200
100
0
0
100
T (°C)
200
$R_{th(j-c)}$=150°C/W
$R_{th(j-c)}$=450°C/W


D3088
600
I_T (mA)
400
200
0
max values
T_j=25°C
T_j=150°C
0
2
V_T (V)
4


D3089
10^4
$R_{th(j-amb)}$ (°C/W)
10^3
10^2
10
1
10^{-5}
10^{-4}
10^{-3}
10^{-2}
10^{-1}
1
10
10^2
10^3
10^4
t_p (s)

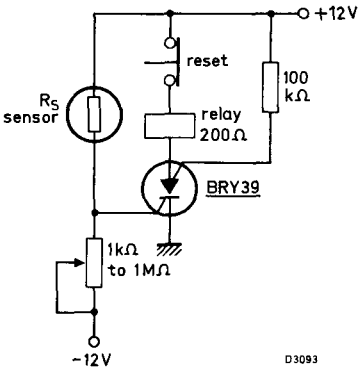

D3090
T_{amb}=25°C
I_T (A)
1
10^{-1}
10^{-2}
d=0.01
0.02
0.05
0.1
0.2
0.5
t_p
T
$d=\frac{t_p}{T}$
10^{-2}
10^{-1}
1
10
t_p (ms)
10^2


D3091
T_{amb}=70°C
I_T (A)
1
10^{-1}
10^{-2}
d=0.01
0.02
0.05
0.1
0.2
0.5
t_p
T
$d=\frac{t_p}{T}$
10^{-2}
10^{-1}
1
10
t_p (ms)
10^2


03092
$V_D = V_R = 70V$
I_R
I_D
(nA)
10^3
10^2
10
1
10^{-1}
typ
0
50
100
T_j (°C)
150

APPLICATION INFORMATION

Sensing network



R_S must be chosen in accordance with the light, temperature, or radiation intensity to be sensed; its resistance should be of the same order as that of the potentiometer.

In the arrangement shown, a decrease in resistance of R_S triggers the thyristor, closing the relay that activates the warning system. If the positions of R_S and the potentiometer are interchanged, an increase in the resistance of R_S will trigger the thyristor.

N-P-N SILICON PLANAR EPITAXIAL TRANSISTORS

BSS40
BSS41

Silicon planar epitaxial n-p-n transistors intended for use in driving very high speed core or semiconductor memories and for similar applications.

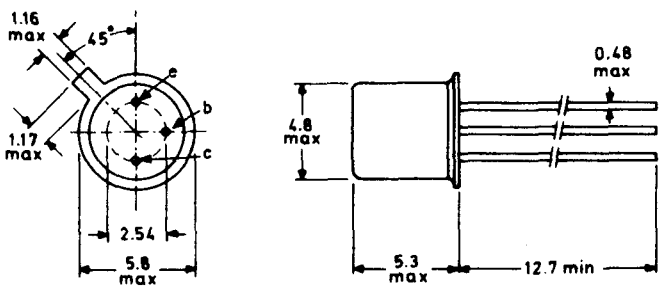
QUICK REFERENCE DATA

	BSS40	BSS41	
V_{CBO} max.	60	60	V
V_{CEO} max.	40	30	V
I_{CM} max.	1.0	1.0	A
P_{tot} max. ($T_{amb} \leq 25^{o}C$)	360	360	mW
h_{FE} min. ($I_C = 500mA$, $V_{CE} = 1V$)	25	25	
$V_{CE(sat)}$ max. ($I_C = 500mA$, $I_B = 50mA$)	0.5	0.5	V
f_T min. ($I_C = 50mA$, $V_{CE} = 10V$)	200	200	MHz
t_{on} max. ($-V_{BE(off)} = 2V$, $I_C = 500mA$, $I_{B(on)} = 50mA$)	35	35	ns
t_{off} max. ($I_C = 500mA$, $I_{B(on)} = -I_{B(off)} = 50mA$)	45	45	ns

Unless otherwise stated data are applicable to both types

OUTLINE AND DIMENSIONS

Conforming to BS3934 SO-12A/SB3-6A
J.E.D.E.C. TO-18



Collector connected to case

Accessories available: 56246, 56263

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

	BSS40	BSS41	
V_{CBO} max.	60	60	V
V_{CEO} max.	40	30	V
V_{EBO} max.	5.0		V
I_{CM} max.	1.0		A
I_{BM} max.	0.2		A
P_{tot} max., $T_{amb} \leq 25^{o}C$	360		mW

Temperature

T_{stg}	-65 to +200	^{o}C
T_j max.	200	^{o}C

THERMAL CHARACTERISTICS

$R_{th(j\text{-}amb)}$ (in free air)	480	$^{o}C/W$
$R_{th(j\text{-}case)}$	150	$^{o}C/W$

ELECTRICAL CHARACTERISTICS ($T_j = 25^{o}C$ unless otherwise stated)

			Min.	Typ.	Max.	
$V_{(BR)CBO}$	Collector-base breakdown voltage $I_C = 100\mu A$, $I_E = 0$		60	-	-	V
	Collector-emitter breakdown voltage					
$V_{(BR)CER}$	$I_C = 1.0mA$, $R_{BE} = 50\Omega$	BSS40	60	-	-	V
		BSS41	50	-	-	V
$V_{(BR)CEO}$	$I_C = 10mA$, $I_B = 0$	BSS40	40	-	-	V
		BSS41	30	-	-	V
$V_{(BR)EBO}$	Emitter-base breakdown voltage $I_E = 100\mu A$, $I_C = 0$		5.0	-	-	V
I_{CER}	Collector cut-off current $V_{CE} = 40V$, $R_{BE} = 50\Omega$		-	-	1.0	μA
	$V_{CE} = 40$, $R_{BE} = 50\Omega$, $T_j = 150^{o}C$		-	-	1.0	mA
$-I_{BEX}$	Base cut-off current $-V_{BE} = 4.0V$, $V_{CE} = 40V$	BSS40	-	-	1.0	μA
	$-V_{BE} = 4.0V$, $V_{CE} = 30V$	BSS41	-	-	1.0	μA

ELECTRICAL CHARACTERISTICS (contd.)

		Min.	Typ.	Max.	
$V_{CE(sat)}$	*Collector-emitter saturation voltage				
	$I_C = 150mA$, $I_B = 10mA$	-	-	0.3	V
	$I_C = 500mA$, $I_B = 50mA$	-	-	0.5	V
$V_{BE(sat)}$	*Base-emitter saturation voltage				
	$I_C = 150mA$, $I_B = 10mA$	-	-	1.0	V
	$I_C = 500mA$, $I_B = 50mA$	-	-	1.2	V
h_{FE}	*Static forward current transfer ratio				
	$I_C = 150mA$, $V_{CE} = 1.0V$	30	-	-	
	$I_C = 500mA$, $V_{CE} = 1.0V$	25	-	-	
f_T	Transition frequency				
	$I_C = 50mA$, $V_{CE} = 10V$, $f = 100MHz$	200	-	-	MHz
C_{Tc}	Collector capacitance				
	$I_E = I_e = 0$, $V_{CB} = 10V$, $f = 1.0MHz$	-	-	10	pF
C_{Te}	Emitter capacitance				
	$I_C = I_c = 0$, $V_{EB} = 0.5V$, $f = 1.0MHz$	-	-	50	pF

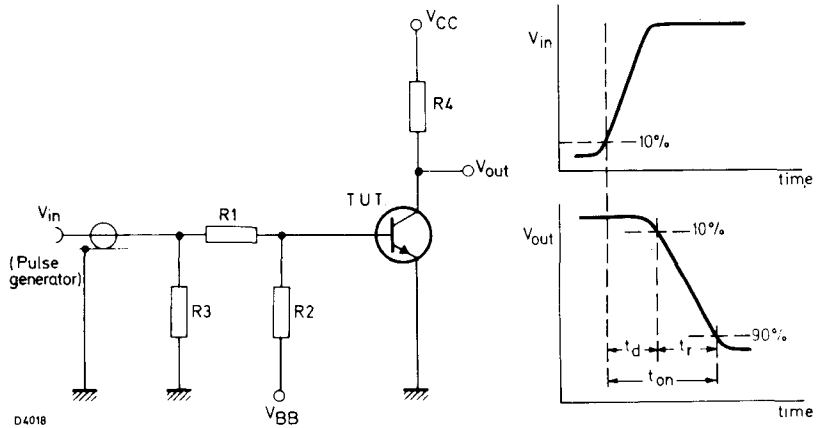
Switching characteristics (see test circuits on page 4)

t_{on}	Turn-on time when switched from				
	$-V_{BE(off)} = 2V$ to $I_C = 500mA$, $I_{B(on)} = 50mA$	-	-	35	ns
t_{off}	Turn-off time when switched from				
	$I_C = 500mA$, $I_{B(on)} = 50mA$ to cut-off				
	with $-I_{B(off)} = 1.0mA$	-	-	250	ns
	with $-I_{B(off)} = 50mA$	-	-	45	ns
t_s	Storage time when switched from				
	$I_C = 500mA$, $I_{B(on)} = 50mA$ to cut-off				
	with $-I_{B(off)} = 50mA$	10	-	-	ns

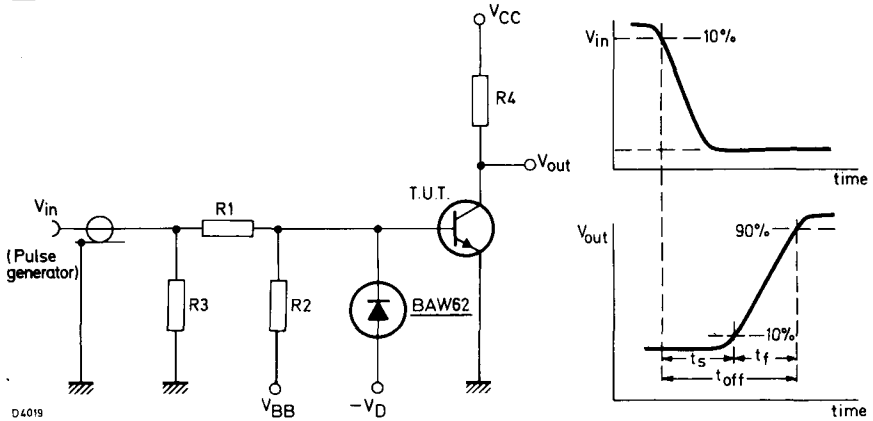
*Measured under pulsed conditions $t_p = 300\mu s$, $d = 0.01$

ELECTRICAL CHARACTERISTICS (contd.)

Turn-on time test circuit



Turn-off time test circuit

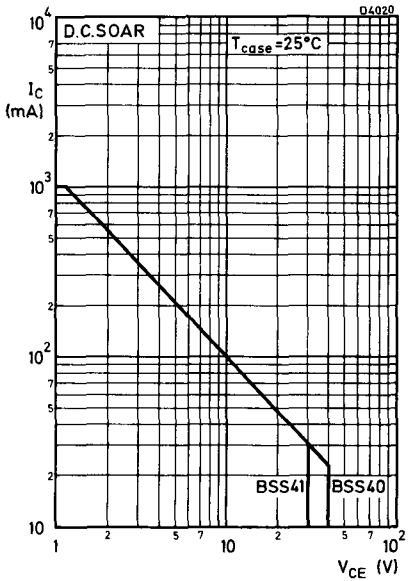


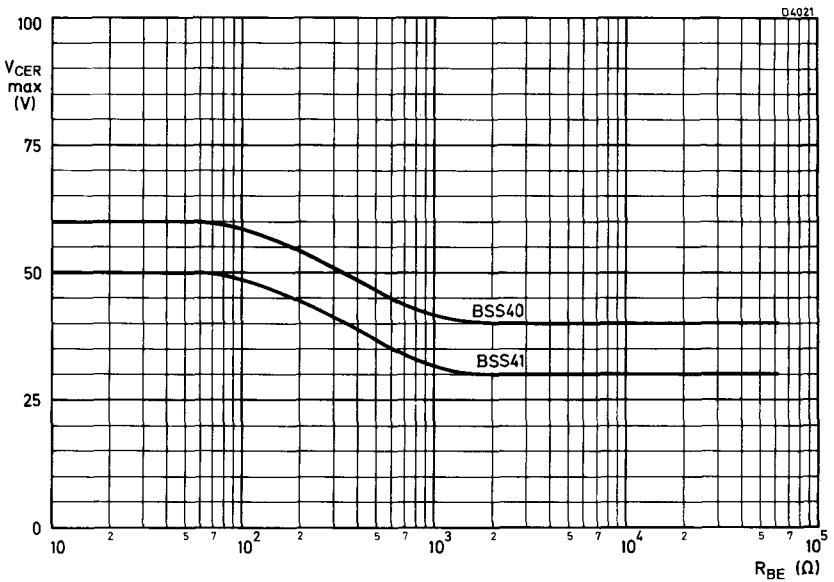
BSS40, BSS41								t_{on}		t_{off}		
I_C (mA)	$I_{B(on)}$ (mA)	$-I_{B(off)}$ (mA)	V_{CC} (V)	R_1 (Ω)	R_2 (Ω)	R_3 (Ω)	R_4 (Ω)	$-V_{BB}$ (V)	V_{in} (V)	$+V_{BB}$ (V)	V_{in} (V)	$-V_D$ (V)
500	50	50	30	375	400	56	60	4	24.75	16.7	37.5	3
500	50	1	30	750	∞	56	60				37.5	

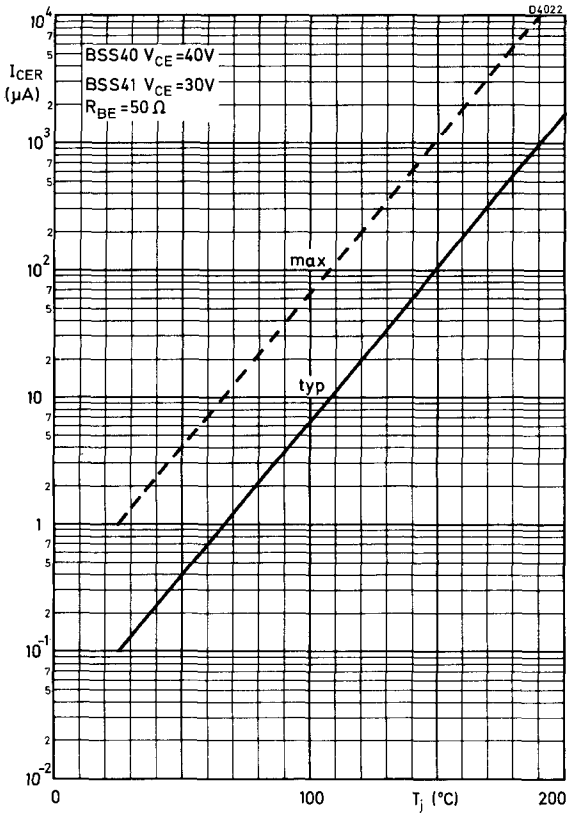
Pulse generator

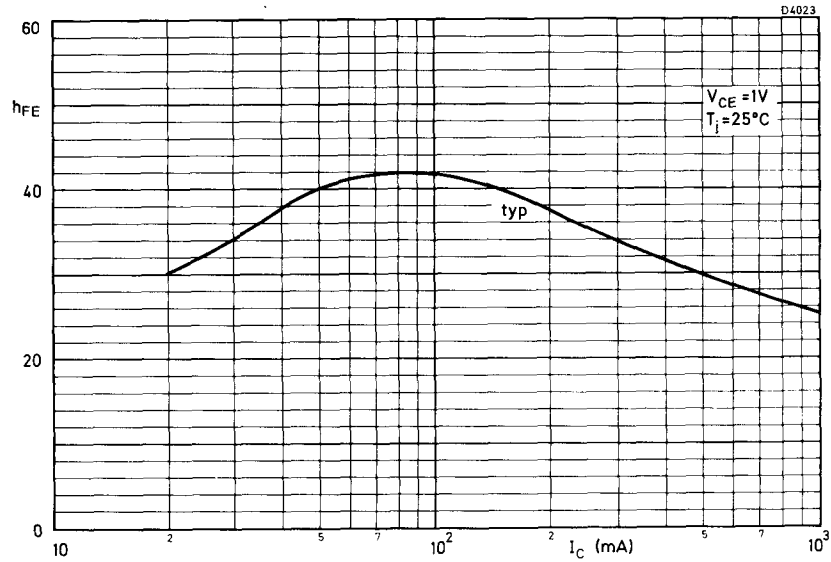
Pulse duration $t_p \geq 500ns$ Fall time $t_f \leq 5ns$

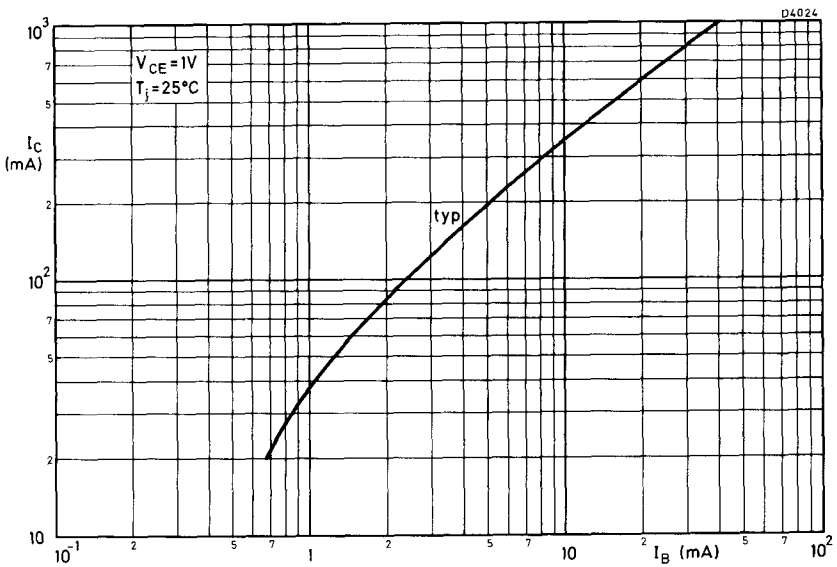
Rise time $t_r \leq 5ns$ Source impedance $R_S = 50\Omega$

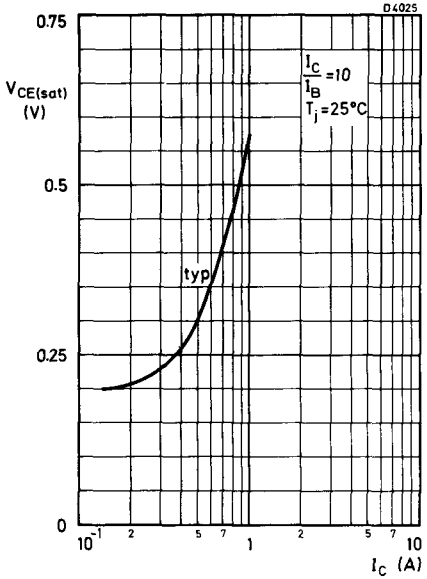

D4020
D.C.SOAR
T_{case}=25°C
I_C (mA)
BSS41
BSS40
V_{CE} (V)

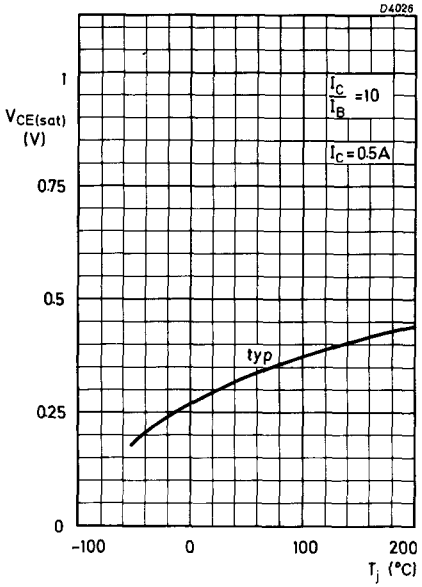

D4021
V_{CER} max (V)
BSS40
BSS41
R_{BE} (Ω)

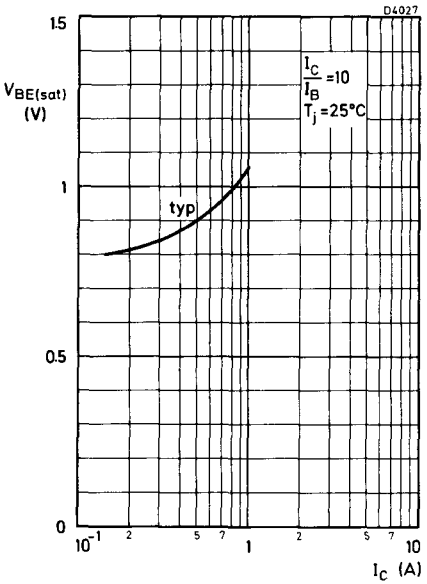

D4022
BSS40 V_{CE} =40V
BSS41 V_{CE} =30V
R_{BE} =50 Ω
I_{CER} (μA)
max
typ
T_j (°C)
0
100
200

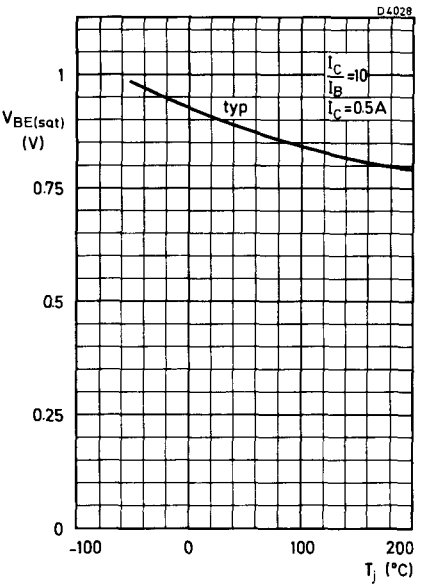

D4023
60
h_{FE}
40
20
0
V_{CE} =1V
T_j=25°C
typ
10
2
5
7
10^2
2
I_C (mA)
5
7
10^3

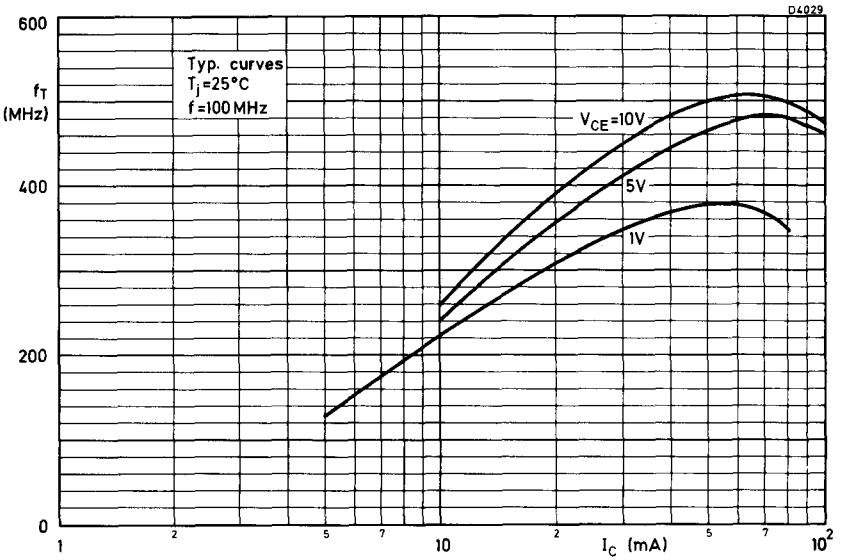

D4024
10^3
7
5
I_C
(mA)
2
10^2
7
5
2
10
V_{CE} =1V
T_j=25°C
typ
10^{-1}
2
5
7
1
2
5
7
10
2
I_B (mA)
5
7
10^2

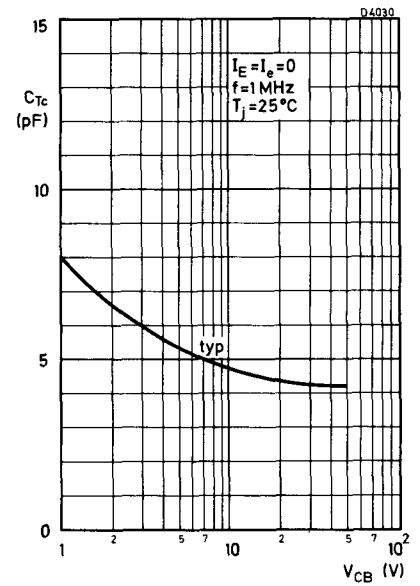

D4025
0.75
0.5
0.25
0
$V_{CE(sat)}$ (V)
$\frac{I_C}{I_B}$ =10
T_j=25°C
typ
10^{-1}
2
5
7
1
2
5
7
10
I_C (A)

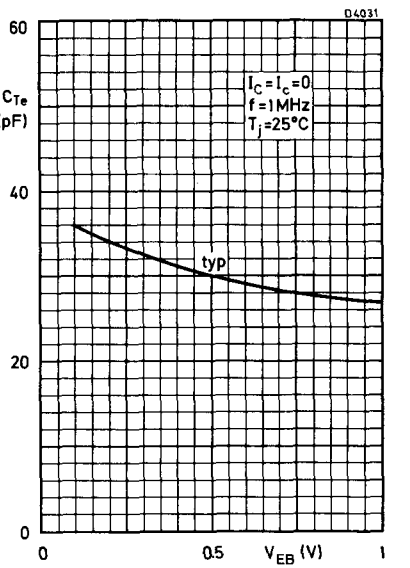

D4026
1
0.75
0.5
0.25
0
$V_{CE(sat)}$ (V)
$\frac{I_C}{I_B}$ =10
I_C=0.5A
typ
-100
0
100
200
T_j (°C)

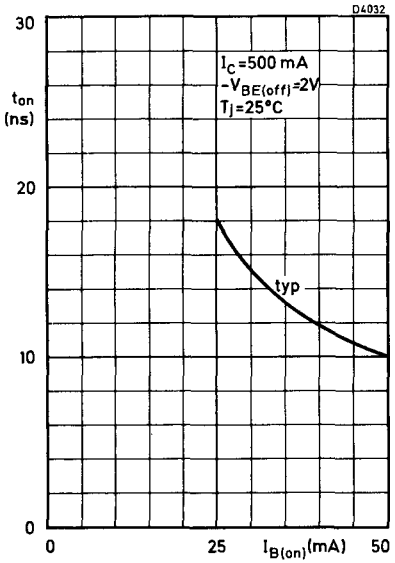

D4027
1.5
1
0.5
0
$V_{BE(sat)}$ (V)
$\frac{I_C}{I_B}$ =10
T_j=25°C
typ
10^{-1}
2
5
7
1
2
5
7
10
I_C (A)

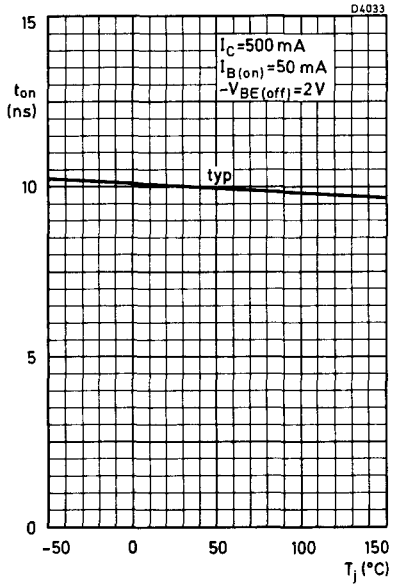

D4028
1
0.75
0.5
0.25
0
$V_{BE(sat)}$ (V)
$\frac{I_C}{I_B}$ =10
I_C=0.5A
typ
-100
0
100
200
T_j (°C)

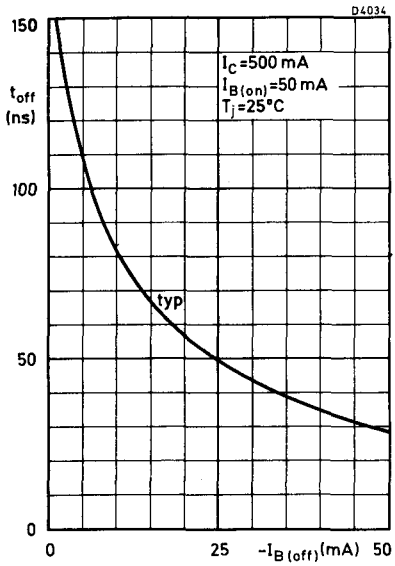

D4029
600
f_T
(MHz)
400
200
0
Typ. curves
T_j=25°C
f=100MHz
V_{CE}=10V
5V
1V
1
2
5
7
10
2
5
7
10^2
I_C (mA)

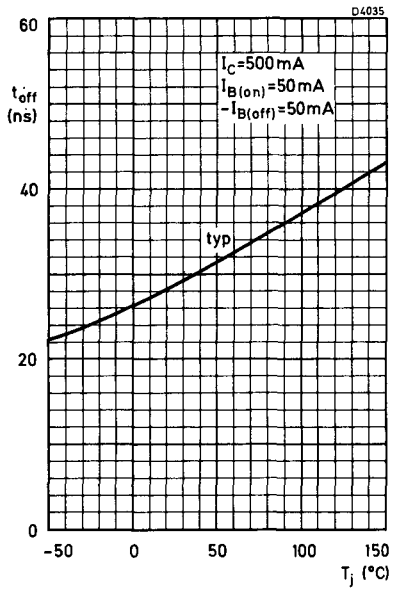

D4030
15
C_{Tc}
(pF)
10
5
0
$I_E = I_e = 0$
f=1MHz
T_j=25°C
typ
1
2
5
7
10
2
5
7
10^2
V_{CB} (V)

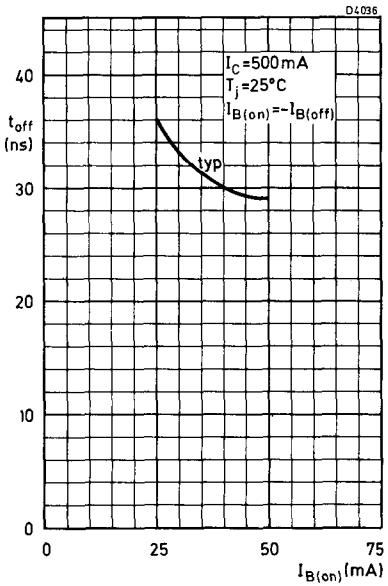

D4031
60
C_{Te}
(pF)
40
20
0
$I_C = I_c = 0$
f=1MHz
T_j=25°C
typ
0
0.5
V_{EB} (V)
1

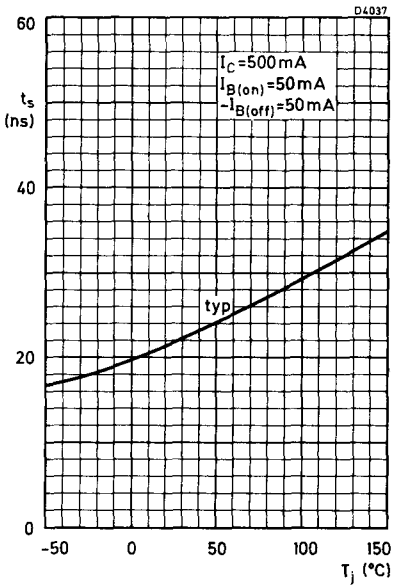

D4032
30
20
10
0
t_{on} (ns)
I_C=500 mA
$-V_{BE(off)}$=2V
T_j=25°C
typ
0
25
$I_{B(on)}$(mA)
50


D4033
15
10
5
0
t_{on} (ns)
I_C=500 mA
$I_{B(on)}$=50 mA
$-V_{BE(off)}$=2 V
typ
-50
0
50
100
150
T_j (°C)


D4034
150
100
50
0
t_{off} (ns)
I_C=500 mA
$I_{B(on)}$=50 mA
T_j=25°C
typ
0
25
$-I_{B(off)}$(mA)
50


D4035
60
40
20
0
t_{off} (ns)
I_C=500 mA
$I_{B(on)}$=50 mA
$-I_{B(off)}$=50 mA
typ
-50
0
50
100
150
T_j (°C)


D4036
I_C=500mA
T_j=25°C
$I_{B(on)}$=-$I_{B(off)}$
typ
t_{off} (ns)
40
30
20
10
0
0
25
50
75
$I_{B(on)}$(mA)


D4037
I_C=500mA
$I_{B(on)}$=50mA
-$I_{B(off)}$=50mA
typ
t_s (ns)
60
40
20
0
-50
0
50
100
150
T_j (°C)

N-P-N SILICON PLANAR DARLINGTON TRANSISTORS

BSS50
BSS51
BSS52

Silicon n-p-n planar Darlington transistors for industrial switching applications e.g. print hammer, solenoid, relay and lamp driving. Encapsulated in a TO-39 envelope with the collector connected to the can.

QUICK REFERENCE DATA

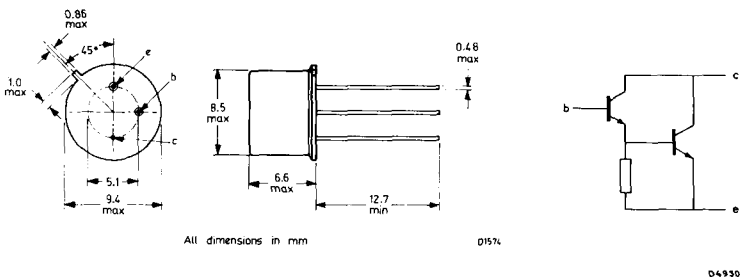
	BSS50	BSS51	BSS52	
V_{CBO} max.	60	80	100	V
V_{CE} max.	45	60	80	V
I_C max.	1.0	1.0	1.0	A
P_{tot} max. ($T_{amb} \leq 25^oC$)	0.8	0.8	0.8	W
P_{tot} max. ($T_{case} \leq 25^oC$)	5.0	5.0	5.0	W
h_{FE} min. ($I_C = 500mA$, $V_{CE} = 10V$)	1500	1500	1500	
$V_{CE(sat)}$ max. ($I_C = 1.0A$, $I_B = 1.0mA$)	-	1.6	-	V
$V_{CE(sat)}$ max. ($I_C = 1.0A$, $I_B = 4.0mA$)	1.6	-	1.6	V
t_{off} typ. ($I_C = 500mA$, $I_{B(on)} = -I_{B(off)} = 0.5mA$)	1.0	1.0	1.0	μs

Unless otherwise stated data are applicable to all types

OUTLINE AND DIMENSIONS

Conforms to BS 3934 SO-3/SB3-3B
J.E.D.E.C. TO-39

Collector connected to the envelope



Max. lead diameter is only guaranteed for 12.7mm from the can.

Accessories available: 56218, 56245, 56265

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

		BSS50	BSS51	BSS52	
V_{CBO}	max.	60	80	100	V
*V_{CE}	max.	45	60	80	V
V_{EBO}	max.	5.0	5.0	5.0	V
I_C	max.	1.0	1.0	1.0	A
I_{CM}	max. (peak value)	2.0	2.0	2.0	A
I_B	max.	0.1	0.1	0.1	A
P_{tot}	max. ($T_{amb} \leq 25^oC$)	0.8	0.8	0.8	W
	($T_{case} \leq 25^oC$)	5.0	5.0	5.0	W

Temperature

T_{stg}	range	-65 to +200	^oC
T_j	max.	200	^oC

THERMAL CHARACTERISTICS

$R_{th(j\text{-}amb)}$	220	$^oC/W$
$R_{th(j\text{-}case)}$	35	$^oC/W$

ELECTRICAL CHARACTERISTICS ($T_j = 25^oC$ unless otherwise stated)

			Min.	Typ.	Max.	
I_{CBO}	Collector cut-off current					
	$V_{CB} = 45V$, $I_E = 0$	BSS50	-	-	50	nA
	$V_{CB} = 60V$, $I_E = 0$	BSS51	-	-	50	nA
	$V_{CB} = 80V$, $I_E = 0$	BSS52	-	-	50	nA
I_{EBO}	Emitter cut-off current					
	$V_{EB} = 4.0V$, $I_C = 0$		-	-	50	nA
h_{FE}	Static forward current transfer ratio					
	$I_C = 150mA$, $V_{CE} = 10V$		1500	-	-	
	$I_C = 500mA$, $V_{CE} = 10V$		1500	-	-	

*External R_{BE} not to exceed value shown on page 5.

ELECTRICAL CHARACTERISTICS (Cont'd)

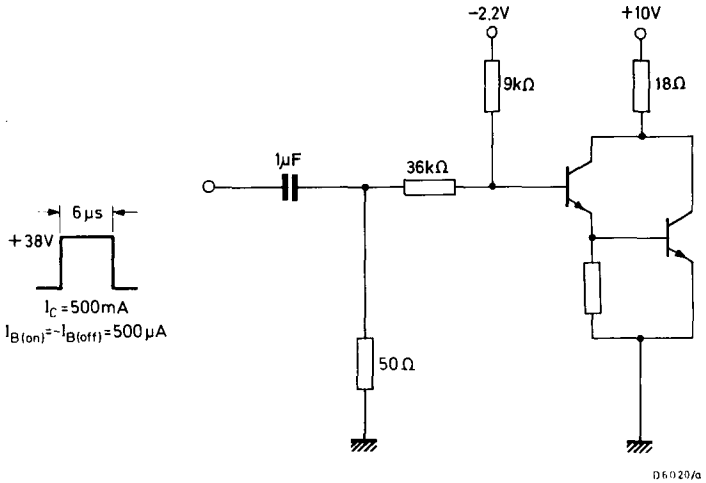
			Min.	Typ.	Max.	
$V_{CE(sat)}$	Collector-emitter saturation voltage					
	$I_C = 500mA$, $I_B = 0.5mA$		-	-	1.3	V
	$I_C = 1.0A$, $I_B = 1.0mA$	BSS51	-	-	1.6	V
	$I_C = 1.0A$, $I_B = 4.0mA$	BSS50	-	-	1.6	V
		BSS52	-	-	1.6	V
	$I_C = 500mA$, $I_B = 0.5mA$, $T_j = 200^oC$		-	-	1.3	V
	$I_C = 1.0A$, $I_B = 1.0mA$, $T_j = 200^oC$	BSS51	-	-	2.3	V
	$I_C = 1.0A$, $I_B = 4.0mA$, $T_j = 200^oC$	BSS50	-	-	1.6	V
		BSS52	-	-	1.6	V
$V_{BE(sat)}$	Base-emitter saturation voltage 1)					
	$I_C = 500mA$, $I_B = 0.5mA$		-	-	1.9	V
	$I_C = 1.0A$, $I_B = 1.0mA$	BSS51	-	-	2.2	V
	$I_C = 1.0A$, $I_B = 4.0mA$	BSS50	-	-	2.2	V
		BSS52	-	-	2.2	V
V_{BE}	Base-emitter voltage 2)					
	$I_C = 150mA$, $V_{CE} = 10V$		1.4	1.45	1.55	V
	$I_C = 500mA$, $V_{CE} = 10V$		1.5	1.55	1.65	V
h_{fe}	Small signal forward current transfer ratio					
	$I_C = 500mA$, $V_{CE} = 5.0V$, $f = 35MHz$		7.5	10	-	
Saturated switching times						
	$I_C = 500mA$, $I_{B(on)} = -I_{B(off)} = 0.5mA$					
t_{on}	Turn-on time		-	-	400	ns
t_{off}	Turn-off time		-	1.0	2.0	μs
	$I_C = 1.0A$, $I_{B(on)} = -I_{B(off)} = 1.0mA$					
t_{on}	Turn-on time		-	-	400	ns
t_{off}	Turn-off time		-	1.0	2.0	μs

Notes: 1) $V_{BE(sat)}$ decreases by about $2.5mV/^oC$ with increasing temperature.

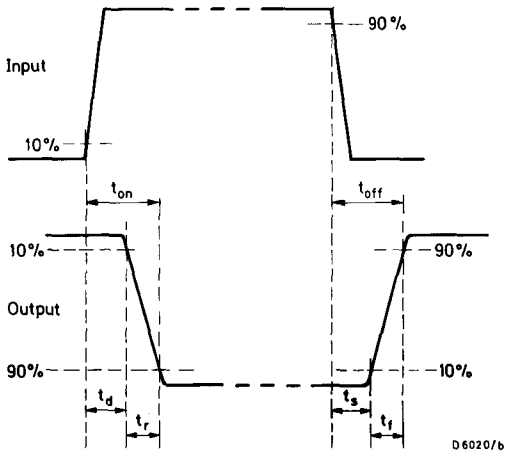
2) V_{BE} decreases by about $3.5mV/^oC$ with increasing temperature.

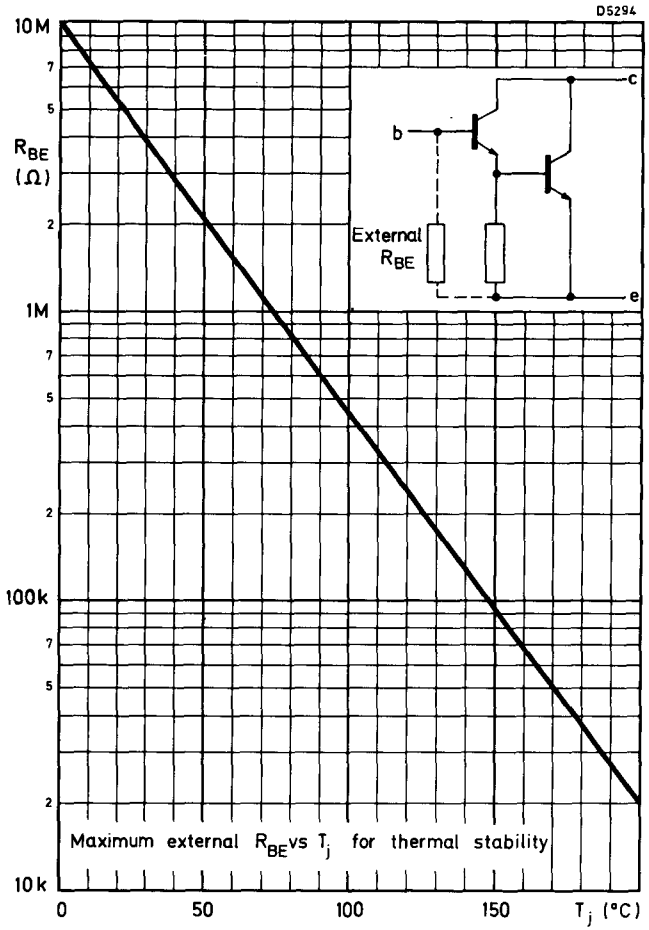
MEASUREMENT OF SATURATED SWITCHING TIMES

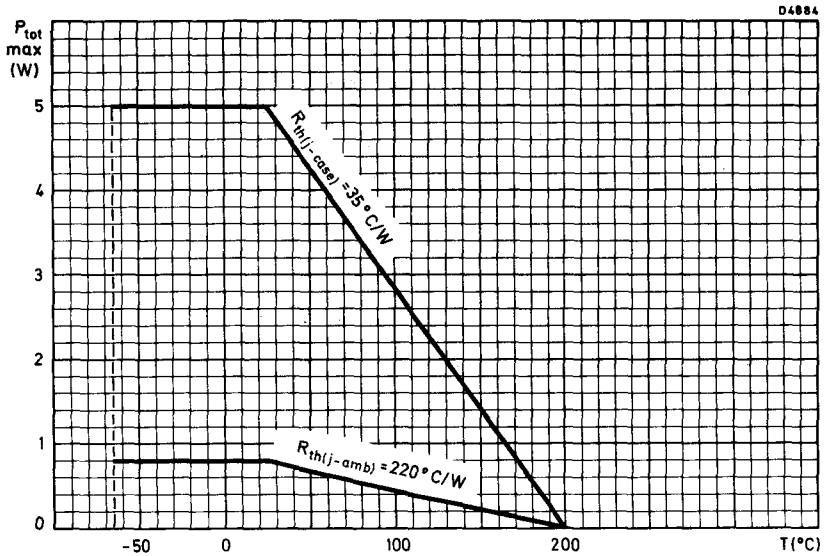
Test circuit for 500mA switching.

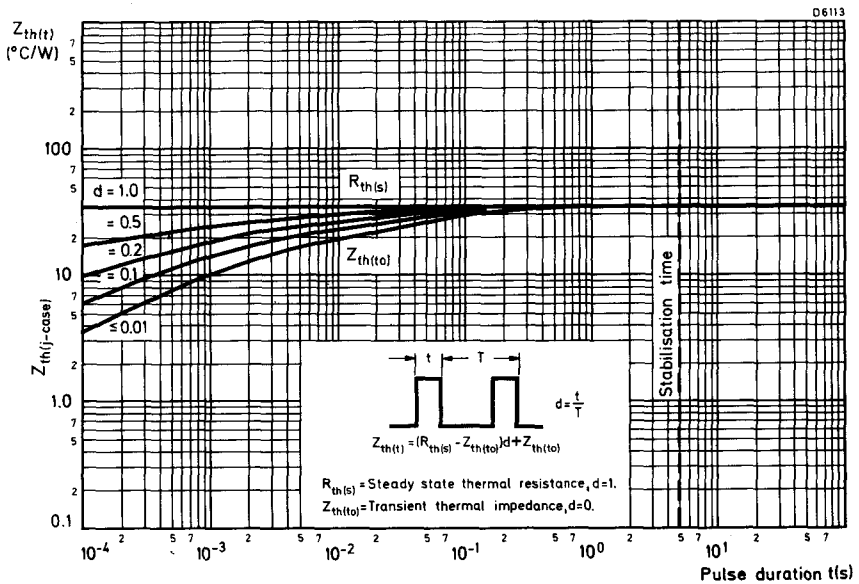


Switching waveforms



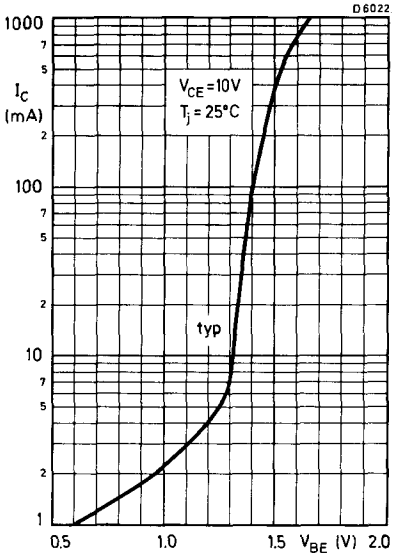

D5294
10M
7
5
R_{BE}
(Ω)
2
1M
7
5
2
100k
7
5
2
10k
0
50
100
150
T_j (°C)
b
c
e
External
R_{BE}
Maximum external R_{BE} vs T_j for thermal stability

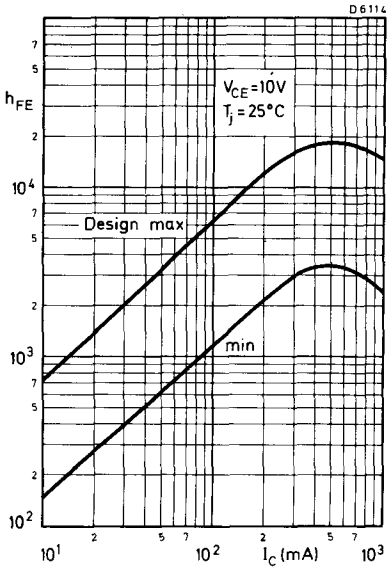

D4884
P_{tot} max (W)
5
4
3
2
1
0
$R_{th(j-case)}$ = 35 °C/W
$R_{th(j-amb)}$ = 220 °C/W
-50
0
100
200
T(°C)

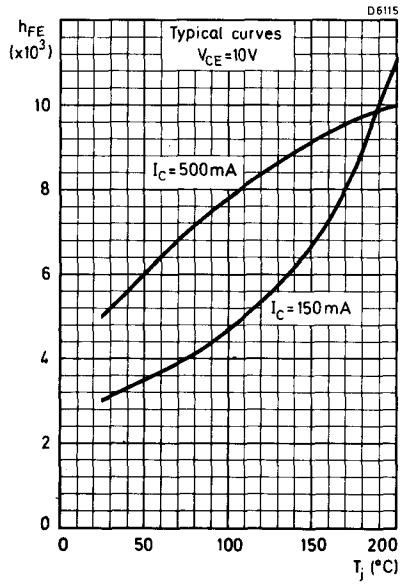

D6113
$Z_{th(t)}$ (°C/W)
100
10
1.0
0.1
$Z_{th(j-case)}$
d = 1.0
= 0.5
= 0.2
= 0.1
≤ 0.01
$R_{th(s)}$
$Z_{th(to)}$
Stabilisation time
t
T
d = t/T
$Z_{th(t)} = (R_{th(s)} - Z_{th(to)})d + Z_{th(to)}$
$R_{th(s)}$ = Steady state thermal resistance, d=1.
$Z_{th(to)}$ = Transient thermal impedance, d=0.
10^{-4}
10^{-3}
10^{-2}
10^{-1}
10^{0}
10^{1}
Pulse duration t(s)

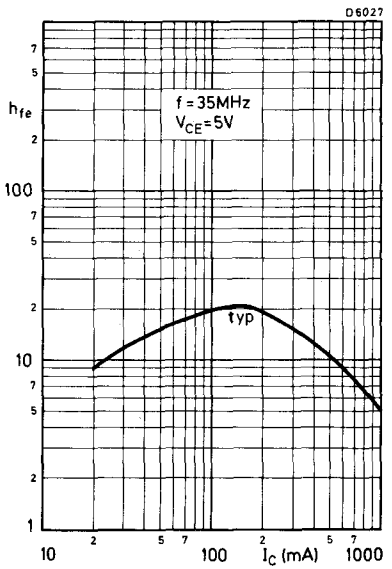
N-P-N SILICON PLANAR DARLINGTON TRANSISTORS

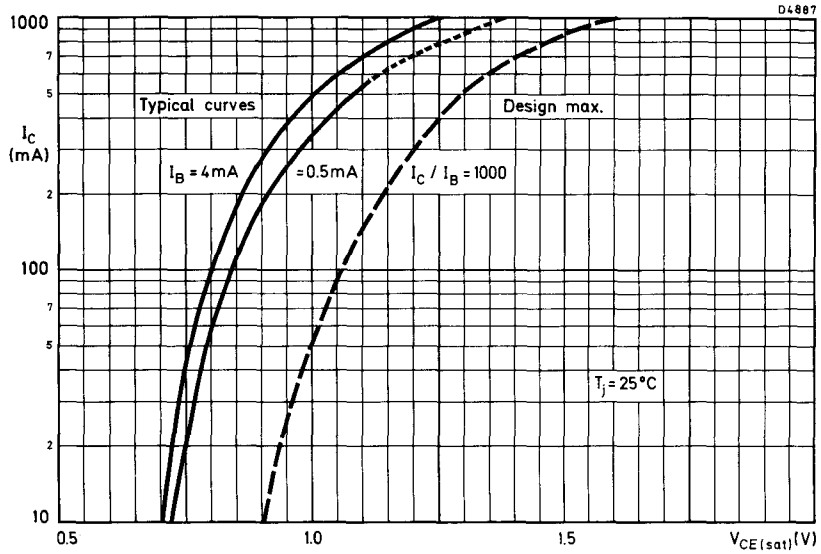
BSS50
BSS51
BSS52

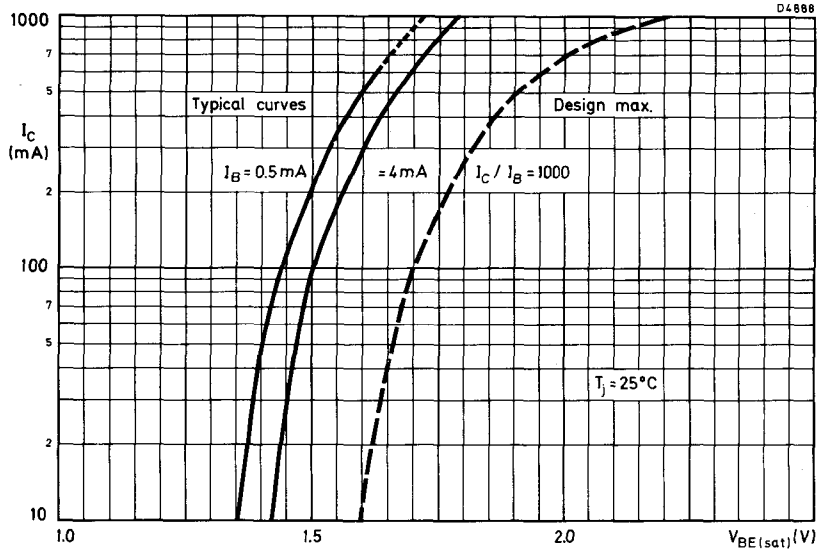









D4867
1000
7
5
2
100
7
5
2
10
I_C (mA)
Typical curves
Design max.
I_B = 4mA
=0.5mA
I_C / I_B = 1000
T_j = 25°C
0.5
1.0
1.5
$V_{CE(sat)}$(V)


D4868
1000
7
5
2
100
7
5
2
10
I_C (mA)
Typical curves
Design max.
I_B = 0.5mA
=4mA
I_C / I_B = 1000
T_j = 25°C
1.0
1.5
2.0
$V_{BE(sat)}$(V)

μ min. N-P-N SILICON PLANAR EPITAXIAL TRANSISTOR

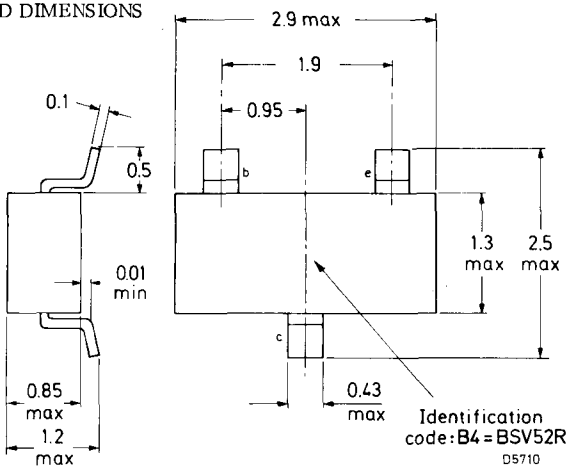
BSV52R

Silicon n-p-n planar epitaxial transistor in a microminiature plastic envelope, intended for high-speed switching in thin and thick film circuits.

QUICK REFERENCE DATA

V_{CBO}	max.		20	V
V_{CES}	max.		20	V
V_{CEO}	max.		12	V
I_{CM}	max.		200	mA
P_{tot}	max. ($T_{amb} \leq 25^{o}C$)		200	mW
T_j	max.		150	^{o}C
h_{FE} at I_C = 10mA, V_{CE} = 1V			40-120	
I_C = 50mA, V_{CE} = 1V		min.	25	
f_T at I_C = 10mA, V_{CE} = 10V, f = 100MHz		min.	400	MHz
		typ.	500	MHz
t_s	max. at $I_C = I_{B(on)} = -I_{B(off)} = 10mA$		13	ns

OUTLINE AND DIMENSIONS



All dimensions in millimetres
Plan view from above

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{CBO}	max.	20	V
V_{CES}	max.	20	V
V_{CEO}	max. (I_C = 10mA)	12	V
V_{EBO}	max.	5.0	V
I_C	max.	100	mA
I_{CM}	max.	200	mA
P_{tot}	max. $T_{amb} \leq 25^oC$, mounted on a ceramic substrate of 7 × 5 × 0.5mm	200	mW

Temperature

T_{stg}		-65 to +150	^oC
T_j	max.	150	^oC

THERMAL CHARACTERISTICS

$R_{th(j-amb)}$	Thermal resistance between junction and ambient, the device mounted on a ceramic substrate of 7 × 5 × 0.5mm	0.62	$^oC/mW$

ELECTRICAL CHARACTERISTICS (T_j = 25°C unless otherwise stated)

		Min.	Typ.	Max.	
I_{CBO}	Collector cut-off current				
	I_E = 0, V_{CB} = 10V	-	-	100	nA
	I_E = 0, V_{CB} = 10V, T_j = 125°C	-	-	5.0	μA
$V_{CE(sat)}$	Collector-emitter saturation voltage				
	I_C = 10mA, I_B = 0.3mA	-	-	300	mV
	I_C = 10mA, I_B = 1.0mA	-	-	250	mV
	I_C = 50mA, I_B = 5.0mA	-	-	400	mV
$V_{BE(sat)}$	Base-emitter saturation voltage				
	I_C = 10mA, I_B = 1.0mA	700	-	850	mV
	I_C = 50mA, I_B = 5.0mA	-	-	1.2	V
h_{FE}	Static forward current transfer ratio				
	I_C = 1.0mA, V_{CE} = 1.0V	25	-	-	
	I_C = 10mA, V_{CE} = 1.0V	40	-	120	
	I_C = 50mA, V_{CE} = 1.0V	25	-	-	
f_T	Transition frequency				
	I_C = 10mA, V_{CE} = 10V, f = 100MHz	400	500	-	MHz

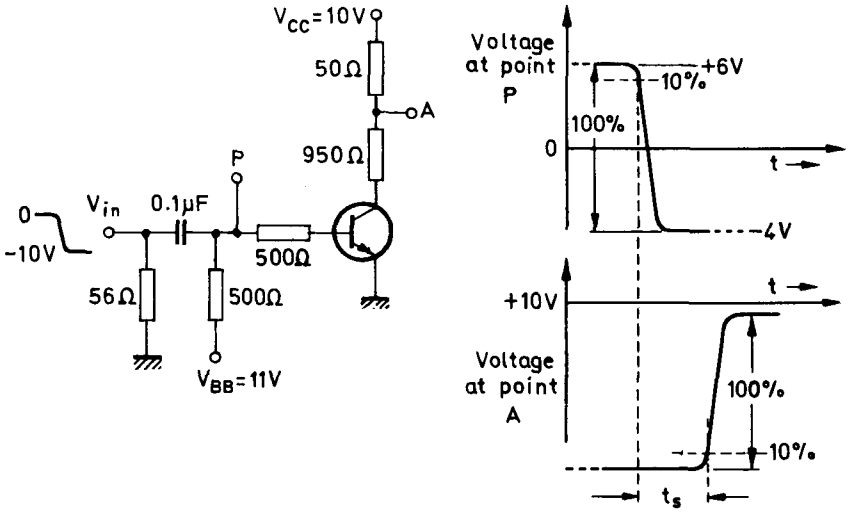
ELECTRICAL CHARACTERISTICS (contd.)

		Min.	Typ.	Max.	
C_{Tc}	Collector capacitance $I_E = I_e = 0$, $V_{CB} = 5.0V$, $f = 1.0MHz$	-	-	4.0	pF
C_{Te}	Emitter capacitance $I_C = I_c = 0$, $V_{EB} = 1.0V$, $f = 1.0MHz$	-	-	4.5	pF

SWITCHING CHARACTERISTICS

t_s	Storage time ($I_C = I_{B(on)} = -I_{B(off)} = 10mA$)	-	-	13	ns

Test circuit and waveforms



Pulse generator:

$Z_s = 50\Omega$
$t_r < 1.0ns$
$t_p > 300ns$
$d < 0.02$

Oscilloscope:

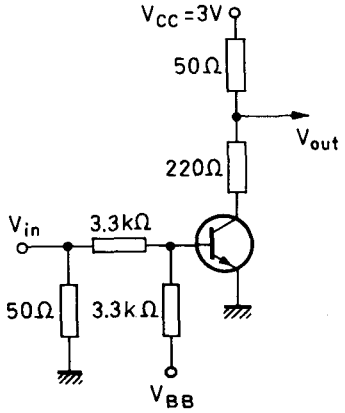
$Z_{in} = 50\Omega$
$t_r < 1.0ns$

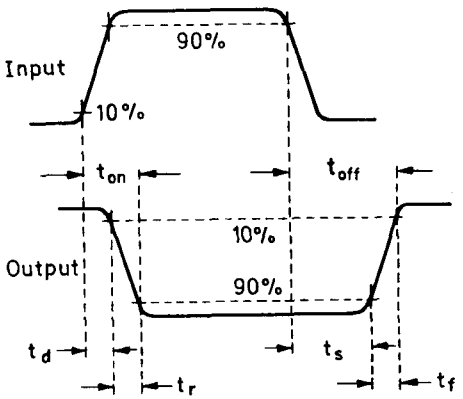
D5725

SWITCHING CHARACTERISTICS (contd.)

		Min.	Typ.	Max.	
t_{on}	Turn-on time when switched from $-V_{BE} = 1.5V$ to $I_C = 10mA$, $I_B = 3mA$, $-V_{BB} = 3V$, $V_{in} = 15V$	-	-	12	ns
t_{off}	Turn-off time when switched from $I_C = 10mA$, $I_B = 3mA$, to cut-off with $-I_{B(off)} = 1.5mA$, $V_{BB} = 12V$, $-V_{in} = 15V$	-	-	18	ns

Test circuit and waveforms

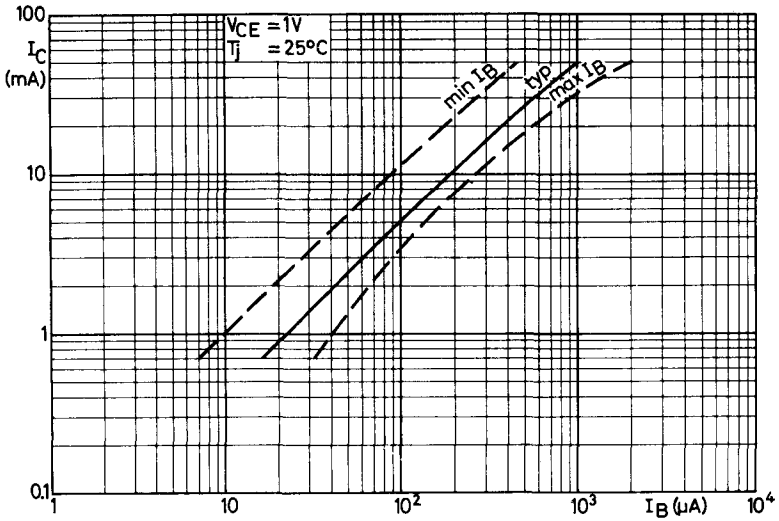


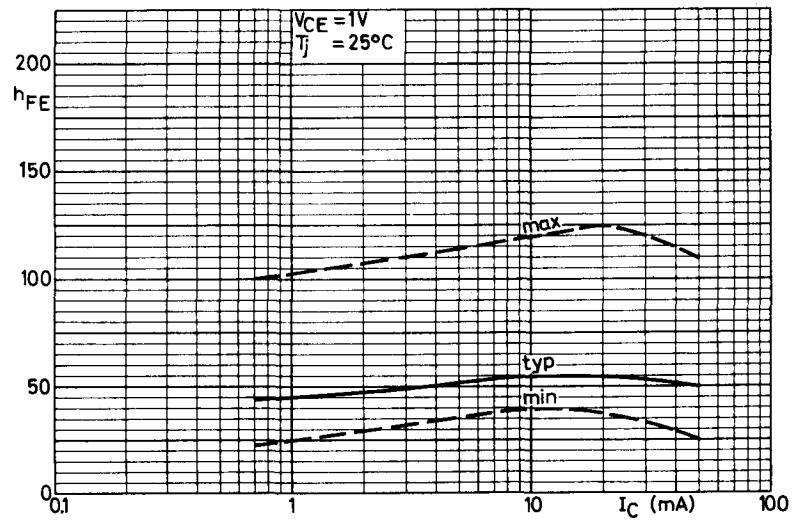


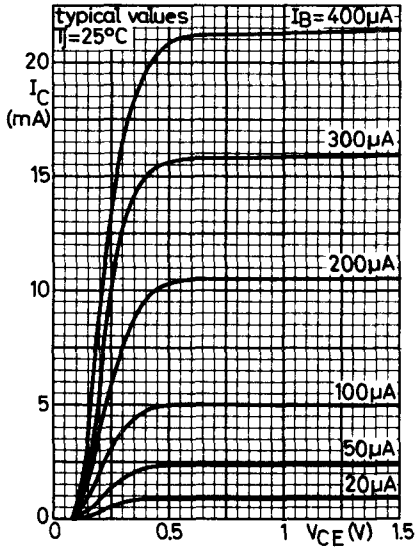
Pulse generator:
$Z_s = 50\Omega$
$t_r < 1.0ns$
$t_p > 300ns$
$d < 0.02$

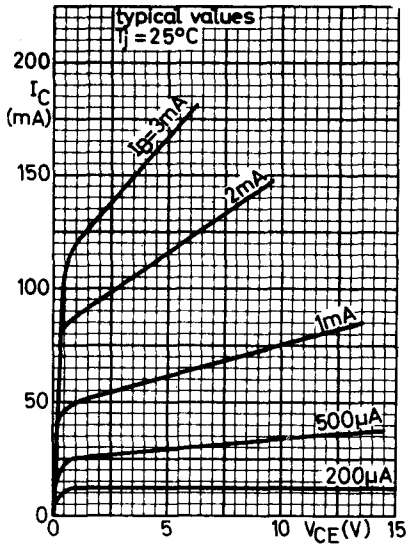
Oscilloscope:
$Z_{in} = 50\Omega$
$t_r < 1.0ns$

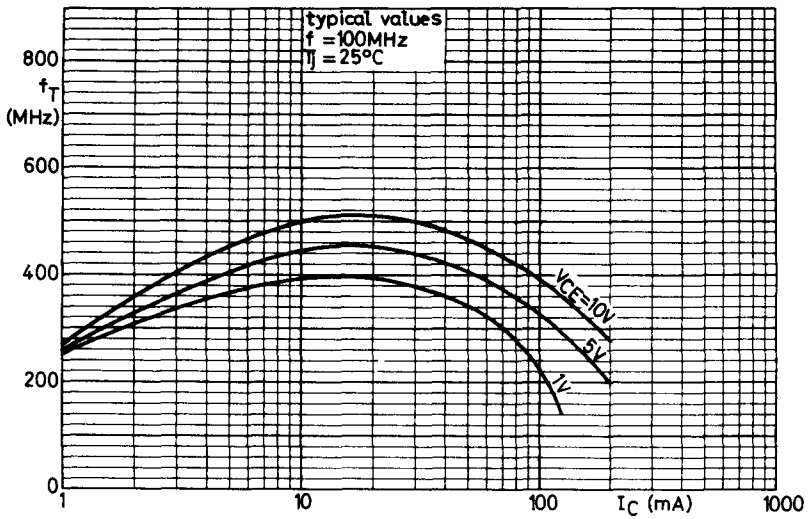
D5726

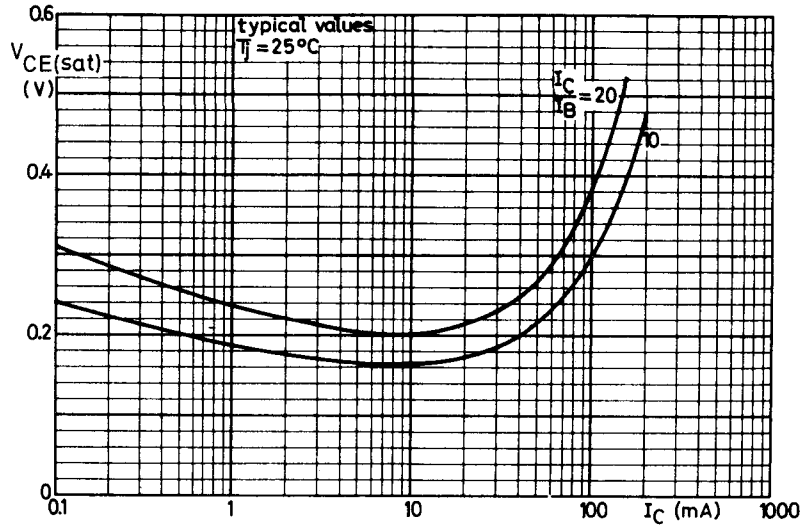

100
I_C (mA)
10
1
0.1
V_{CE} = 1V
T_j = 25°C
min I_B
typ
max I_B
1
10
10^2
10^3
I_B (μA)
10^4

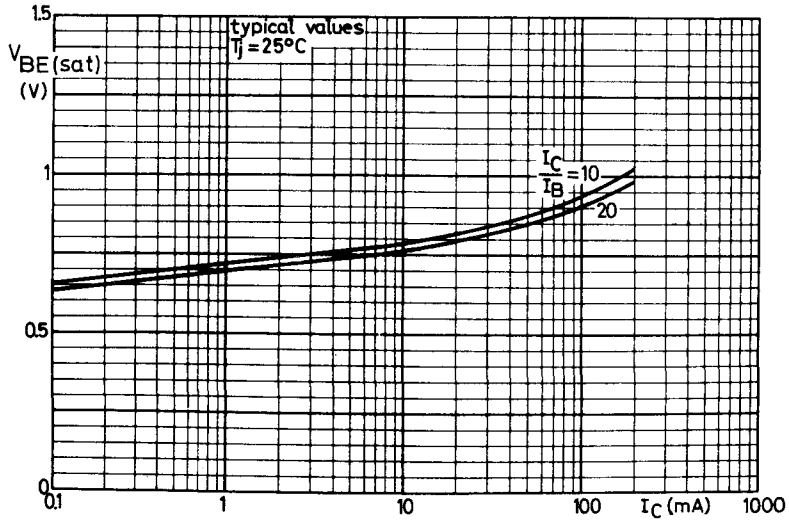

200
h_{FE}
150
100
50
0
V_{CE} = 1V
T_j = 25°C
max
typ
min
0.1
1
10
I_C (mA)
100

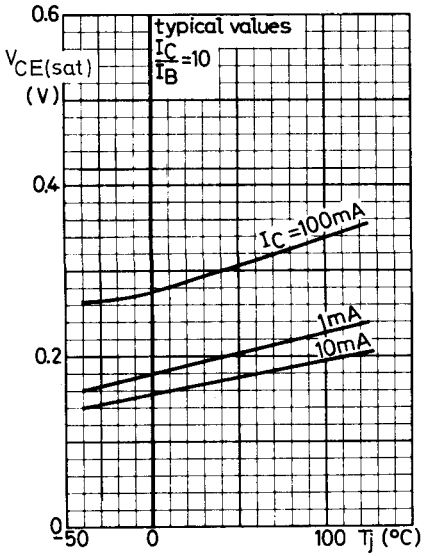

typical values
Tj=25°C
IB=400µA
300µA
200µA
100µA
50µA
20µA
IC (mA)
VCE (V)
0
0.5
1
1.5
5
10
15
20

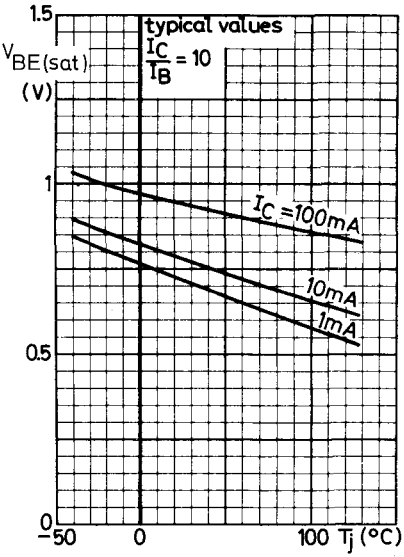

typical values
Tj = 25°C
IB=3mA
2mA
1mA
500µA
200µA
IC (mA)
VCE (V)
0
5
10
15
50
100
150
200

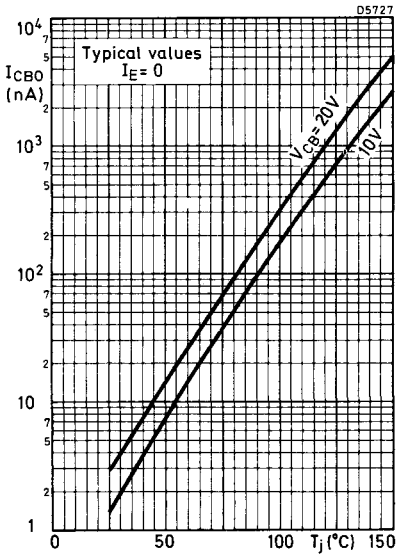

typical values
f =100MHz
Tj = 25°C
fT (MHz)
VCE=10V
5V
1V
IC (mA)
1
10
100
1000
0
200
400
600
800

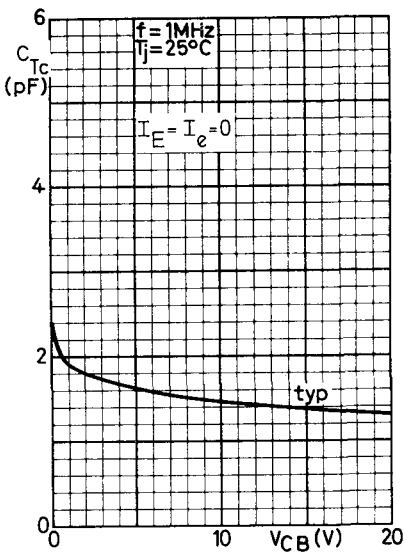

typical values
Tj = 25°C
VCE(sat) (V)
0.6
0.4
0.2
0
IC/IB = 20
10
0.1
1
10
100
IC (mA)
1000


typical values
Tj = 25°C
VBE(sat) (V)
1.5
1
0.5
0
IC/IB = 10
20
0.1
1
10
100
IC (mA)
1000


typical values
$\frac{I_C}{I_B}$=10
$V_{CE(sat)}$ (V)
0.6
0.4
0.2
0
I_C=100mA
1mA
10mA
−50
0
100
T_j (°C)


typical values
$\frac{I_C}{I_B}$ = 10
$V_{BE(sat)}$ (V)
1.5
1
0.5
0
I_C=100mA
10mA
1mA
−50
0
100
T_j (°C)


D5727
Typical values
I_E= 0
I_{CBO} (nA)
10^4
10^3
10^2
10
1
V_{CB}=20V
10V
0
50
100
T_j(°C)
150


f = 1MHz
T_j=25°C
C_{Tc} (pF)
6
4
2
0
$I_E = I_e$=0
typ
0
10
V_{CB} (V)
20

N-P-N SILICON PLANAR EPITAXIAL TRANSISTOR

BSV64

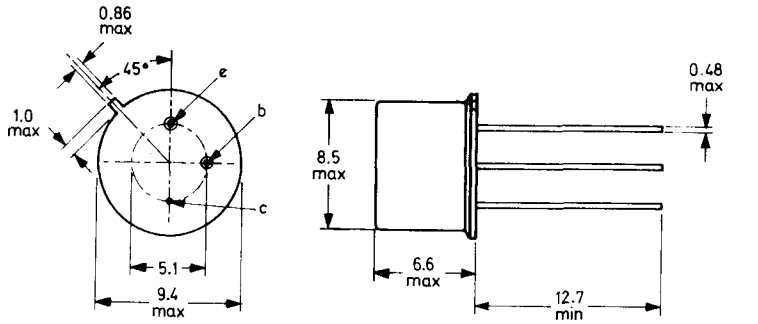
N-P-N silicon planar epitaxial transistor, with good high current saturation characteristics, primarily intended for use as a print hammer drive.

QUICK REFERENCE DATA			
V_{CBO} max.		100	V
V_{CEO} max.		60	V
I_{CM} max.		5.0	A
P_{tot} max.	($T_{case} \leq 50^{o}C$)	5.0	W
h_{FE} min.	($I_C = 2.0A$, $V_{CE} = 2.0V$)	40	
f_T typ.	($I_C = 0.5A$, $V_{CE} = 5.0V$, $f = 35MHz$, $T_{amb} = 25^{o}C$)	100	MHz
t_{off} max.	($I_C = 5.0A$, $I_{B(on)} = -I_{B(off)} = 0.5A$)	1.2	μs

OUTLINE AND DIMENSIONS

Conforms to B.S. 3934 SO-3/SB3-3A

J.E.D.E.C. TO-39



All dimensions in mm

D1574

Collector connected to case

The maximum lead diameter is guaranteed only for 12.7mm.

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{CBO} max.	100	V
V_{CER} max. ($R_B \leq 50\Omega$)	80	V
V_{CEO} max.	60	V
V_{EBO} max.	5.0	V
I_{CM} max.	5.0	A
I_C max.	2.0	A
I_B max.	1.0	A
P_{tot} max. $T_{case} \leq 50^oC$	5.0	W

Temperature

T_{stg}	-55 to +175	^oC
T_j max.	+175	^oC

THERMAL CHARACTERISTIC

$R_{th(j\text{-}case)}$ max.	25	degC/W

ELECTRICAL CHARACTERISTICS (at $T_j = 25^oC$ unless otherwise stated)

		Min.	Typ.	Max.	
I_{CBO}	Collector cut-off current $V_{CB} = 60V$, $I_E = 0$	-	-	10	μA
I_{EBO}	Emitter cut-off current $V_{EB} = 4.0V$, $I_C = 0$	-	-	10	μA
h_{FE}	Static forward current transfer ratio $I_C = 2.0A$, $V_{CE} = 2.0V$	40	-	-	
$V_{CE(sat)}$	Collector-emitter saturation voltage $I_C = 5.0A$, $I_B = 0.5A$	-	-	1.0	V
$V_{BE(sat)}$	Base-emitter saturation voltage $I_C = 5.0A$, $I_B = 0.5A$	-	-	1.8	V
C_{Tc}	Collector capacitance $V_{CB} = 10V$, $I_E = I_e = 0$, $f = 1.0MHz$	-	-	80	pF

ELECTRICAL CHARACTERISTICS (contd.)

		Min.	Typ.	Max.	
f_T	Transition frequency $I_C = 0.5A$, $V_{CE} = 5.0V$, $f = 35MHz$, $T_{amb} = 25^oC$	-	100	-	MHz
	Saturated switching times $I_C = 5.0A$, $I_{B(on)} = -I_{B(off)} = 0.5A$, $V_{BE(off)} = 2.0V$				
t_{on}	Turn-on time	-	-	0.6	μs
t_{off}	Turn-off time	-	-	1.2	μs

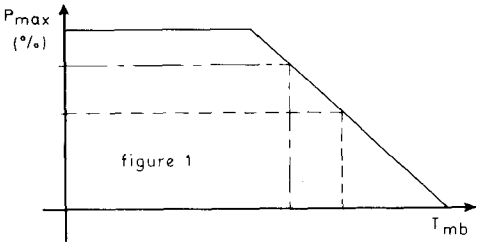
SOLDERING AND WIRING RECOMMENDATIONS

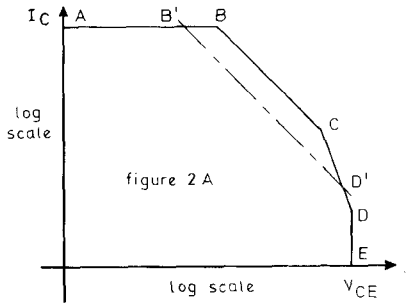
1. When using a soldering iron, transistors may be soldered directly into the circuit, but heat conducted to the junction should, if possible, be kept to a minimum by the use of a thermal shunt.
2. Transistors may be dip-soldered at a solder temperature of 245°C for a maximum soldering time of 5 seconds. The case temperature during soldering must not at any time exceed the maximum storage temperature. These recommendations apply to a transistor mounted flush on a board having punched-through holes, or spaced at least 1.5mm above a board having plated-through holes.
3. Care should be taken not to bend the leads nearer than 1.5mm from the seal.
4. If devices are stored at temperatures above 100°C before incorporation into equipment, some deterioration of the external surface is likely to occur which may make soldering into the circuit difficult. Under these circumstances the leads should be retinned using a suitable activated flux.

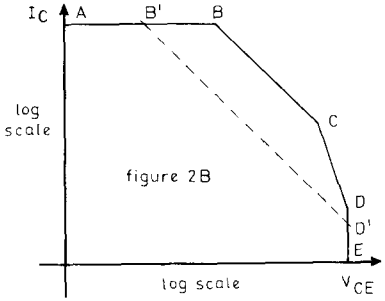
DERATING AGAINST MOUNTING-BASE TEMPERATURE

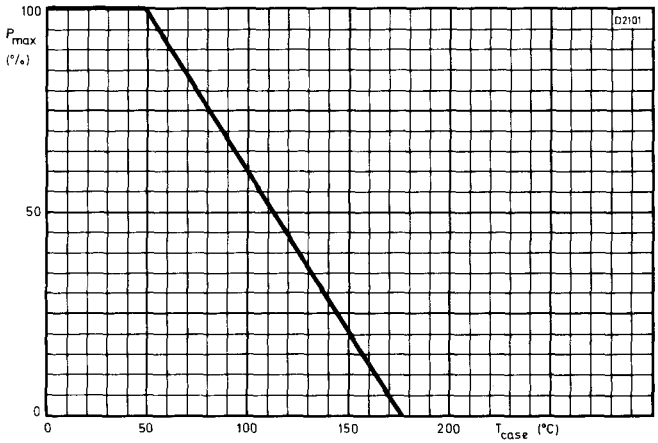
The maximum permissible power for selected pulse widths and/or mounting-base temperature can be obtained from the graphs on pages 5, 6 and 7, where the P_{max} value for $T_{mb} \leq 50^{o}C$ is calculated from the line of constant power (i.e. that part of the curve which has a slope of -1), on the relevant I_C versus V_{CE} curve.

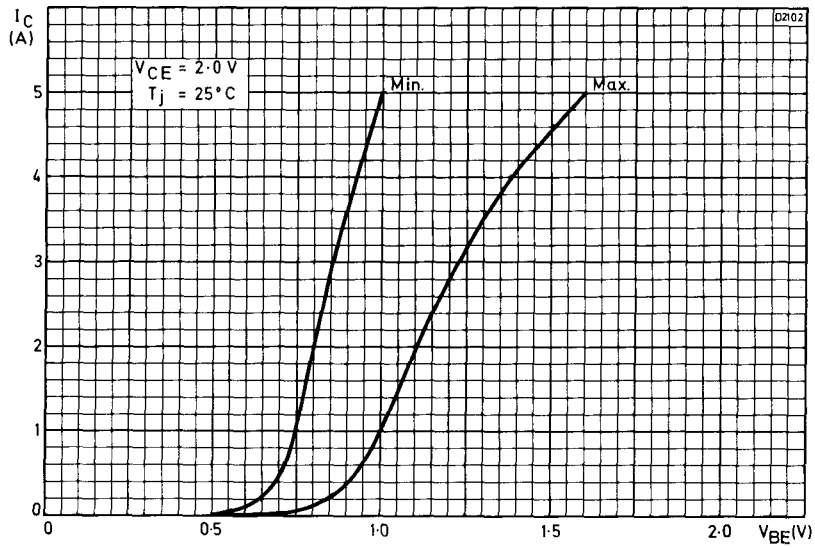
For mounting-base temperatures in excess of $50^{o}C$, the constant power line BC in figures 2A and 2B is reduced to the % of P_{max} as read from the % P_{max} versus T_{mb} graph on page 5. The safe operating area for the higher temperature is defined either by the points A B' D' D E in figure 2A, or by the points A B' D' E in figure 2B. The second-breakdown power line is only modified by the intersection point D' and is not adjusted against temperature in any other way.

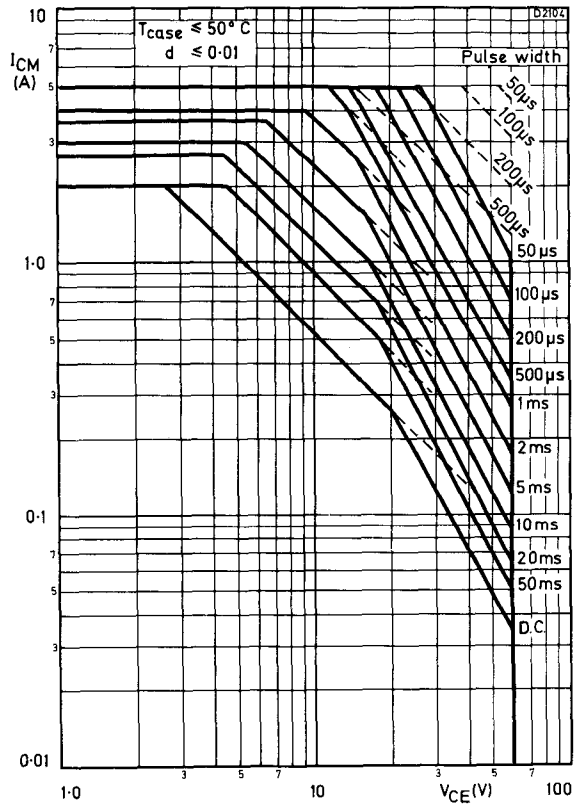


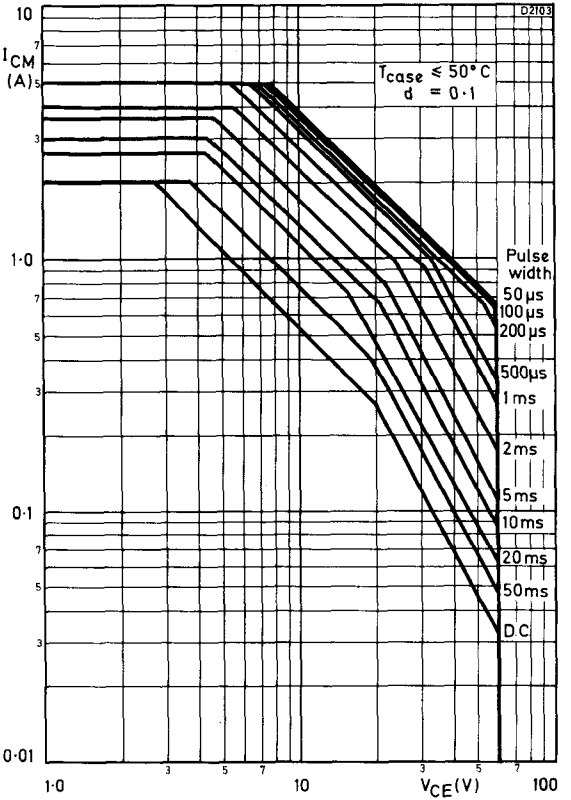


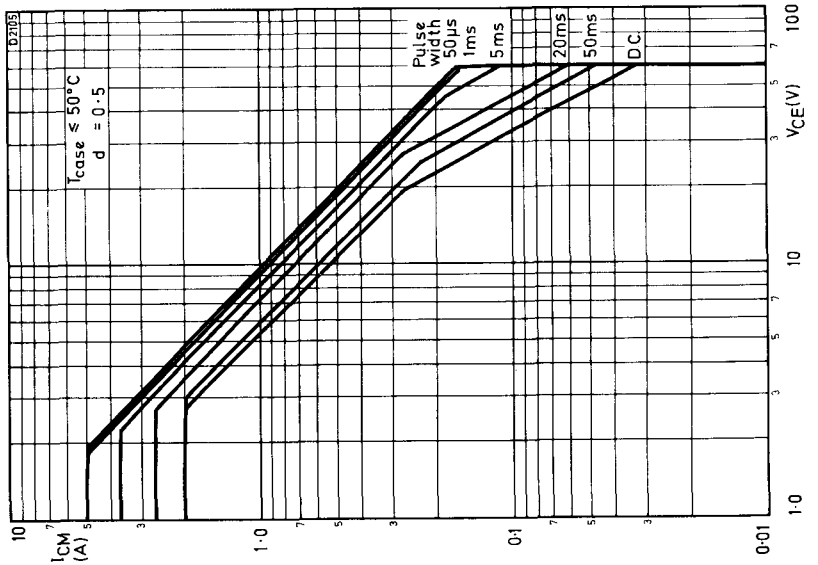


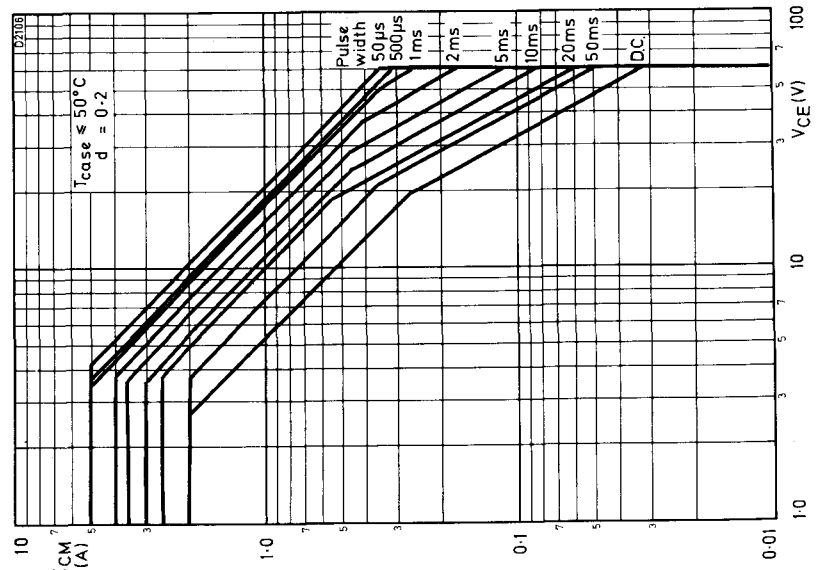

D2101
100
P_{max}
(%)
50
0
0
50
100
150
200
T_{case} (°C)

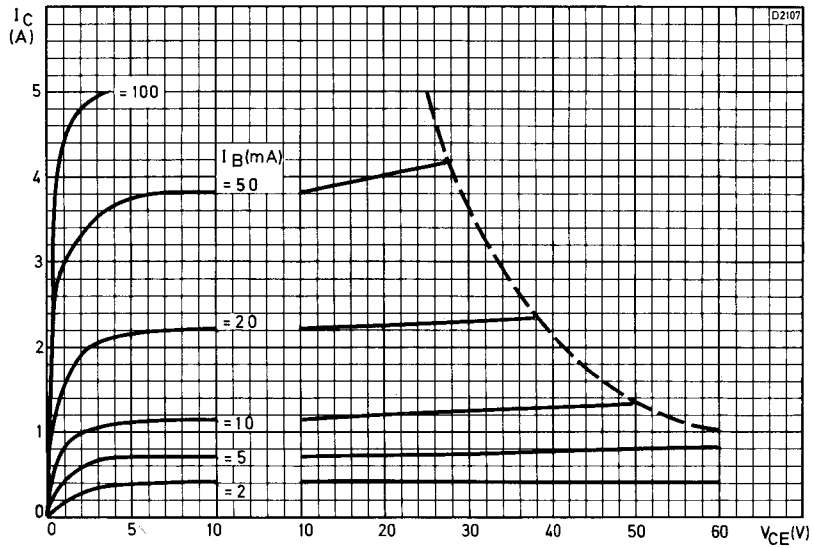

D2102
I_C
(A)
V_{CE} = 2·0 V
T_j = 25°C
Min.
Max.
5
4
3
2
1
0
0
0·5
1·0
1·5
2·0
V_{BE}(V)

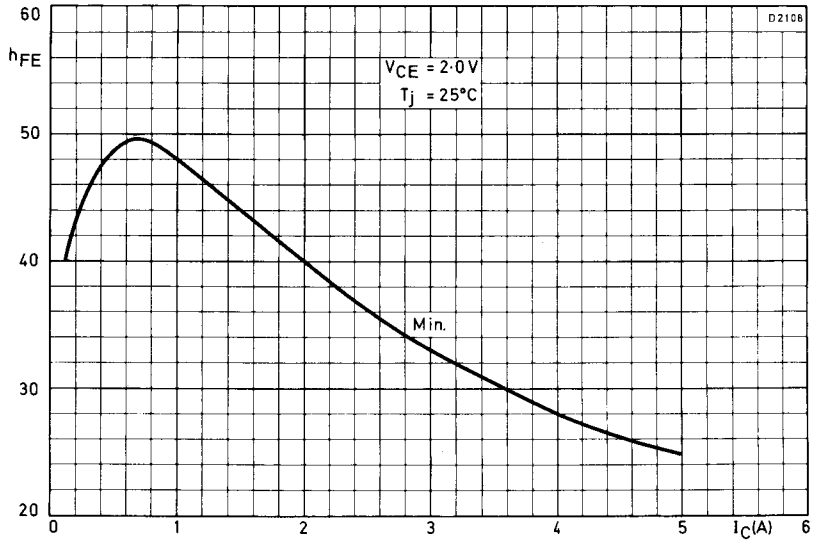

D2104
$T_{case} \leq 50°C$
$d \leq 0{\cdot}01$
I_{CM} (A)
Pulse width
50µs
100µs
200µs
500µs
50 µs
100 µs
200 µs
500µs
1 ms
2 ms
5 ms
10 ms
20 ms
50 ms
D.C
10
1·0
0·1
0·01
1·0
10
100
V_{CE}(V)

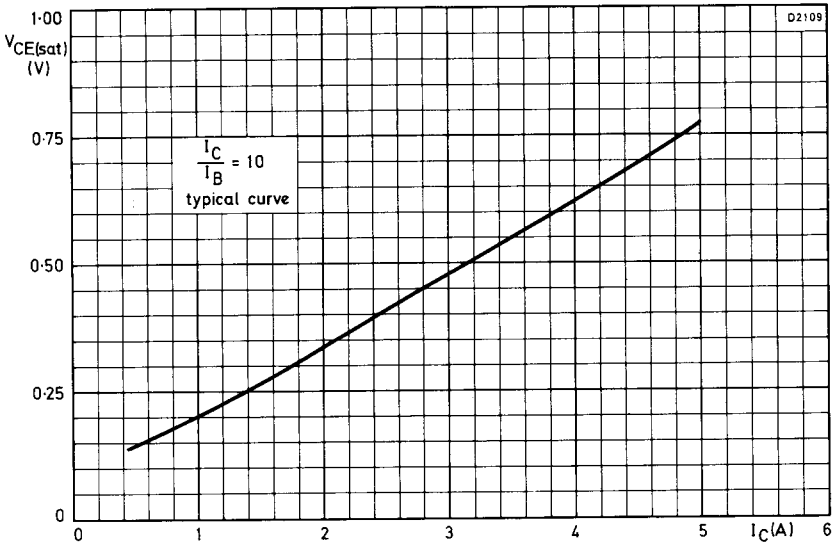

D2103
$T_{case} \leq 50°C$
$d = 0{\cdot}1$
I_{CM} (A)
Pulse width
50 µs
100 µs
200 µs
500µs
1 ms
2 ms
5 ms
10 ms
20 ms
50 ms
D.C
10
1·0
0·1
0·01
1·0
10
100
V_{CE}(V)

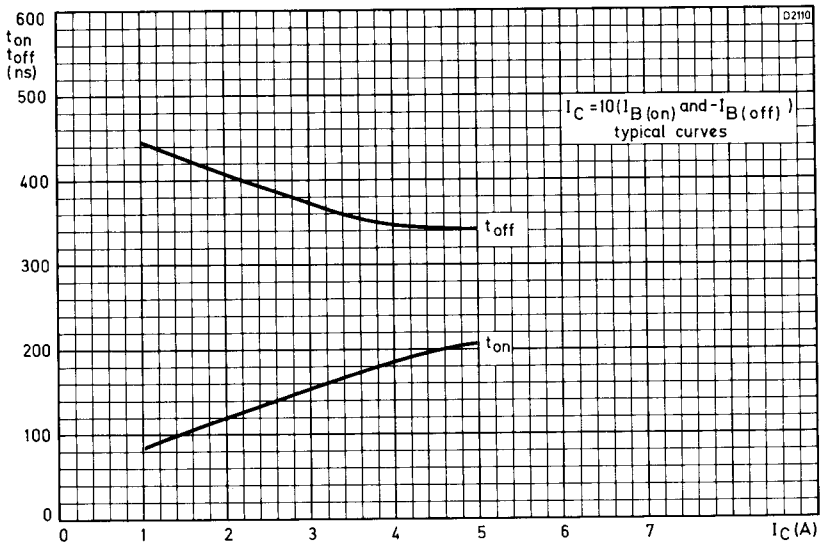

D2105
$T_{case} \leq 50°C$
d = 0·5
Pulse width
50µs
1ms
5ms
20ms
50ms
D.C.
I_{CM} (A)
V_{CE}(V)
10
1·0
0·1
0·01
1·0
10
100


D2106
$T_{case} \leq 50°C$
d = 0·2
Pulse width
50µs
500µs
1ms
2ms
5ms
10ms
20ms
50ms
D.C.
I_{CM} (A)
V_{CE}(V)
10
1·0
0·1
0·01
1·0
10
100


D2107
I_C (A)
5
4
3
2
1
0
= 100
I_B(mA)
= 50
= 20
= 10
= 5
= 2
0
5
10
10
20
30
40
50
60
V_{CE}(V)


D2108
60
h_{FE}
50
40
30
20
V_{CE} = 2·0 V
T_j = 25°C
Min.
0
1
2
3
4
5
I_C(A)
6


D2109
1·00
$V_{CE(sat)}$ (V)
0·75
0·50
0·25
0
$\frac{I_C}{I_B} = 10$
typical curve
0
1
2
3
4
5
I_C(A)
6


D2110
600
t_{on}
t_{off}
(ns)
500
400
300
200
100
0
$I_C = 10(I_{B(on)}$ and $-I_{B(off)})$
typical curves
t_{off}
t_{on}
0
1
2
3
4
5
6
7
I_C(A)

P-N-P SILICON PLANAR EPITAXIAL TRANSISTOR

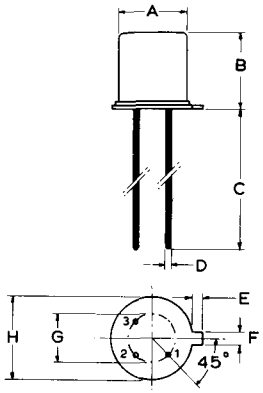
BSV68

Silicon planar epitaxial transistor intended for anode switching in dynamically driven numerical indicator tubes.

QUICK REFERENCE DATA		
$-V_{CER}$ max. (R_{BE} = 10kΩ)	110	V
$-V_{CEO}$ max.	100	V
$-I_{CM}$ max.	100	mA
P_{tot} max. ($T_{amb} \leq 25^{o}C$)	250	mW
T_j max.	150	^{o}C
h_{FE} min. ($-I_C$ = 25mA, $-V_{CE}$ = 5V)	30	
f_T typ. ($-I_C$ = 25mA, $-V_{CE}$ = 5V, f = 35MHz)	95	MHz

OUTLINE AND DIMENSIONS

Conforms to B.S. 3934 SO-12A/SB3-6A
J.E.D.E.C. TO-18



	Millimetres		
	Min.	Typ.	Max.
A	-	-	4.8
B	-	-	5.3
C	12.7	-	-
D	-	-	0.48
E	-	-	1.17
F	-	-	1.16
G	-	2.54	-
H	-	-	5.8

Viewed from underside

Connections:
1. Emitter
2. Base
3. Collector connected to envelope

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

$-V_{CBO}$ max. ($-I_C = 10\mu A$)	110	V
$-V_{CER}$ max. ($-I_C = 10\mu A$, $R_{BE} = 10k\Omega$)	110*	V
$-V_{CEO}$ max. ($-I_C = 100\mu A$)	100	V
$-V_{EBO}$ max. ($-I_E = 10\mu A$)	6.0	V
$-I_C$ max.	100	mA
$-I_{CM}$ max.	100†	mA
$-I_{BM}$ max.	100	mA
P_{tot} max. ($T_{amb} \leq 25^oC$)	250	mW

Temperature

T_{stg}	-65 to +150	^oC
T_j max.	150	^oC

THERMAL CHARACTERISTIC

$R_{th(j-amb)}$	0.5	degC/mW

ELECTRICAL CHARACTERISTICS ($T_j = 25^oC$ unless otherwise stated)

		Min.	Typ.	Max.	
$-I_{CBO}$	Collector-base cut-off current $I_E = 0$, $-V_{CB} = 100V$, $T_j = 70^oC$	-	-	10	μA
$-I_{CER}$	Collector-emitter cut-off current $-V_{CE} = 110V$, $R_{BE} = 10k\Omega$	-	-	10	μA
$-I_{EBO}$	Emitter-base cut-off current $I_C = 0$, $-V_{EB} = 6V$	-	-	10	μA

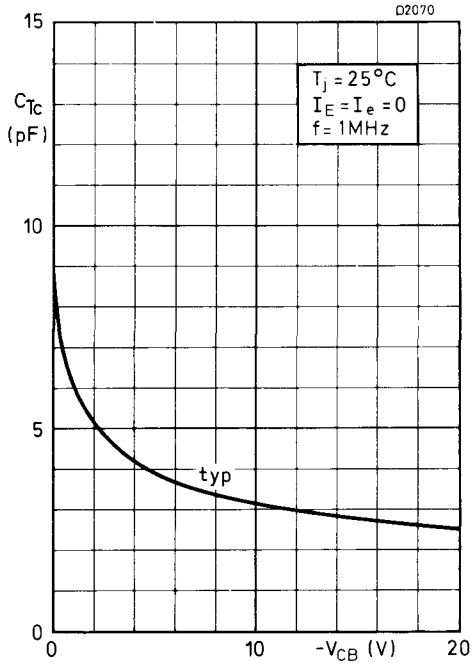
*The transistor may be operated in the breakdown region, provided the collector current does not exceed $10\mu A$ at $T_{amb} = 70^oC$.

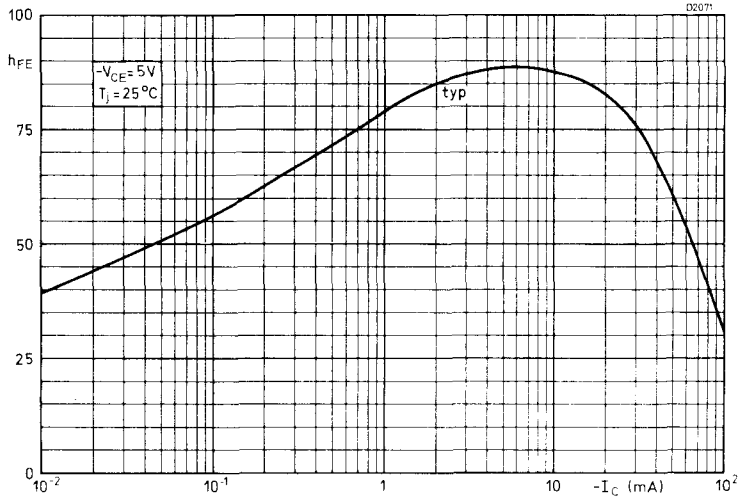
It can withstand an inductive load of 4mH in series with a resistance of $4k\Omega$, combined with a collector current of 25mA before switching-off.

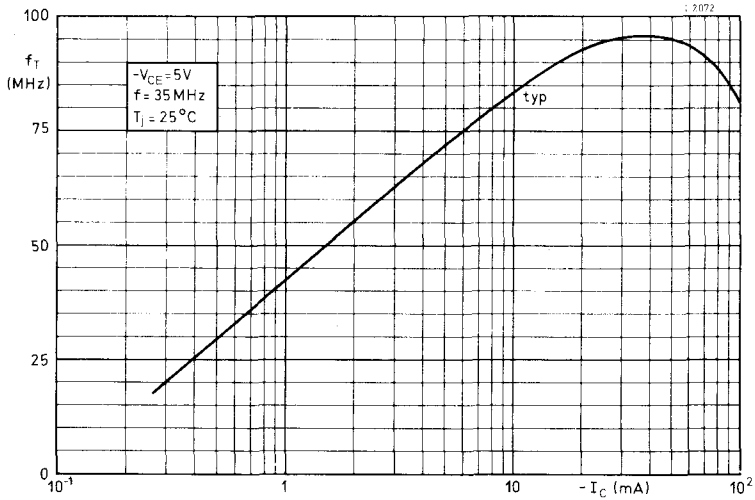
†The transistor can withstand a capacitive load of 100pF, combined with a collector voltage equal to $-V_{CER}$ before switching-on.

ELECTRICAL CHARACTERISTICS (contd.)

		Min.	Typ.	Max.	
$-V_{CE(sat)}$	Collector-emitter saturation voltage $-I_C = 25mA$, $-I_B = 2.5mA$	-	-	250	mV
$-V_{BE(sat)}$	Base-emitter saturation voltage $-I_C = 25mA$, $-I_B = 2.5mA$	-	-	900	mV
h_{FE}	Static forward current transfer ratio				
	$-I_C = 10mA$, $-V_{CE} = 5V$	30	-	-	
	$-I_C = 25mA$, $-V_{CE} = 5V$	30	-	-	
C_{Tc}	Collector capacitance $I_E = I_e = 0$, $-V_{CB} = 10V$, $f = 1MHz$	-	-	5.0	pF
f_T	Transition frequency $-I_C = 25mA$, $-V_{CE} = 5V$, $f = 35MHz$	50	95	-	MHz

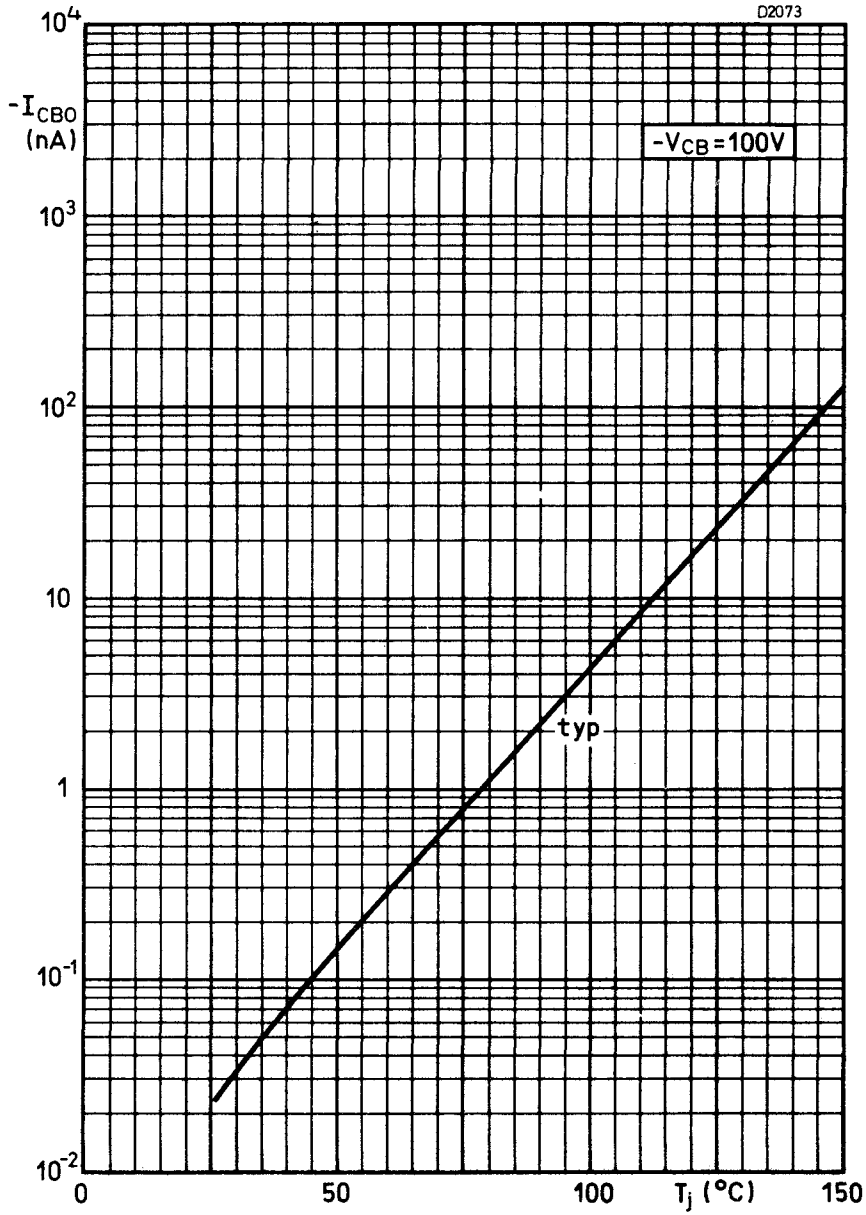



D2071
100
h_{FE}
$-V_{CE}$ = 5V
T_j = 25 °C
typ
75
50
25
0
10^{-2}
10^{-1}
1
10
$-I_C$ (mA)
10^2


2072
100
f_T
(MHz)
$-V_{CE}$ = 5V
f = 35 MHz
T_j = 25 °C
typ
75
50
25
0
10^{-1}
1
10
$-I_C$ (mA)
10^2

P-N-P SILICON PLANAR EPITAXIAL TRANSISTOR

BSV68



OUTL

g

All dim

MAY 1

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{DS} max.	Drain-source voltage	40	V
V_{DGO} max.	Drain-gate voltage (open source)	40	V
$-V_{GSO}$ max.	Gate-source voltage (open drain)	40	V
I_G max.	Forward gate current	50	mA
P_{tot} max.	Total power dissipation, $T_{amb} \leq 25^oC$	350	mW

Temperature

T_{stg}	Storage temperature	-65 to +200	^oC
T_j max.	Junction temperature	175	^oC

THERMAL CHARACTERISTICS

$R_{th(j-amb)}$	Thermal resistance from junction to ambient in free air	0.43	degC/mW

ELECTRICAL CHARACTERISTICS ($T_j = 25^o$ unless otherwise stated)

			Min.	Typ.	Max.	
$-I_{GSS}$	Gate cut-off current					
	$-V_{GS} = 20V$, $V_{DS} = 0$		-	-	0.25	nA
	$-V_{GS} = 20V$, $V_{DS} = 0$, $T_j = 150^oC$		-	-	0.5	μA
I_D	Drain cut-off current					
	$V_{DS} = 15V$, $-V_{GS} = 12V$		-	-	0.25	nA
	$V_{DS} = 15V$, $-V_{GS} = 12V$, $T_j = 150^oC$		-	-	0.5	μA
I_{DSS}	Drain current					
	$V_{DS} = 15V$, $V_{GS} = 0$	BSV78	50	-	-	mA
		BSV79	20	-	-	mA
		BSV80	10	-	-	mA
$-V_{(P)GS}$	Gate-source cut-off voltage					
	$I_D = 1nA$, $V_{DS} = 15V$	BSV78	3.75	-	11	V
		BSV79	2.0	-	7.0	V
		BSV80	1.0	-	5.0	V

ELECTRICAL CHARACTERISTICS (contd.)

			Min.	Typ.	Max.	
$-V_{GS}$	Gate-source voltage $I_D = 1.5\mu A$, $V_{DS} = 15V$	BSV78	3.5	-	10	V
		BSV79	1.75	-	6.0	V
		BSV80	0.75	-	4.0	V
$V_{DS(on)}$	Drain-source 'on' voltage					
	$I_D = 20mA$, $V_{GS} = 0$	BSV78	-	-	500	mV
	$I_D = 10mA$, $V_{GS} = 0$	BSV79	-	-	400	mV
	$I_D = 5mA$, $V_{GS} = 0$	BSV80	-	-	325	mV
$r_{DS(on)}$	Drain-source 'on' resistance					
	$I_D = 0$, $V_{GS} = 0$, $f = 1kHz$	BSV78	-	-	25	Ω
		BSV79	-	-	40	Ω
		BSV80	-	-	60	Ω

y-parameters at f = 1MHz (common source)
$-V_{GS} = 10V$, $V_{DS} = 0$

C_{is}	Input capacitance	-	-	10	pF
$-C_{rs}$	Feedback capacitance	-	-	5	pF

Switching characteristics (see test circuit on page 4)

Turn-on time when switched from:

$-V_{GSM} = 11V$ to $I_D = 20mA$, $V_{DD} = 10V$ (BSV78)
$-V_{GSM} = 7V$ to $I_D = 10mA$, $V_{DD} = 10V$ (BSV79)
$-V_{GSM} = 5V$ to $I_D = 5mA$, $V_{DD} = 10V$ (BSV80)

			BSV78	BSV79	BSV80	
t_d	Delay time	max.	5.0	10	8.0	ns
t_r	Rise time	max.	5.0	5.0	7.0	ns
t_{on}	Turn-on time	max.	10	15	15	ns

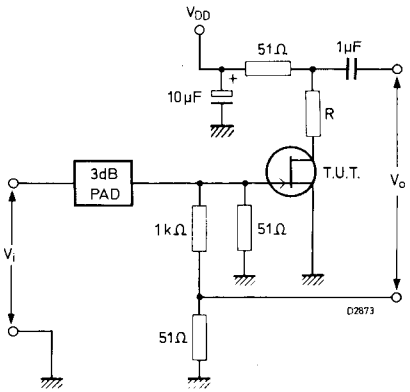
Switching characteristics (contd.)

Turn-off time when switched from:

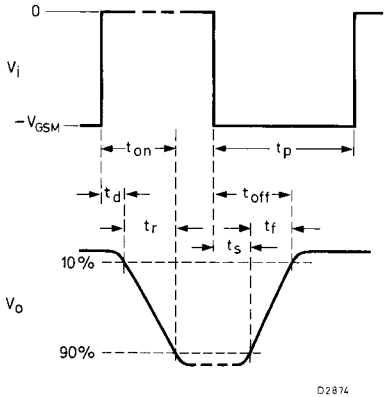
$I_D = 20mA$ to $-V_{GSM} = 11V$, $V_{DD} = 10V$ (BSV78)
$I_D = 10mA$ to $-V_{GSM} = 7V$, $V_{DD} = 10V$ (BSV79)
$I_D = 5mA$ to $-V_{GSM} = 5V$, $V_{DD} = 10V$ (BSV80)

		BSV78	BSV79	BSV80	
t_f	Fall time	6.0	10	20	ns
t_s	Storage time	4.0	5.0	5.0	ns
t_{off}	Turn-off time	10	15	25	ns

Test circuit:



Input and output waveforms:



$$R_L = \frac{10 - V_{DS(on)}}{I_{D(on)}} - 51\Omega$$

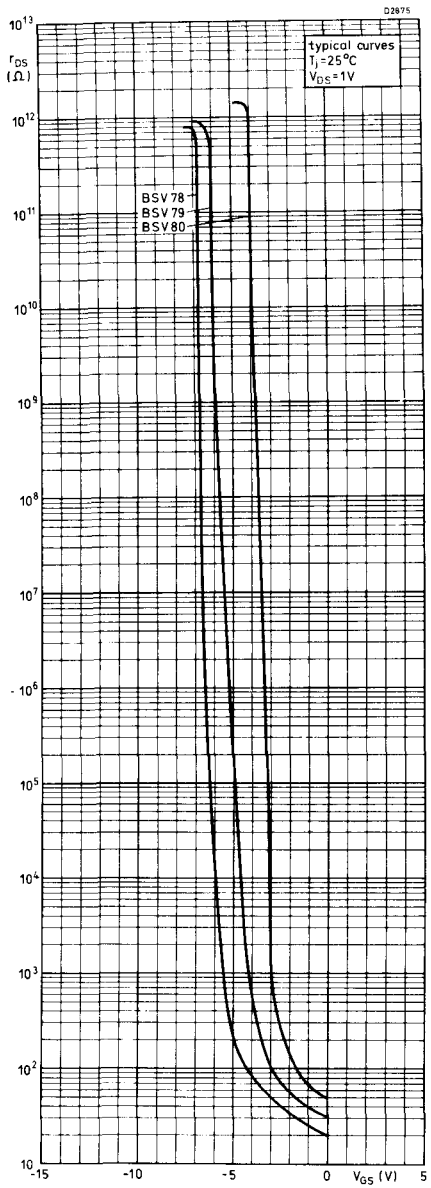
	BSV78	BSV79	BSV80	
R_L =	424	909	1885	Ω

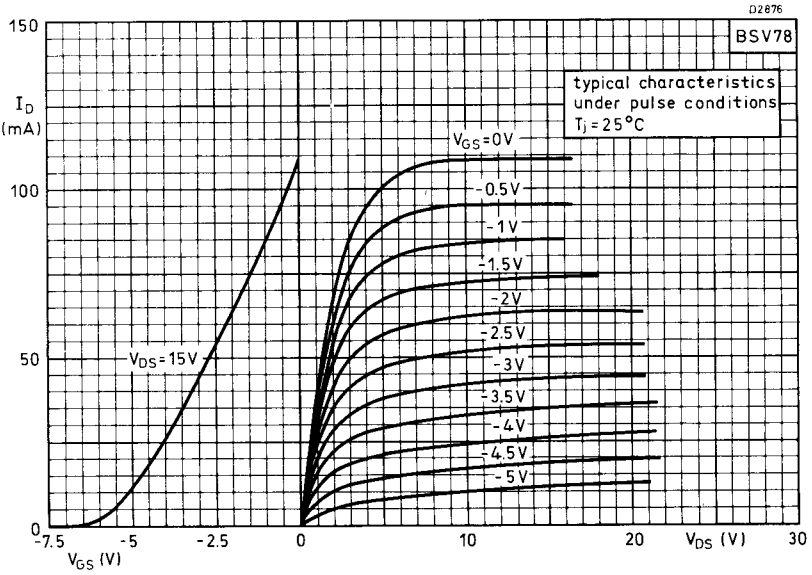
Pulse generator:

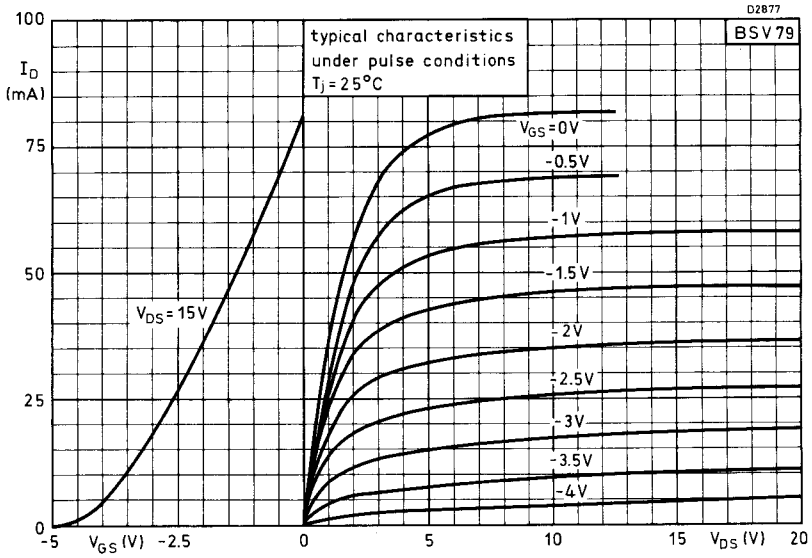
R_i = 50Ω
t_r < 0.5ns
t_f < 5ns

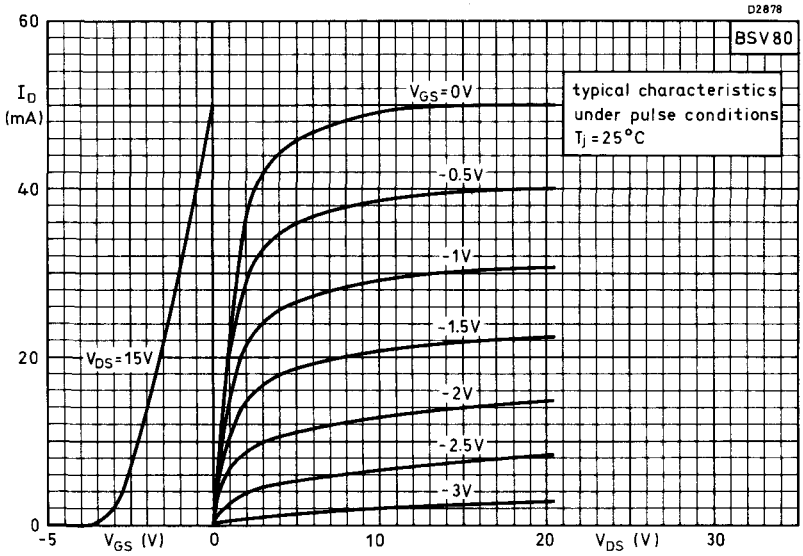
Oscilloscope:

R_i = 50Ω
t_r < 1ns
t_f < 1ns


D2875
typical curves
T_j=25°C
V_{DS}=1V
r_{DS} (Ω)
BSV78
BSV79
BSV80
10^{13}
10^{12}
10^{11}
10^{10}
10^{9}
10^{8}
10^{7}
10^{6}
10^{5}
10^{4}
10^{3}
10^{2}
10
-15
-10
-5
0
V_{GS} (V)
5


D2876
BSV78
typical characteristics
under pulse conditions
$T_j = 25°C$
I_D (mA)
150
100
50
0
V_{GS}=0V
-0.5V
-1V
-1.5V
-2V
-2.5V
-3V
-3.5V
-4V
-4.5V
-5V
V_{DS}=15V
-7.5
-5
-2.5
0
10
20
30
V_{GS} (V)
V_{DS} (V)


D2877
BSV79
typical characteristics
under pulse conditions
$T_j = 25°C$
I_D (mA)
100
75
50
25
0
V_{GS}=0V
-0.5V
-1V
-1.5V
-2V
-2.5V
-3V
-3.5V
-4V
V_{DS}=15V
-5
-2.5
0
5
10
15
20
V_{GS} (V)
V_{DS} (V)


D2878
BSV80
typical characteristics
under pulse conditions
T_j = 25 °C
I_D (mA)
60
40
20
0
V_{GS} = 0 V
-0.5 V
-1 V
-1.5 V
-2 V
-2.5 V
-3 V
V_{DS} = 15 V
-5
V_{GS} (V)
0
10
20
V_{DS} (V)
30

N-CHANNEL INSULATED GATE FIELD EFFECT TRANSISTOR

BSV81

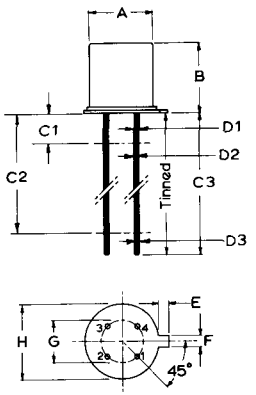
Depletion type, insulated gate, field effect transistor in a TO-72 metal envelope, with the substrate connected to the case. It is intended for chopper and other special switching applications e.g. timing circuits, multiplex circuits etc.
The BSV81 features a very low drain-source 'on' resistance, a very high drain-source 'off' resistance and low feedback capacitances.

QUICK REFERENCE DATA

$r_{DS(on)}$ max. ($V_{DS}=0$, $V_{GS}=5V$, $V_{BS}=0$, f=1kHz)	50	Ω
$r_{DS(off)}$ min. ($V_{DS}=10V$, $-V_{GS}=5V$, $V_{BS}=0$)	10	GΩ
$-C_{rs}$ max. ($-V_{GS}=5V$, $V_{DS}=0$, $I_B=0$, f=1MHz)	0.5	pF
$-C_{rd}$ max. ($-V_{GD}=5V$, $V_{SD}=0$, $I_B=0$, f=1MHz)	1.2	pF

OUTLINE AND DIMENSIONS

Conforms to BS 3934 SO-12A/SB4-3
J.E.D.E.C. TO-72



Viewed from underside

Millimetres

	Min.	Nom.	Max.
A	4.53	-	4.8
B	4.66	-	5.33
C1	-	-	0.51
C2	12.7	-	-
C3	12.7	-	15
D1	-	-	1.01
D2	0.41	-	0.48
D3	-	-	0.53
E	0.84	-	1.17
F	0.92	-	1.16
G	-	2.54	-
H	5.31	-	5.84

Connections
1. Drain
2. Source
3. Gate
4. Substrate connected to envelope

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{DB} max.	Drain-substrate voltage	30	V
V_{SB} max.	Source-substrate voltage	30	V
$\pm V_{GB}$ max.	Gate-substrate voltage (continuous)	10	V
$\pm V_{G-N}$ max.	Repetitive peak gate voltage (gate to all other terminals) $V_{SB}=V_{DB}=0$, f>100Hz	15	V
$\pm V_{G-N}$ max.	Non-repetitive peak gate voltage (gate to all other terminals) $V_{SB}=V_{DB}=0$, t<10ms	50	V
I_{DM} max.	Peak drain current $t_r=20ms$, d=0.1	50	mA
I_{SM} max.	Peak source current $t_r=20ms$, d=0.1	50	mA
P_{tot} max.	Total power dissipation $T_{amb} \leq 25^oC$	200	mW

Temperature

T_{stg}	Storage temperature	-65 to +125	^oC
T_j max.	Junction temperature	125	^oC

THERMAL CHARACTERISTIC

$R_{th(j-amb)}$	Thermal resistance, junction to ambient, in free air	0.5	degC/mW

ELECTRICAL CHARACTERISTICS ($T_j=25^oC$ unless otherwise stated)

		Min.	Max.	
I_{DSX}	Drain cut-off current, $V_{BS}=0$			
	$V_{DS}=10V$, $-V_{GS}=5V$	-	1.0	nA
	$V_{DS}=10V$, $-V_{GS}=5V$, $T_j=125^oC$	-	1.0	μA
I_{SDX}	Source cut-off current, $V_{BD}=0$			
	$V_{SD}=10V$, $-V_{GD}=5V$	-	1.0	nA
	$V_{SD}=10V$, $-V_{GD}=5V$, $T_j=125^oC$	-	1.0	μA
	Gate current, $V_{BS}=0$			
$-I_{GSS}$	$-V_{GS}=10V$, $V_{DS}=0$	-	10	pA
I_{GSS}	$V_{GS}=10V$, $V_{DS}=0$	-	10	pA
$-I_{GSS}$	$-V_{GS}=10V$, $V_{DS}=0$, $T_j=125^oC$	-	200	pA
I_{GSS}	$V_{GS}=10V$, $V_{DS}=0$, $T_j=125^oC$	-	200	pA

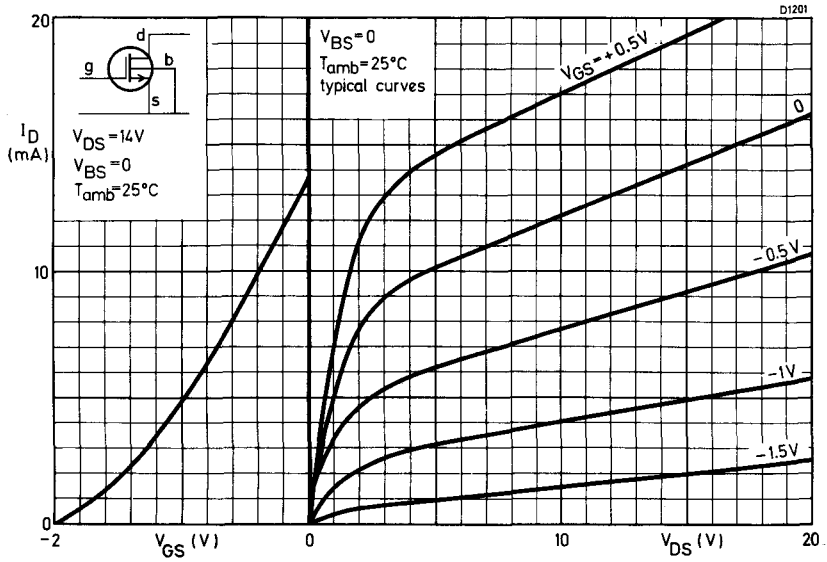
ELECTRICAL CHARACTERISTICS (cont'd)

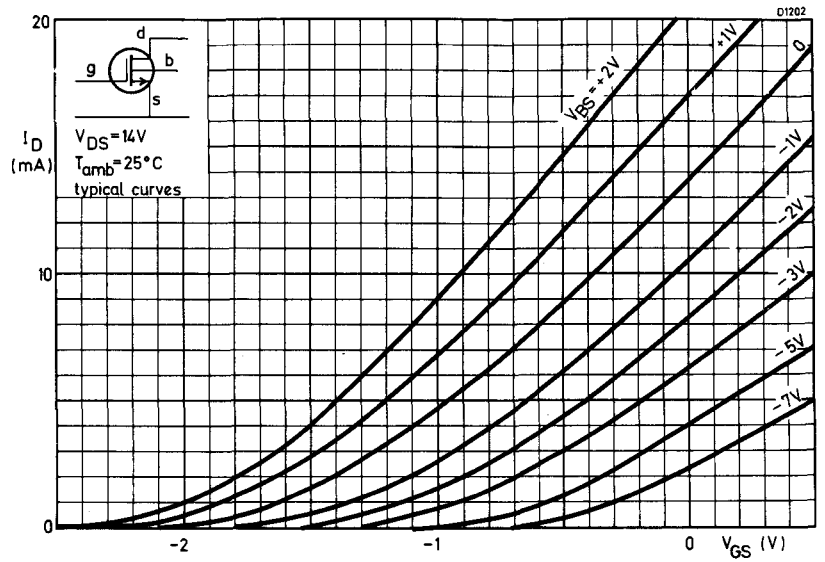
		Min.	Max.	
	Substrate current, $V_{GB}=0$			
$-I_{BDO}$	$-V_{BD}=30V$, $I_S=0$	-	10	μA
$-I_{BSO}$	$-V_{BS}=30V$, $I_D=0$	-	10	μA
$r_{DS(on)}$	Drain-source 'on' resistance at f=1kHz, $V_{BS}=0$			
	$V_{GS}=0$, $V_{DS}=0$	-	100	Ω
	$V_{GS}=0$, $V_{DS}=0$, $T_j=125^oC$	-	150	Ω
	$+V_{GS}=5V$, $V_{DS}=0$	-	50	Ω
$r_{DS(off)}$	Drain-source 'off' resistance $-V_{GS}=5V$, $V_{DS}=10V$, $V_{BS}=0$	10	-	GΩ
	Feedback capacitance at f=1MHz			
$-C_{rs}$	$-V_{GS}=5V$, $V_{DS}=0$, $I_B=0$	-	0.5	pF
$-C_{rd}$	$-V_{GD}=5V$, $V_{SD}=0$, $I_B=0$	-	1.2	pF
	Gate to all other terminals capacitance at f=1MHz			
C_{g-n}	$-V_{GB}=5V$, $V_{SB}=V_{DB}=0$	-	5.0	pF

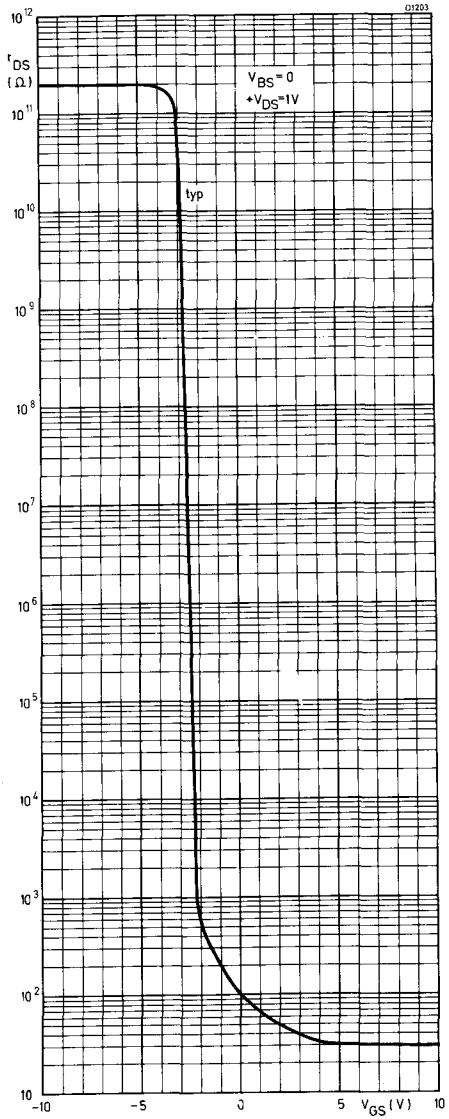
OPERATING NOTE

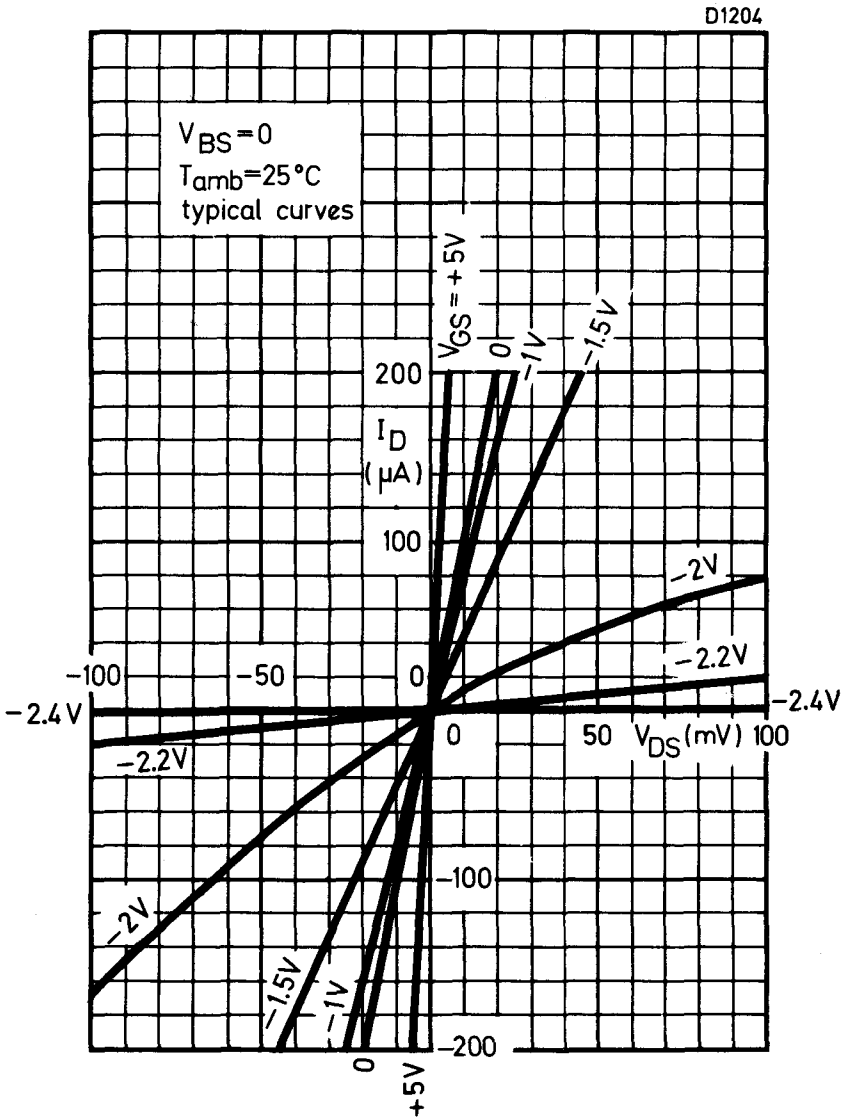
Mounting and handling instructions

To exclude the possibility of damage to the gate oxide layer by an electrostatic charge building up on the high resistance gate electrode, the device is fitted with a conductive rubber ring around the leads. This ring should not be removed until after the device has been mounted in the circuit.


D1201
20
10
0
I_D (mA)
d
g
b
s
V_{DS}=14V
V_{BS}=0
T_{amb}=25°C
V_{BS}=0
T_{amb}=25°C
typical curves
V_{GS}=+0.5V
0
-0.5V
-1V
-1.5V
-2
V_{GS} (V)
0
10
V_{DS} (V)
20


D1202
20
10
0
I_D (mA)
d
g
b
s
V_{DS}=14V
T_{amb}=25°C
typical curves
V_{BS}=+2V
+1V
0
-1V
-2V
-3V
-5V
-7V
-2
-1
0
V_{GS} (V)


C1203
10^{12}
r_{DS} (Ω)
10^{11}
10^{10}
10^{9}
10^{8}
10^{7}
10^{6}
10^{5}
10^{4}
10^{3}
10^{2}
10
V_{BS} = 0
+V_{DS}=1V
typ
-10
-5
0
5
10
V_{GS} (V)


D1204
$V_{BS}=0$
$T_{amb}=25°C$
typical curves
$V_{GS}=+5V$
0
-1V
-1.5V
200
I_D
(μA)
100
-2V
-2.2V
-100
-50
0
-2.4V
-2.4V
0
50
V_{DS}(mV)
100
-2.2V
-100
-2V
-1.5V
-1V
0
+5V
-200

N-P-N SILICON PLANAR EPITAXIAL TRANSISTORS

BSW66
BSW67
BSW68

N-P-N silicon planar epitaxial transistors intended for highly inductive load switching.

QUICK REFERENCE DATA

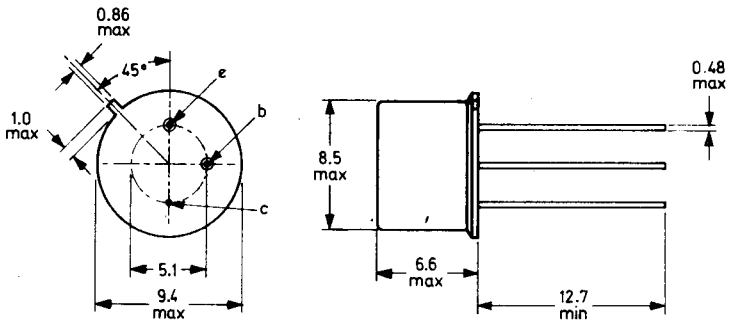
	BSW66	BSW67	BSW68	
V_{CBO} max.	100	120	150	V
V_{CEO} max.	100	120	150	V
I_{CM} max.		2.0		A
P_{tot} max. T_{case} = 100°C		2.85		W
T_{amb} = 45°C		0.7		W
E max., L = 150mH		5.0		mWs
T_j max.		200		°C
h_{FE} min., V_{CE} = 5V, I_C = 10mA		30		
V_{CE} = 5V, I_C = 500mA		30		
$V_{CE(sat)}$ max., I_C = 500mA, I_B = 50mA	400	400	500	mV
f_T typ., V_{CB} = 20V, $-I_E$ = 100mA, f = 35MHz		80		MHz

Unless otherwise stated data is applicable to all types

OUTLINE AND DIMENSIONS

Conforms to BS 3934 SO-3/SB3-3A
J.E.D.E.C. TO-39

Collector connected to case



All dimensions in mm

D1574

Max. lead diameter is only guaranteed for 12.7mm

Accessories available:- 56218, 56245, 56265

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

	BSW66	BSW67	BSW68	
V_{CBO} max.	100	120	150	V
V_{CEO} max.	100	120	150	V
V_{EBO} max.		6.0		V
$I_{C(AV)}$ max. ($t_{av} \leq 20ms$)		1.0		A
I_{CM} max.		2.0		A
P_{tot} max. $T_{case} \leq 25^{o}C$		5.0		W
$T_{amb} \leq 25^{o}C$		0.8		W
E max. (switch-off energy, L=150mH)		5.0		mWs

Temperature

T_{stg} range	-65 to +200	^{o}C
T_j max.	200	^{o}C

THERMAL CHARACTERISTICS

$R_{th(j-amb)}$ In free air	220	degC/W
$R_{th(j-case)}$	35	degC/W

ELECTRICAL CHARACTERISTICS ($T_j = 25^{o}C$ unless otherwise stated)

			Min.	Typ.	Max.	
I_{CBO}	Collector cut-off current					
	$V_{CB} = 1/2V_{CBO}$ max. $I_E = 0$		-	-	100	nA
	$V_{CB} = 1/2V_{CBO}$ max. $I_E = 0$, $T_j = 150^{o}C$		-	-	50	μA
	$V_{CB} = V_{CBO}$ max. $I_E = 0$		-	-	100	μA
I_{EBO}	Emitter cut-off current					
	$V_{EB} = 3.0V$, $I_C = 0$		-	-	100	nA
	$V_{EB} = 6.0V$, $I_C = 0$		-	-	100	μA
$V_{(BR)CEO}$	Collector-emitter breakdown voltage					
	$I_C = 100mA$, $I_B = 0$	BSW66	100	-	-	V
		BSW67	120	-	-	V
		BSW68	150	-	-	V

ELECTRICAL CHARACTERISTICS (contd.)

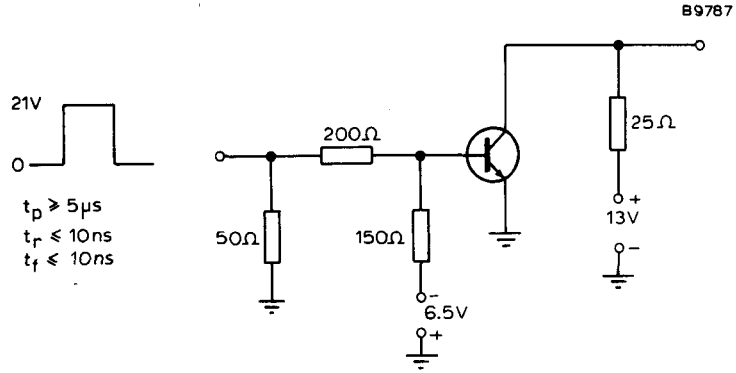
		Min.	Typ.	Max.	
$V_{CE(sat)}$	Collector-emitter saturation voltage				
	$I_C = 100mA$, $I_B = 10mA$	-	-	150	mV
	$I_C = 500mA$, $I_B = 50mA$				
	BSW66	-	-	400	mV
	BSW67	-	-	400	mV
	BSW68	-	-	500	mV
	$I_C = 1.0A$, $I_B = 150mA$	-	-	1.0	V
$V_{BE(sat)}$	Base-emitter saturation voltage				
	$I_C = 100mA$, $I_B = 10mA$	-	-	0.9	V
	$I_C = 500mA$, $I_B = 50mA$	-	-	1.1	V
	$I_C = 1.0A$, $I_B = 150mA$	-	-	1.2	V
h_{FE}	Static forward current transfer ratio				
	$I_C = 10mA$, $V_{CE} = 5.0V$	30	-	-	
	$I_C = 100mA$, $V_{CE} = 5.0V$	40	-	-	
	$I_C = 500mA$, $V_{CE} = 5.0V$	30	-	-	
	$I_C = 1.0A$, $V_{CE} = 5.0V$	15	-	-	
f_T	Transition frequency $-I_E = 100mA$, $V_{CB} = 20V$, $f = 35MHz$	-	80	-	MHz
C_{Tc}	Collector capacitance $V_{CB} = 10V$, $I_E = I_e = 0$, $f = 1.0MHz$	-	-	35	pF
C_{Te}	Emitter capacitance $V_{EB} = 0$, $I_C = I_c = 0$, $f = 1.0MHz$	-	-	650	pF

Switching characteristics (see test circuits on page 4)

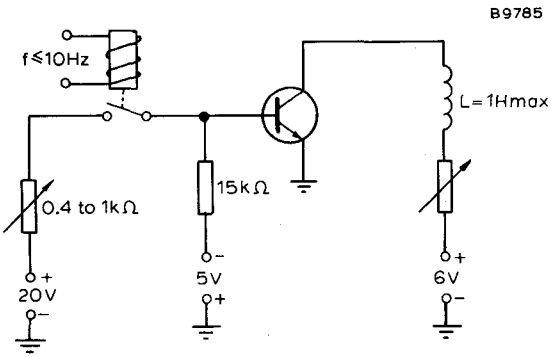
t_{on}	Turn-on time $I_C = 500mA$, $I_{Bon} = 50mA$, $-V_{BEoff} = 4V$	-	0.5	-	μs
t_{off}	Turn-off time $I_C = 500mA$, $I_{Bon} = -I_{Boff} = 50mA$	-	1.0	-	μs

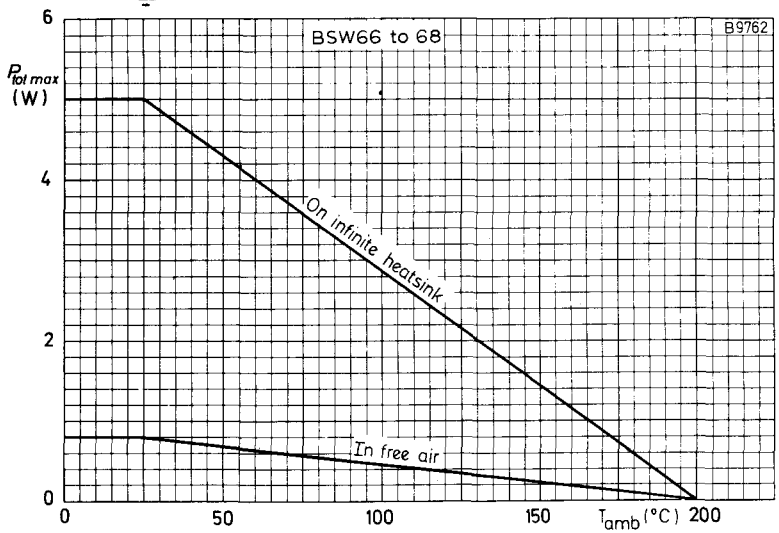
ELECTRICAL CHARACTERISTICS (cont'd)

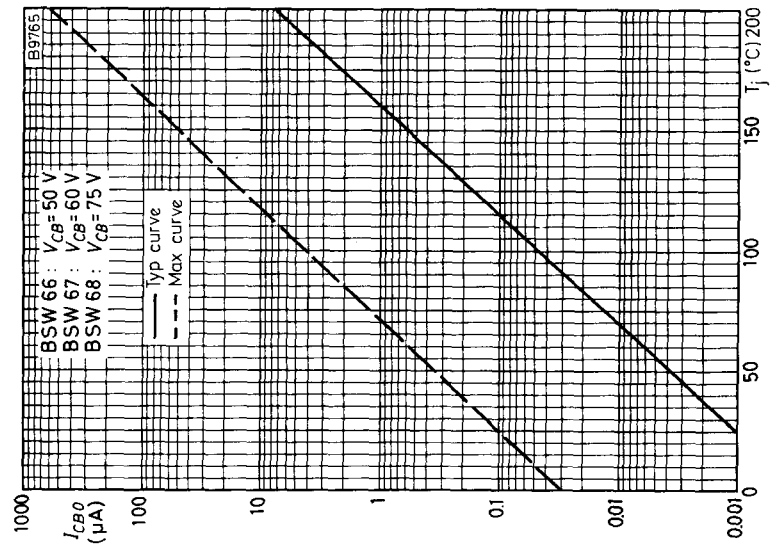
Test circuit for switching characteristics

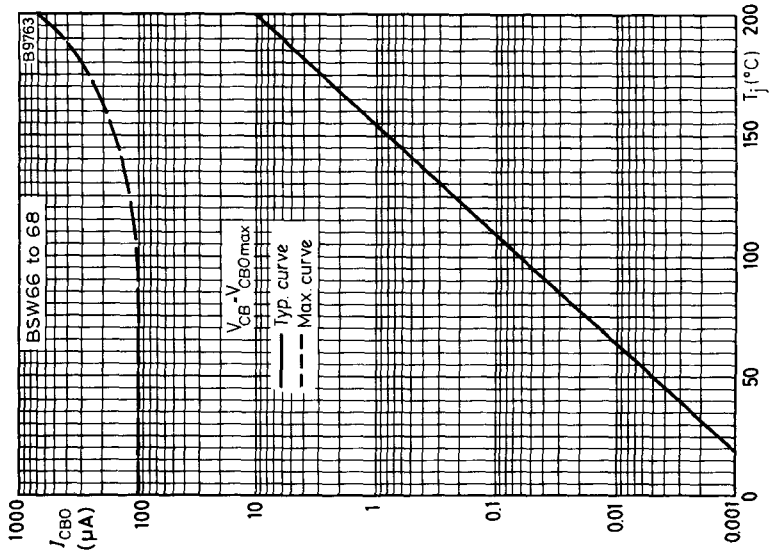


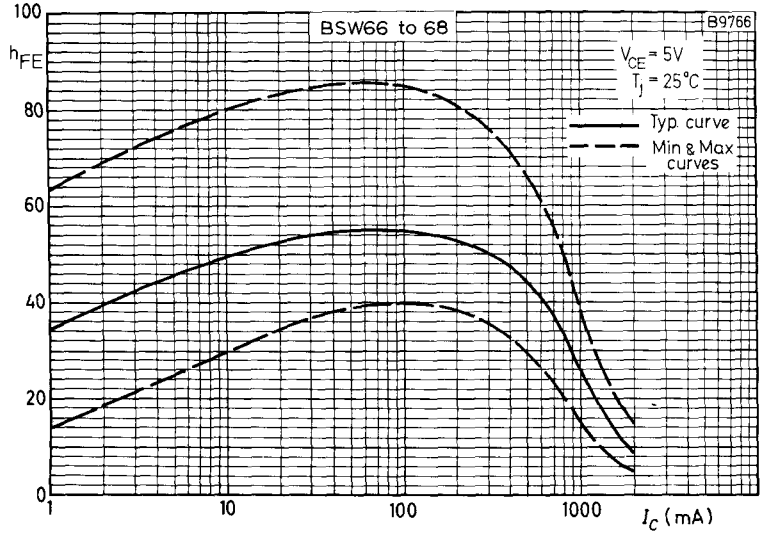
Test circuit for switch-off energy

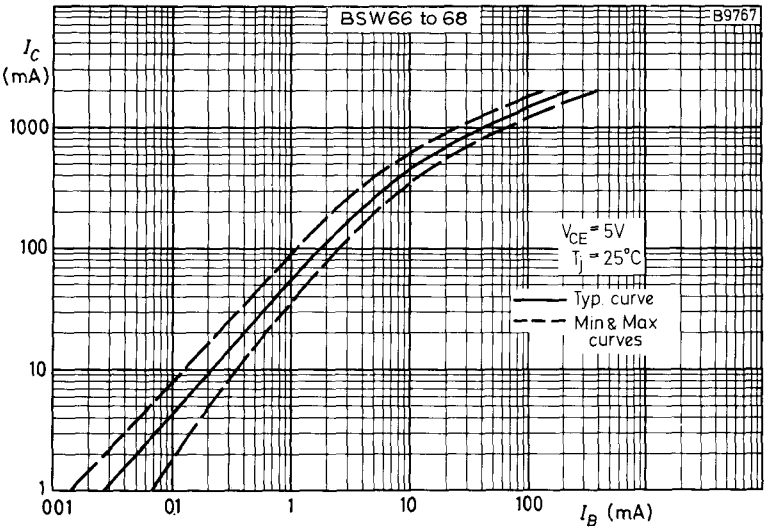


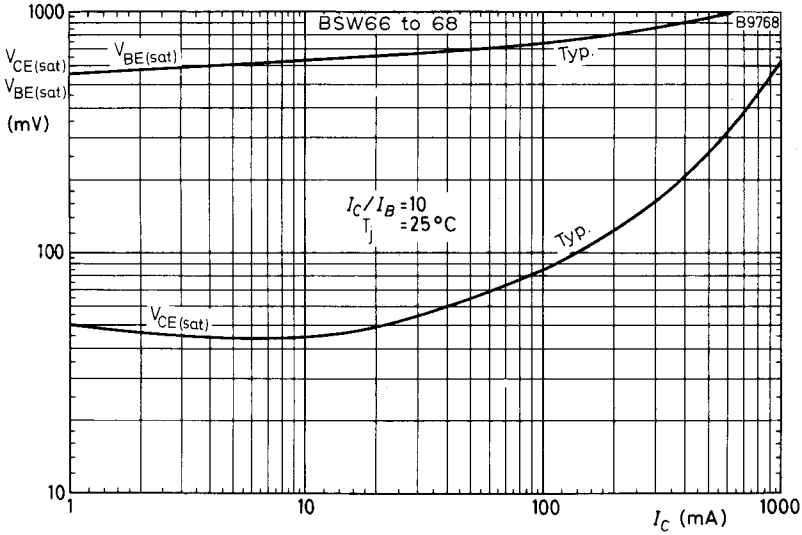


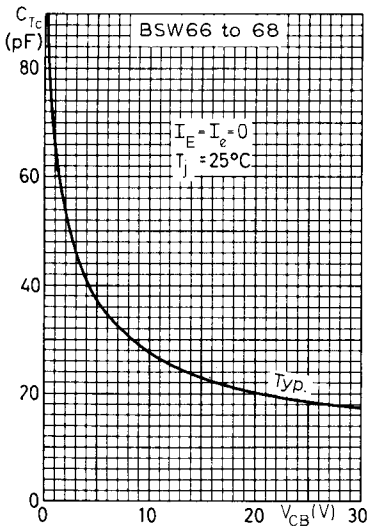

B9765
BSW 66 : V_{CB} = 50 V
BSW 67 : V_{CB} = 60 V
BSW 68 : V_{CB} = 75 V
Typ curve
Max curve
I_{CBO} (μA)
1000
100
10
1
0.1
0.01
0.001
0
50
100
150
200
T_j (°C)

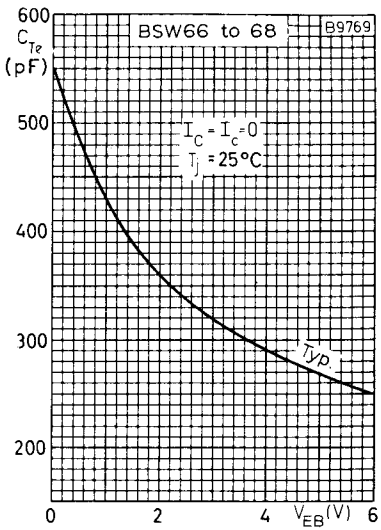

B9763
BSW66 to 68
V_{CB}=V_{CBOmax}
Typ. curve
Max. curve
I_{CBO} (μA)
1000
100
10
1
0.1
0.01
0.001
0
50
100
150
200
T_j (°C)

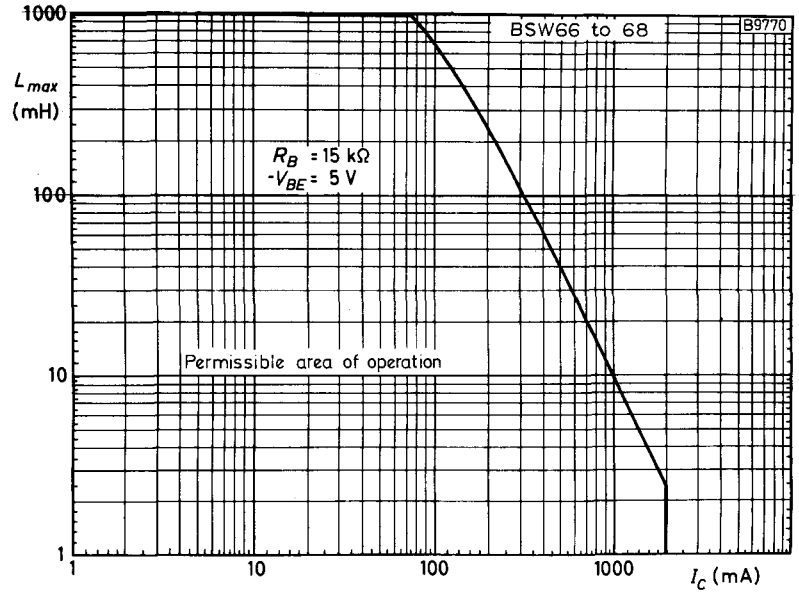

BSW66 to 68
B9766
h_{FE}
V_{CE} = 5V
T_j = 25°C
Typ. curve
Min & Max curves
100
80
60
40
20
0
1
10
100
1000
I_C (mA)

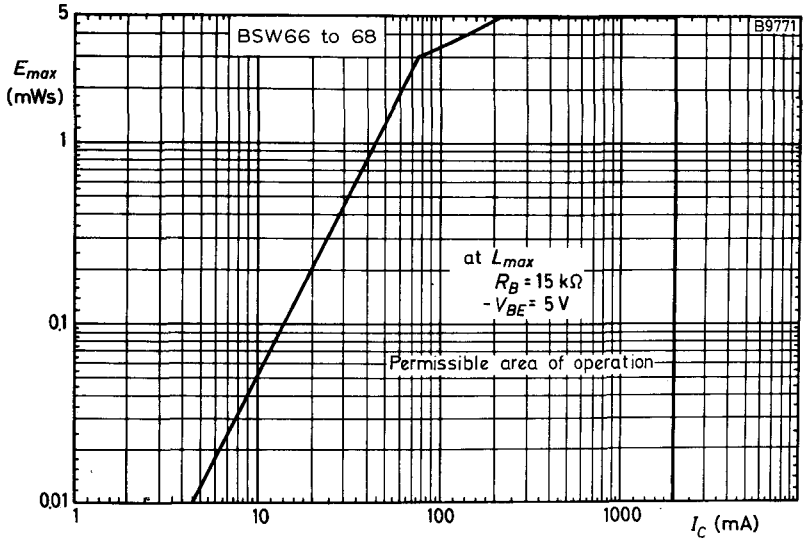

BSW66 to 68
B9767
I_C (mA)
1000
100
10
1
001
01
1
10
100
I_B (mA)
V_{CE} = 5V
T_j = 25°C
Typ. curve
Min & Max curves


BSW66 to 68
B9768
$V_{CE(sat)}$
$V_{BE(sat)}$
(mV)
$V_{BE(sat)}$
Typ.
I_C/I_B =10
T_j =25°C
Typ.
$V_{CE(sat)}$
1000
100
10
1
10
100
1000
I_C (mA)


C_{Tc}
(pF)
BSW66 to 68
80
60
40
20
0
$I_E = I_e = 0$
T_j =25°C
Typ.
0
10
20
V_{CB}(V)
30


600
C_{Te}
(pF)
BSW66 to 68
B9769
500
400
300
200
$I_C = I_c = 0$
T_j =25°C
Typ.
0
2
4
V_{EB}(V)
6


BSW66 to 68
B9770
L_{max} (mH)
1000
100
10
1
R_B = 15 kΩ
$-V_{BE}$ = 5 V
Permissible area of operation
1
10
100
1000
I_C (mA)


BSW66 to 68
B9771
E_{max} (mWs)
5
1
0,1
0,01
at L_{max}
R_B = 15 kΩ
$-V_{BE}$ = 5 V
Permissible area of operation
1
10
100
1000
I_C (mA)

SILICON N-P-N PLANAR EPITAXIAL TRANSISTORS

BSX19
BSX20

The BSX19 and BSX20 are *n-p-n* silicon planar epitaxial transistors, primarily intended for high-speed saturated switching and high frequency amplifier applications. TO-18 construction, collector connected to envelope.

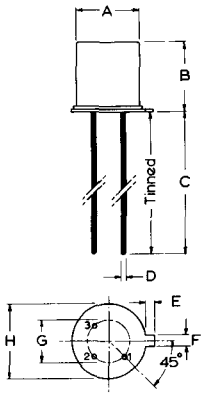
Unless otherwise shown data is applicable to both types

QUICK REFERENCE DATA

	BSX19	BSX20	
V_{CBO} max. ($I_E = 0$)	40		V
V_{CES} max. ($V_{BE} = 0$)	40		V
V_{CEO} max. ($I_B = 0$)	15		V
I_{CM} max.	500		mA
P_{tot} max. ($T_{amb} = 25^oC$)	360		mW
T_j max.	200		^oC
h_{FE} ($I_C = 10mA$, $V_{CE} = 1.0V$)	20-60	40-120	
($I_C = 100mA$, $V_{CE} = 2.0V$)	>10	>20	
f_T min. ($I_C = 10mA$, $V_{CE} = 10V$)	400	500	Mc/s
t_s max. ($I_C = I_B = -I_{BM} = 10mA$)	10	13	ns

OUTLINE AND DIMENSIONS

Conforming to J.E.D.E.C. TO-18
V.A.S.C.A. SO-12A/SB3-6A



	Millimetres		
	Min.	Nom.	Max.
A	-	-	4.8
B	-	-	5.33
C	12.7	-	-
D	-	0.43	-
E	-	1.0	-
F	-	1.05	-
G	-	2.54	-
H	5.3	5.55	5.8

Connections 1. Emitter
2. Base
3. Collector connected to envelope

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{CBO} max. ($I_E = 0$)	40	V
V_{CES} max. ($V_{BE} = 0$)	40	V
V_{CEO} max. ($I_B = 0$, $I_C = 10mA$)	15	V
V_{EBO} max. ($I_C = 0$)	4.5	V
I_{CM} max. ($t = 10\mu s$)	500	mA
P_{tot} max. ($T_{amb} = 25^oC$)	360	mW

Temperature

T_{stg} min.	-65	^oC
T_{stg} max.	200	^oC
T_j max.	200	^oC

THERMAL CHARACTERISTICS

$\Theta_{j\text{-amb}}$	0.48 deg C/mW
$\Theta_{j\text{-case}}$	0.15 deg C/mW

ELECTRICAL CHARACTERISTICS ($T_j = 25^oC$ unless otherwise stated)

		Min.	Typ.	Max.	
I_{CBO}	Collector cut-off current				
	$V_{CB} = 20V$, $I_E = 0$	-	-	400*	nA
	$V_{CB} = 20V$, $I_E = 0$, $T_j = 150^oC$	-	-	30	μA
I_{CES}	Collector-emitter cut-off current				
	$V_{CE} = 15V$, $V_{BE} = 0$, $T_j = 55^oC$	-	-	0.4	μA
	$V_{CE} = 40V$, $V_{BE} = 0$	-	-	1.0	μA
I_{EBO}	Emitter cut-off current				
	$V_{EB} = 4.5V$, $I_C = 0$	-	-	10	μA
I_{BEX}	Base-emitter cut-off current				
	$V_{CE} = 15V$, $V_{BE} = -3.0V$, $T_j = 55^oC$	-	-	-0.6	μA
I_{CEX}	Collector-emitter cut-off current				
	$V_{CE} = 15V$, $V_{BE} = -3.0V$, $T_j = 55^oC$	-	-	0.6	μA

			Min.	Typ.	Max.	
I_B	Base current					
	$I_E = -10mA$, $V_{CB} = 0$	BSX19	167*	-	500*	μA
		BSX20	83*	-	250*	μA
$V_{CEO(sust)}$	Collector-emitter sustaining voltage					
	$I_C = 10mA$, $I_B = 0$		15*	-	-	V
$V_{CER(sust)}$	$I_C = 10mA$, $R_{BE} = 10\Omega$		20	-	-	V
$V_{CE(sat)}$	Collector-emitter saturation voltage					
	$I_C = 10mA$, $I_B = 1.0mA$		-	-	0.25*	V
	$I_C = 10mA$, $I_B = 0.6mA$	BSX19	-	-	0.3	V
	$I_C = 10mA$, $I_B = 0.3mA$	BSX20	-	-	0.3	V
	$I_C = 100mA$, $I_B = 10mA$		-	-	0.60	V
$V_{BE(sat)}$	Base-emitter saturation voltage					
	$I_C = 10mA$, $I_B = 1.0mA$		0.70*	-	0.85*	V
	$I_C = 100mA$, $I_B = 10mA$		-	-	1.5	V
V_{BE}	Base-emitter voltage					
	$V_{CE} = 20V$, $I_C = 30\mu A$, $T_j = 100^oC$		0.35	-	-	V
h_{FE}	Static forward current transfer ratio					
	$I_C = 10mA$, $V_{CE} = 1.0V$	BSX19	20	-	60	
		BSX20	40	-	120	
	$I_C = 10mA$, $V_{CE} = 1.0V$,	BSX19	10	-	-	
	$T_j = -55^oC$	BSX20	20	-	-	
	$I_C = 100mA$, $V_{CE} = 2.0V$	BSX19	10	-	-	
		BSX20	20	-	-	
f_T	Transition frequency					
	$I_C = 10mA$, $V_{CE} = 10V$	BSX19	400	500	-	Mc/s
		BSX20	500	600	-	Mc/s

*These are the characteristics which are recommended for acceptance testing purposes.

			Min.	Typ.	Max.	
c_{tc}	Collector capacitance					
	V_{CB}=5.0V, I_E=I_e=0,					
	f=1.0Mc/s		-	-	4.0	pF
c_{te}	Emitter capacitance					
	V_{EB}=1.0V, I_C=I_c=0,					
	f=1.0Mc/s		-	-	4.5	pF
Switching characteristics						
t_{on}	Turn-on time (see Fig.1)					
	I_C=10mA, I_B=3.0mA					
	from V_{BE}=-1.5V		-	-	12	ns
	I_C=100mA, I_B=40mA					
	from V_{BE}=-2.25V		-	-	7.0	ns
t_{off}	Turn-off time (see Fig.1)					
	I_C=10mA, I_B=3.0mA,					
	I_{BM}=-1.5mA	BSX19	-	-	15	ns
		BSX20	-	-	18	ns
	I_C=100mA, I_B=40mA,					
	I_{BM}=-20mA	BSX19	-	-	18	ns
		BSX20	-	-	21	ns

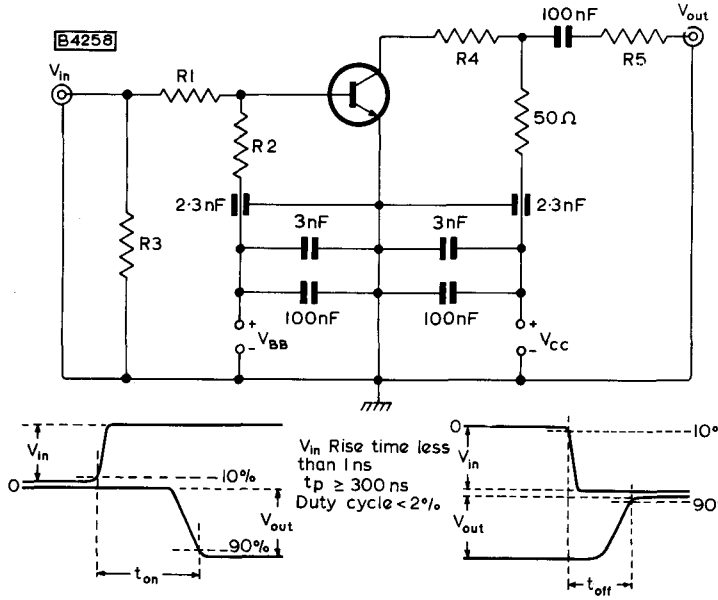


Fig.1

Circuit conditions:

I_C (mA)	I_B (mA)	$-I_{BM}$ (mA)	V_{CC} (V)	$R_1 = R_2$ (kΩ)	R_3 (Ω)	R_4 (Ω)	R_5 (kΩ)
10	3.0	1.5	3.0	3.3	50	220	0
100	40	20	6.0	0.33	56	0	1.0

t_{on}			t_{off}	
V_{BB} (V)	V_{BE} (V)	V_{in} (V)	V_{BB} (V)	V_{in} (V)
-3.0	-1.5	15	12	-15
-4.5	-2.25	20	15.3	-20

Note: $-I_{BM}$ is the reverse current that can flow during switching-off. The indicated $-I_{BM}$ is determined and limited by the applied cut-off voltage and series resistance.

			Min.	Typ.	Max.	
t_s	Storage time (see fig.2)					
	$I_C = I_B = -I_{BM} = 10mA$	BSX19	-	5.0	10	ns
		BSX20	-	6.0	13	ns

Storage time test circuit

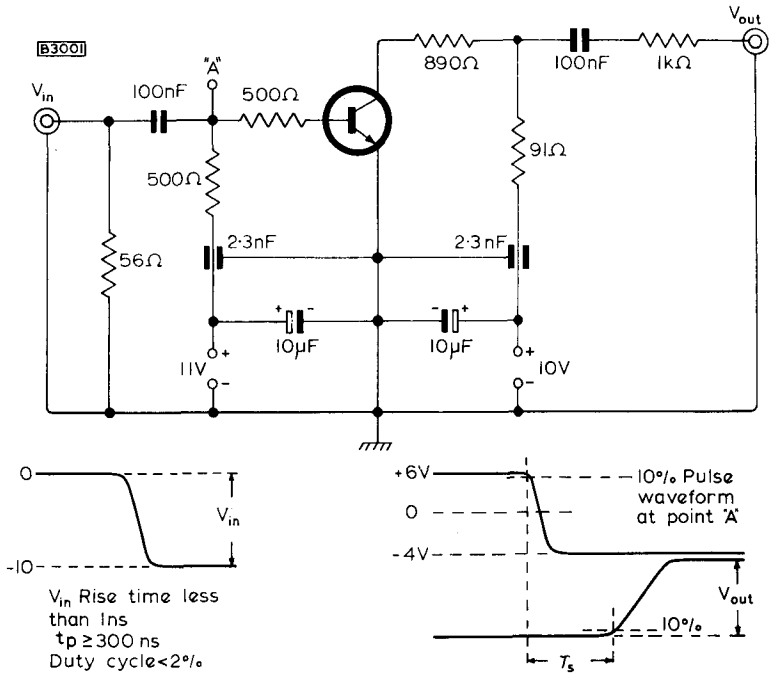
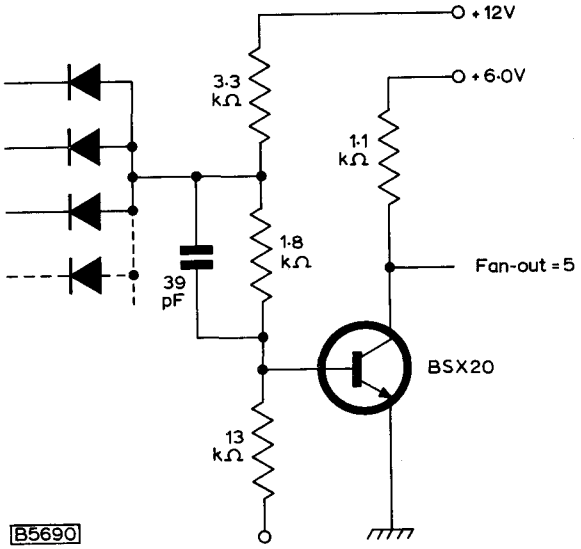


Fig. 2

TYPICAL CIRCUIT USING BSX20

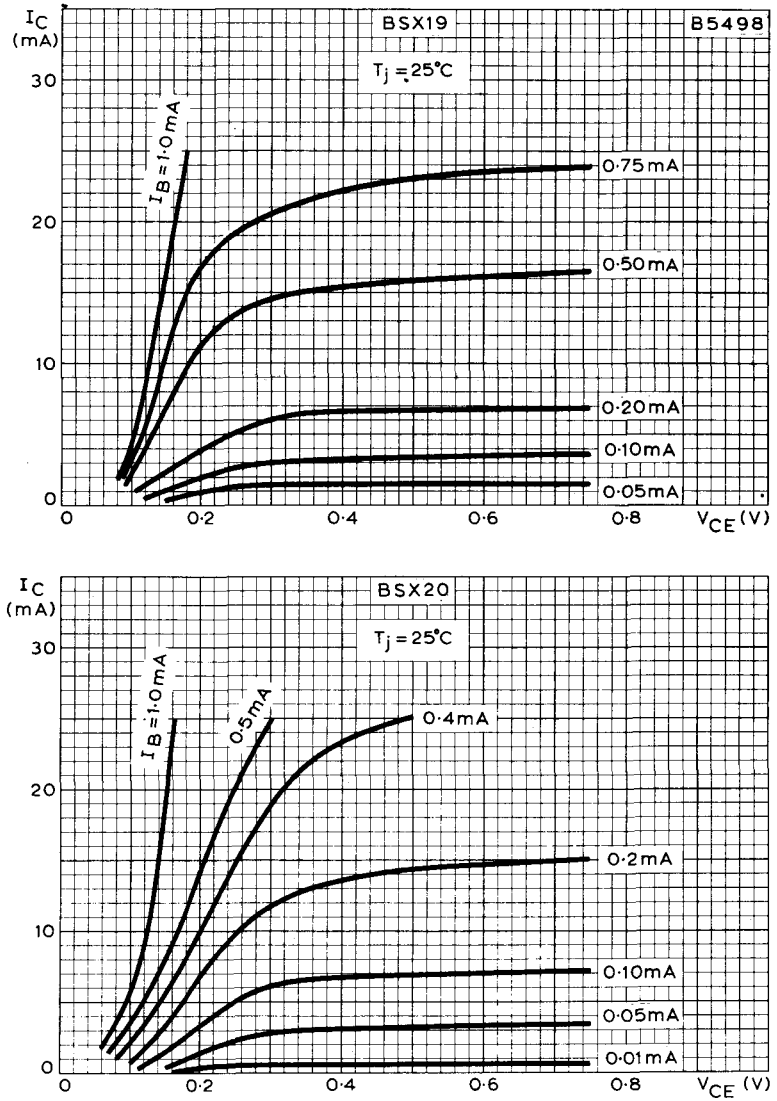
NAND gate (Diode-transistor logic)



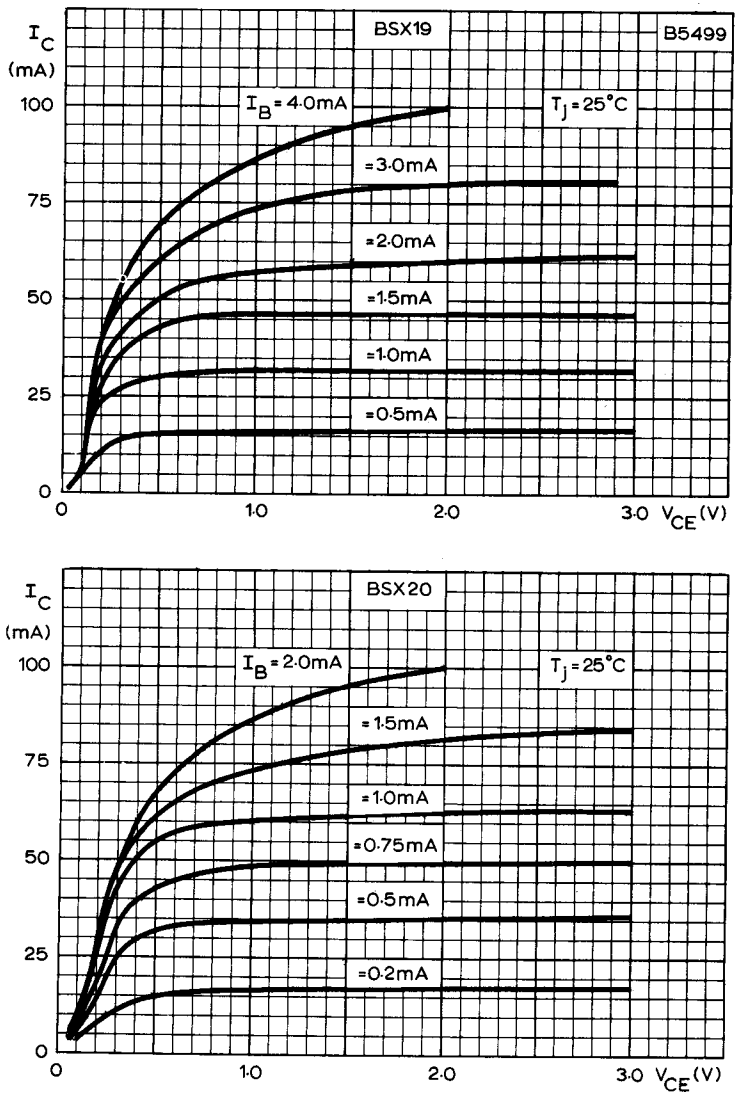
Typical delay time per stage t_d = 15ns, when 'fan-in' = 5

NOTE

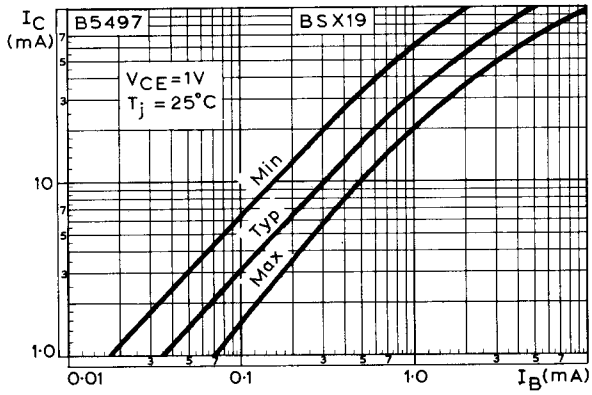
Fan-out = 5 means that the circuit may be loaded by a maximum of five circuits, each presenting a load identical to that of one input branch of the input circuit itself.

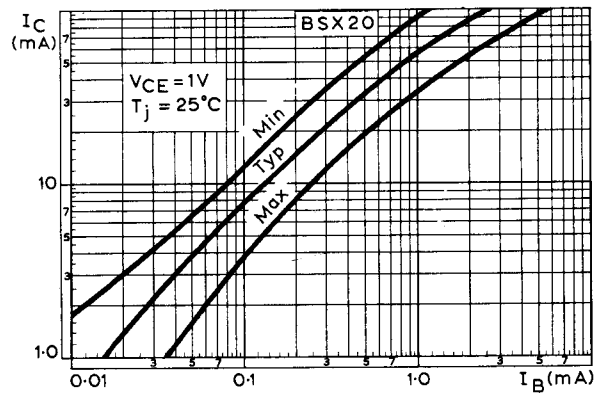


TYPICAL OUTPUT CHARACTERISTICS. $T_j = 25^{\circ}C$

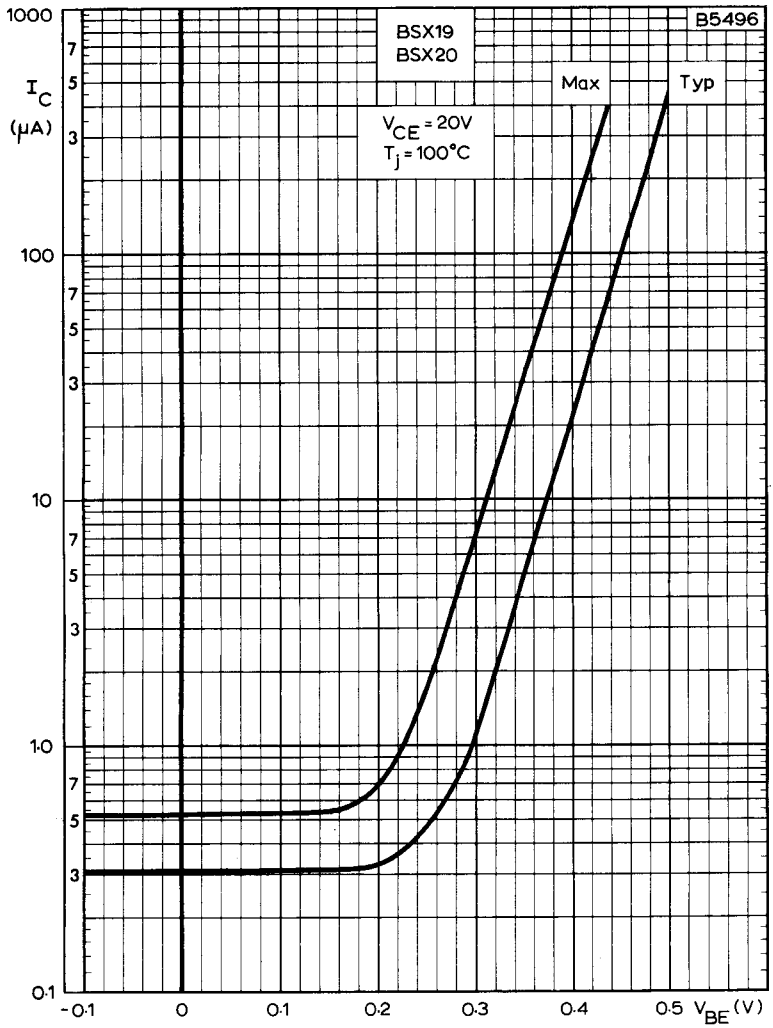


TYPICAL OUTPUT CHARACTERISTICS. $T_j = 25^{\circ}C$

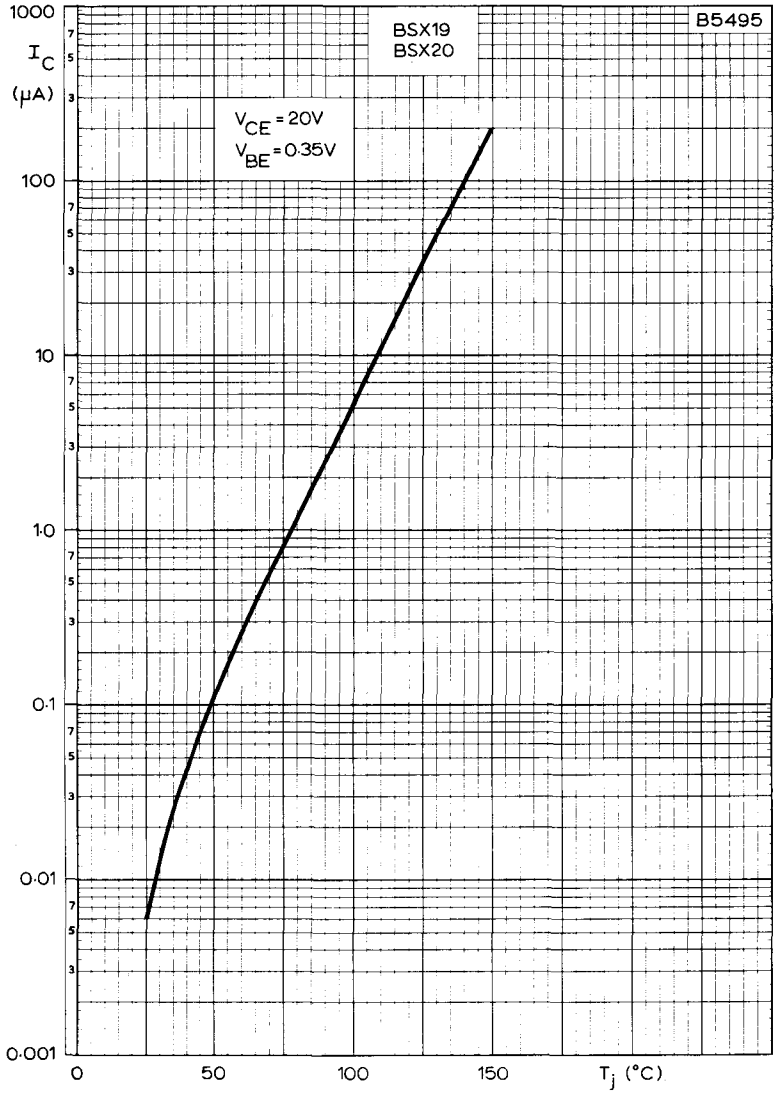




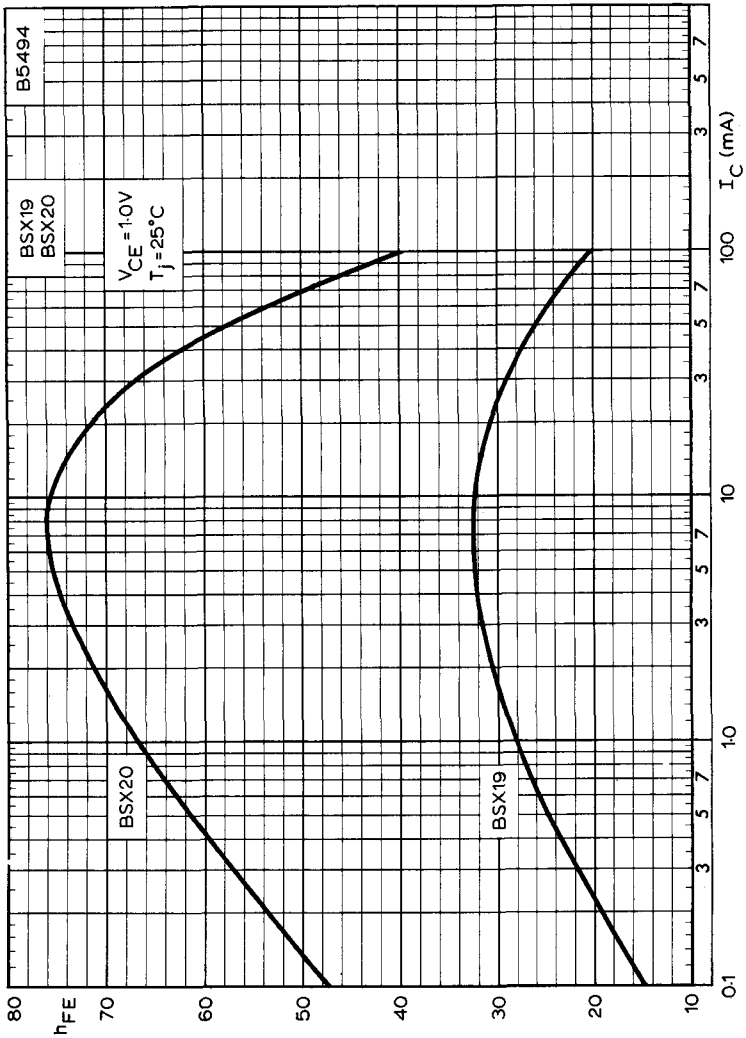
COLLECTOR CURRENT PLOTTED AGAINST BASE CURRENT



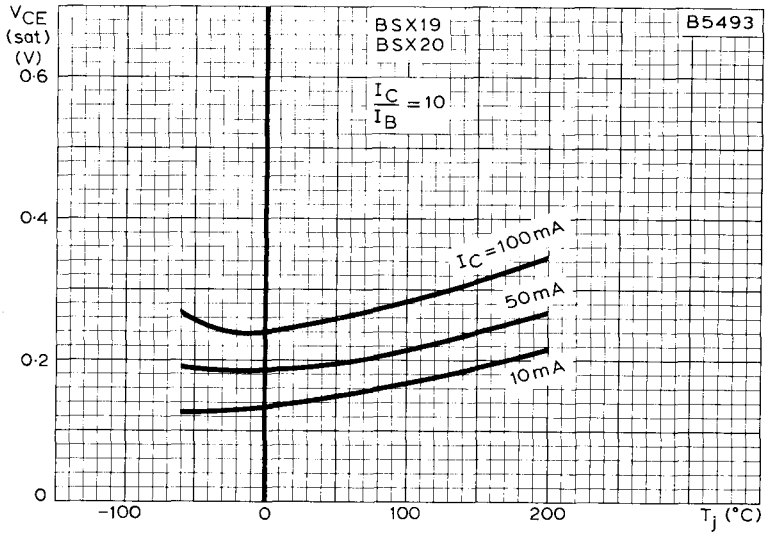
COLLECTOR CURRENT PLOTTED AGAINST BASE-EMITTER VOLTAGE

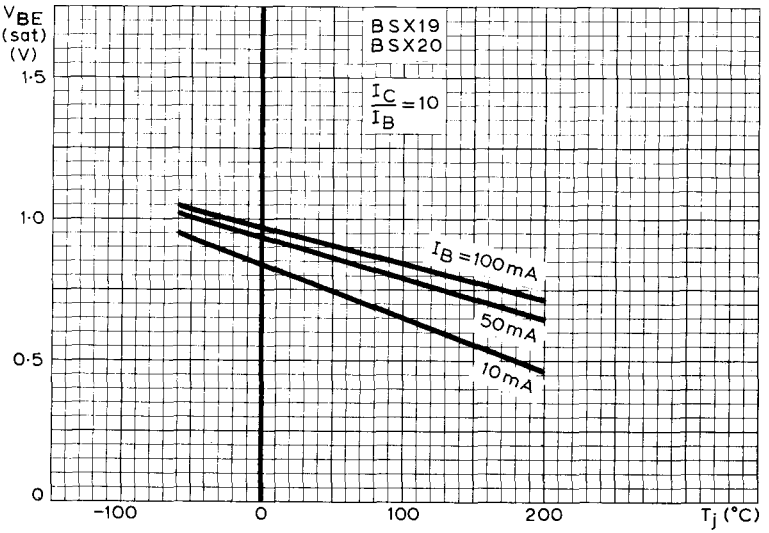


TYPICAL COLLECTOR CURRENT PLOTTED AGAINST JUNCTION TEMPERATURE

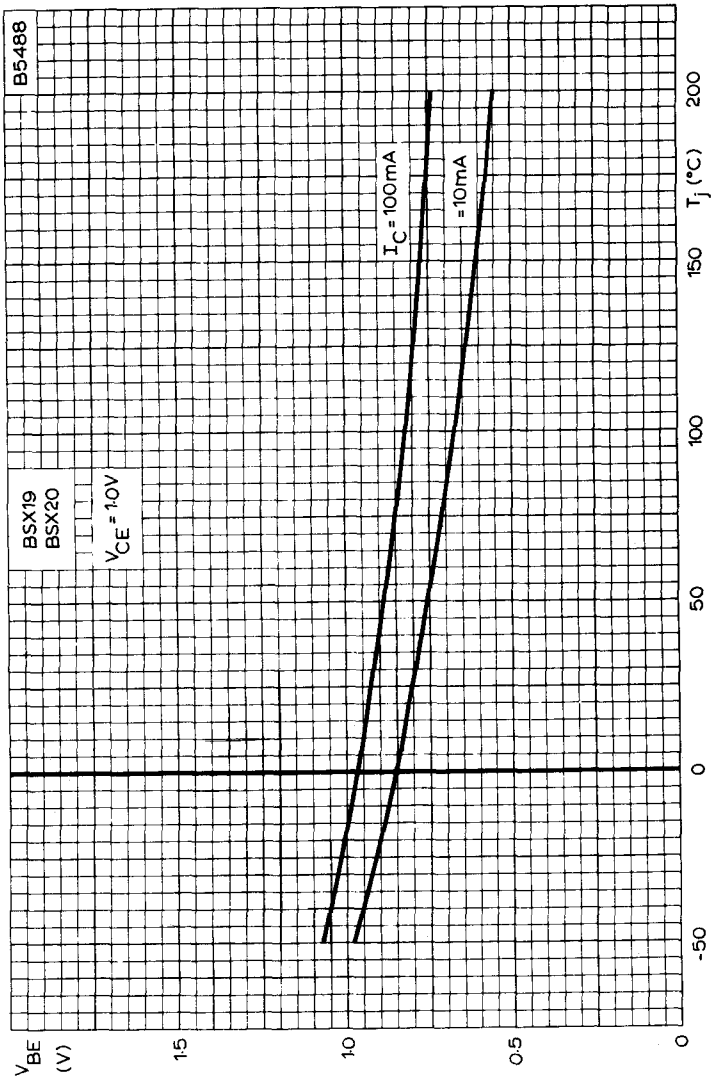


TYPICAL STATIC FORWARD CURRENT TRANSFER RATIO PLOTTED AGAINST COLLECTOR CURRENT

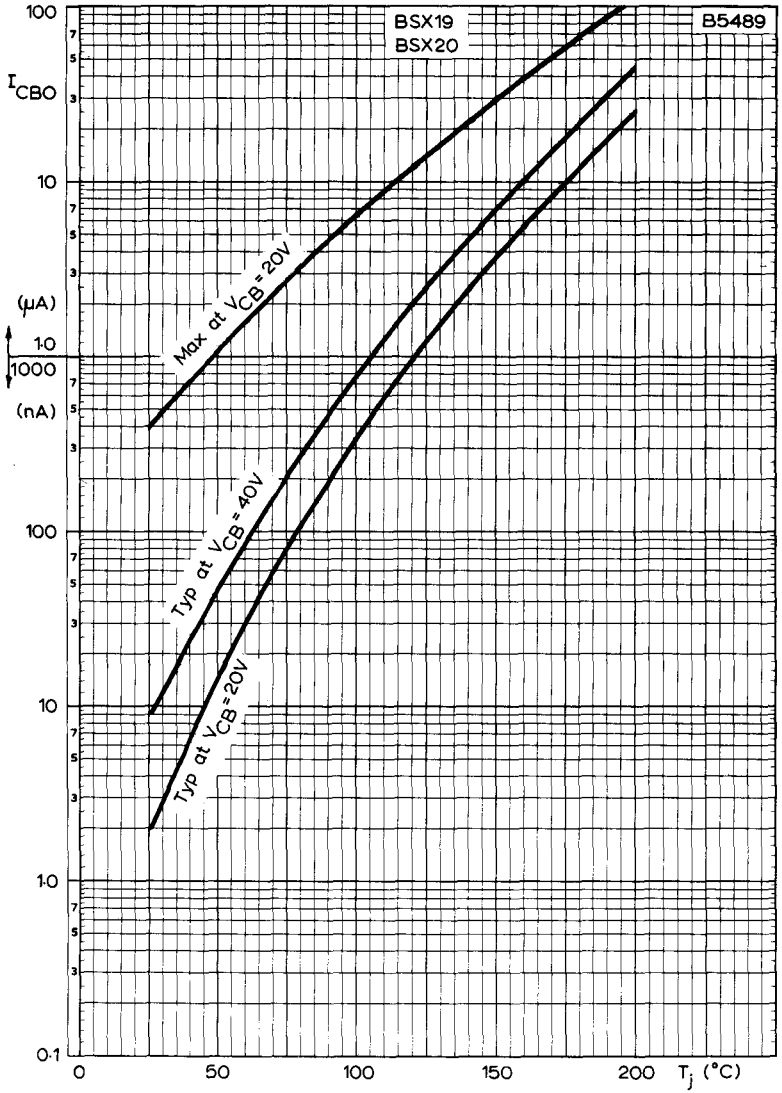




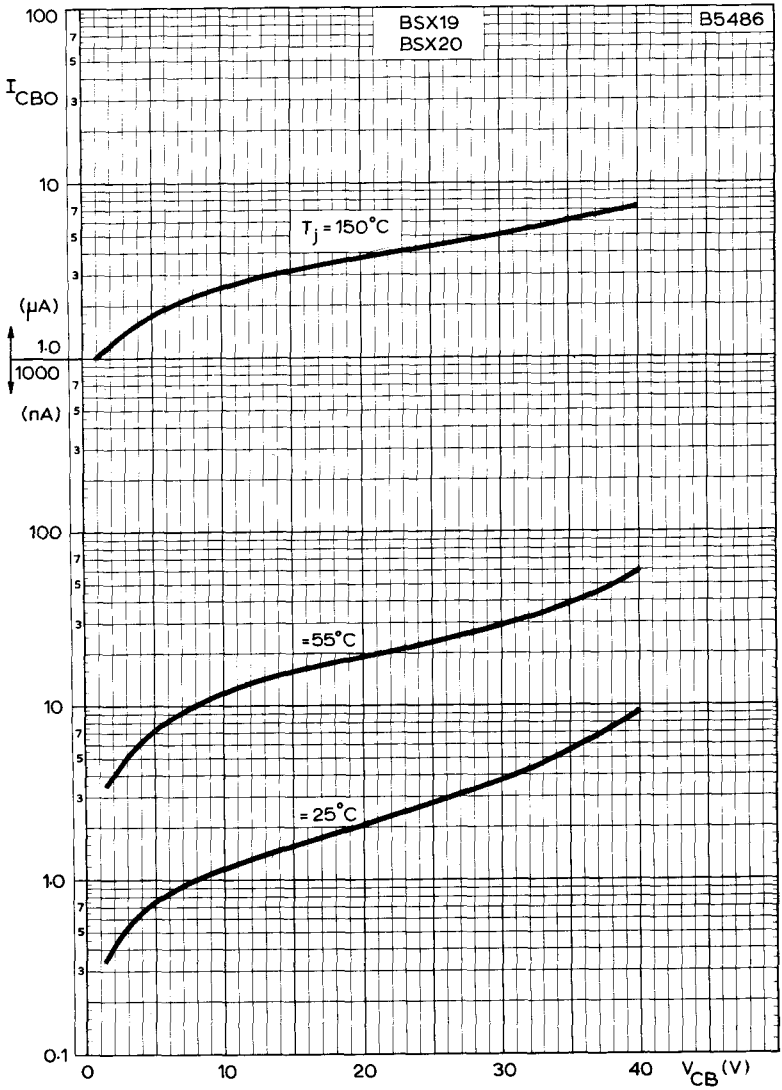
TYPICAL COLLECTOR-EMITTER SATURATION AND BASE-EMITTER SATURATION VOLTAGES PLOTTED AGAINST JUNCTION TEMPERATURE.



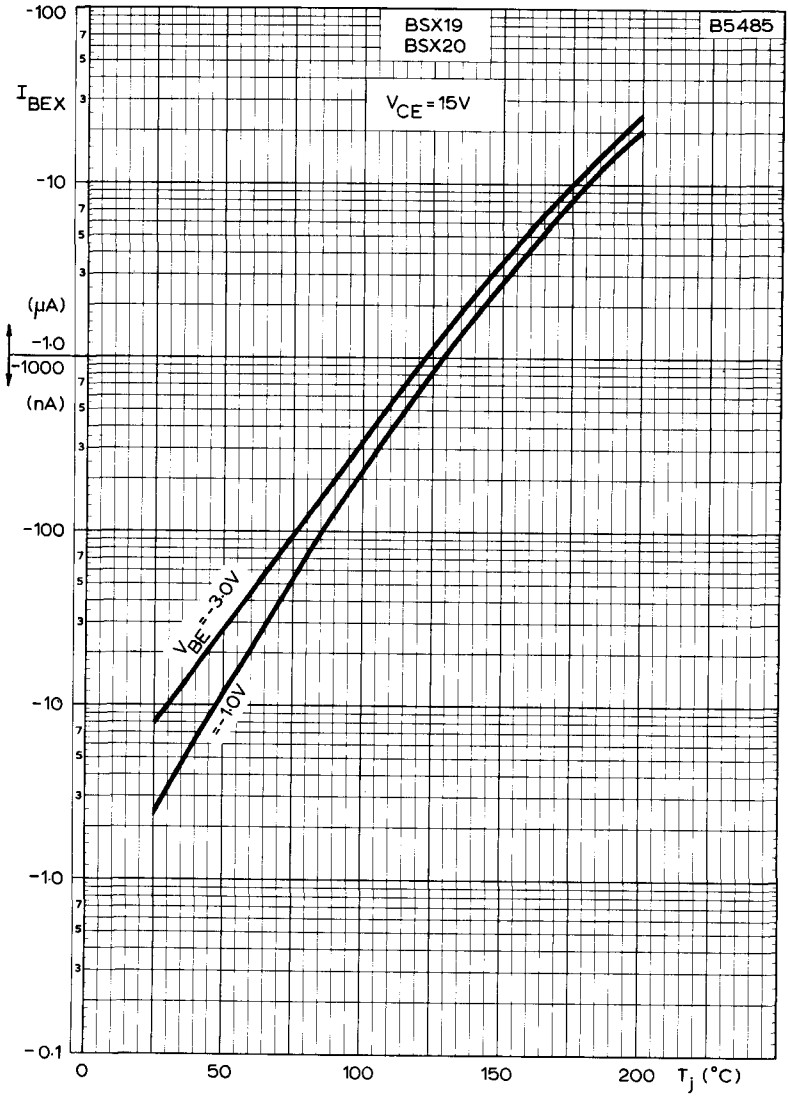
TYPICAL BASE-EMITTER VOLTAGE PLOTTED AGAINST JUNCTION TEMPERATURE



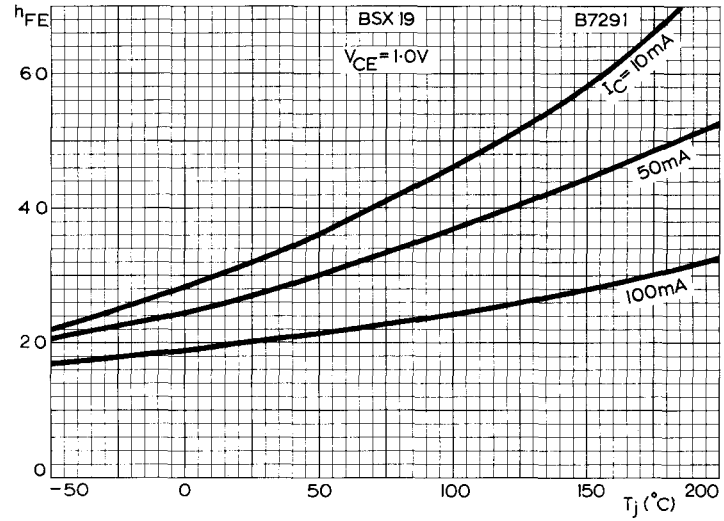
COLLECTOR CUT-OFF CURRENT PLOTTED AGAINST JUNCTION TEMPERATURE

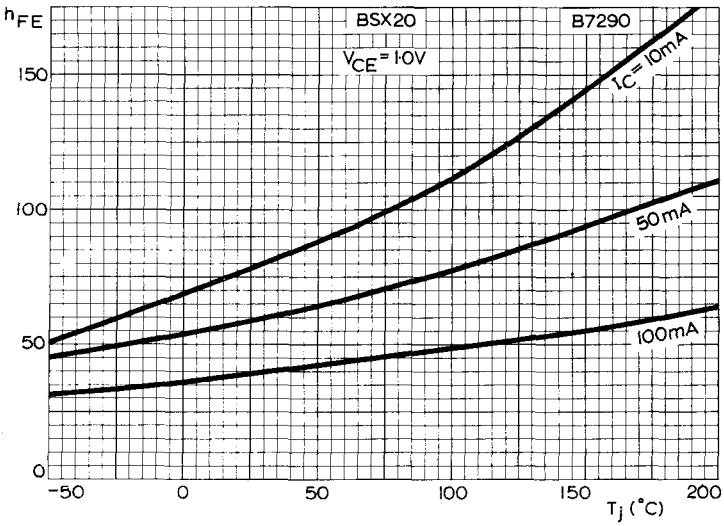


TYPICAL COLLECTOR CUT-OFF CURRENT PLOTTED AGAINST COLLECTOR-BASE VOLTAGE

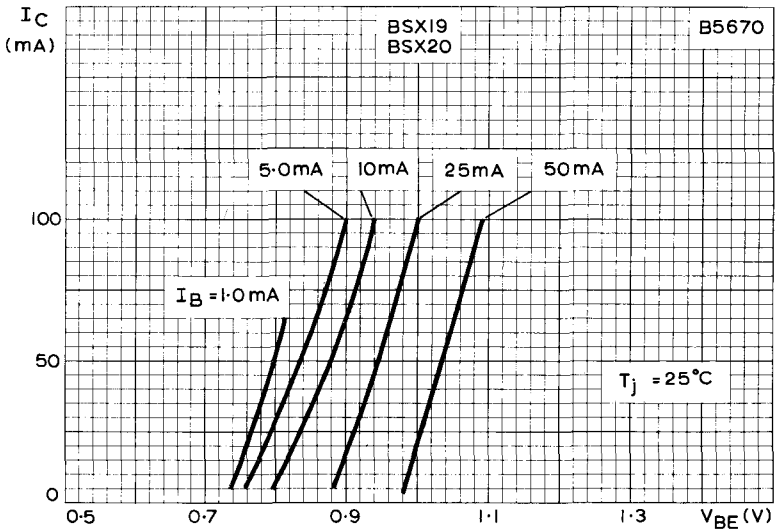


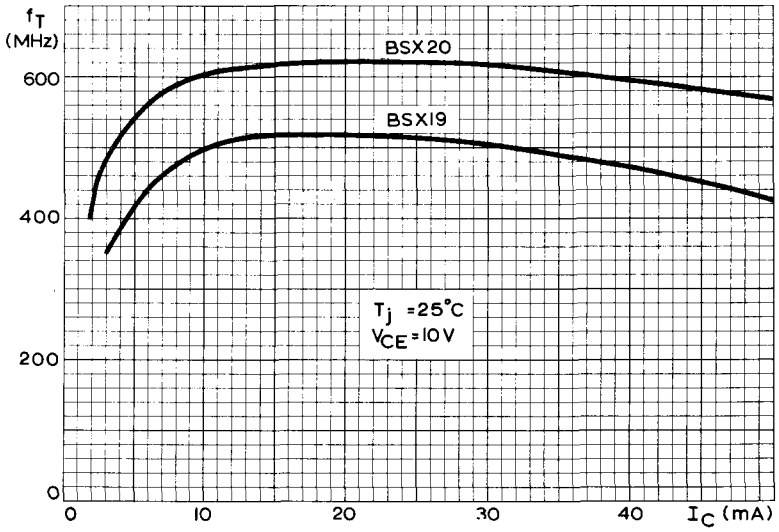
TYPICAL BASE-EMITTER CUT-OFF CURRENT PLOTTED AGAINST JUNCTION TEMPERATURE



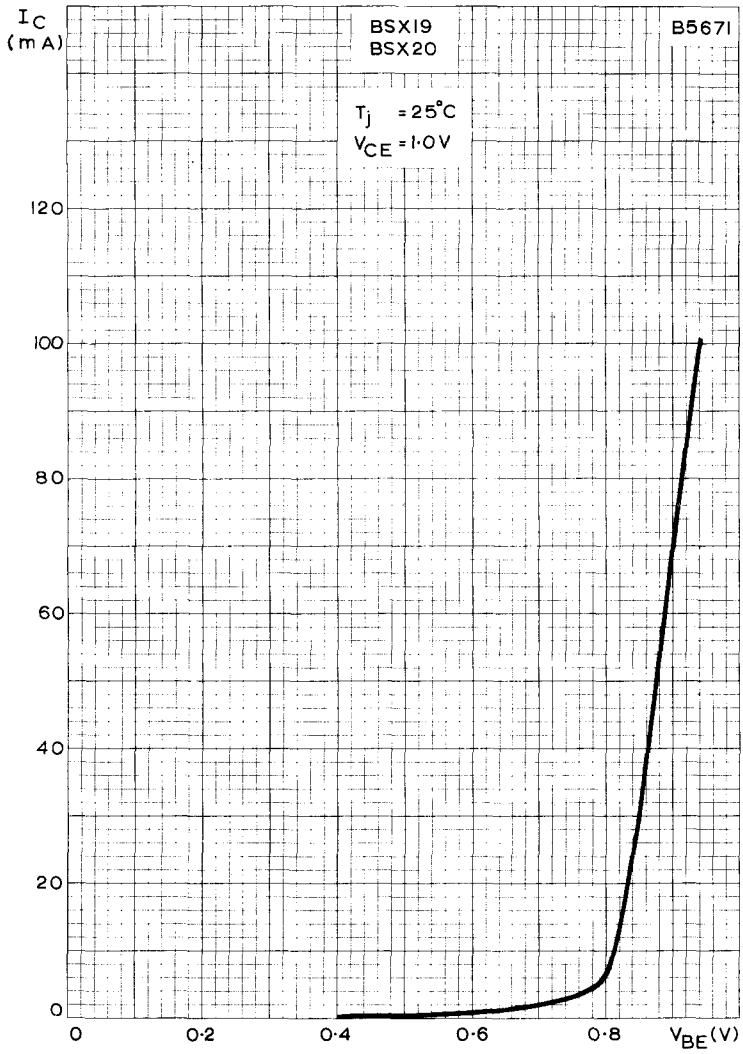


TYPICAL VARIATION OF STATIC FORWARD CURRENT TRANSFER RATIO WITH JUNCTION TEMPERATURE

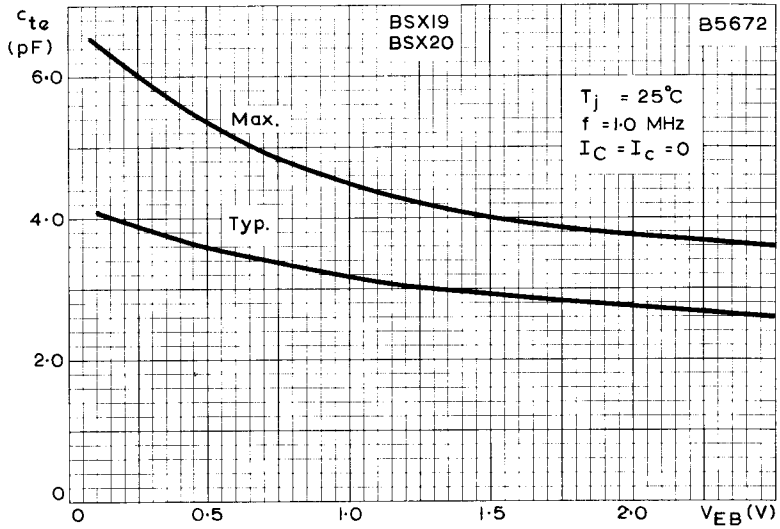


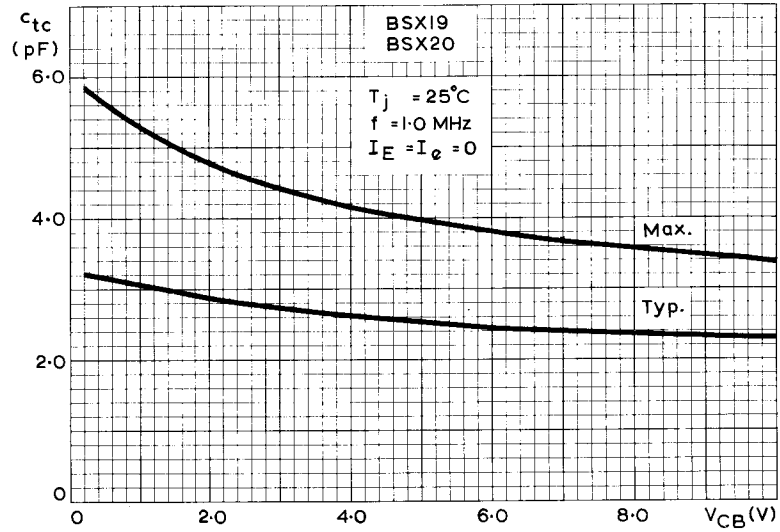


TYPICAL COLLECTOR CURRENT PLOTTED AGAINST BASE - EMITTER VOLTAGE
TYPICAL TRANSITION FREQUENCY PLOTTED AGAINST COLLECTOR CURRENT



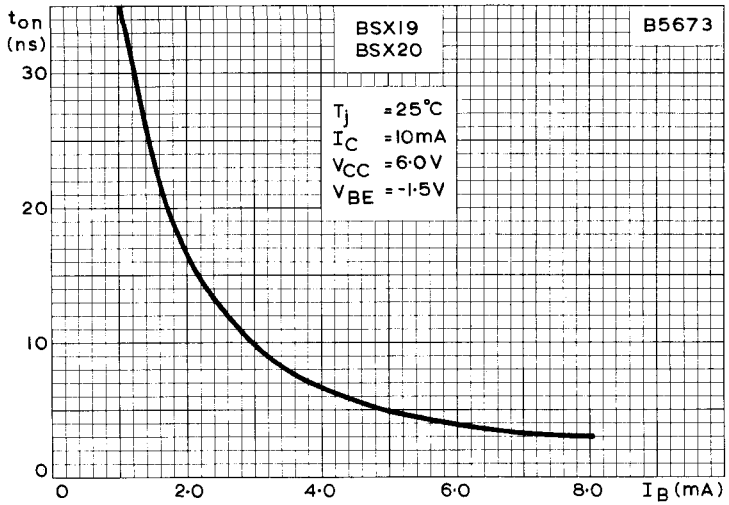
TYPICAL COLLECTOR CURRENT PLOTTED AGAINST BASE-EMITTER VOLTAGE

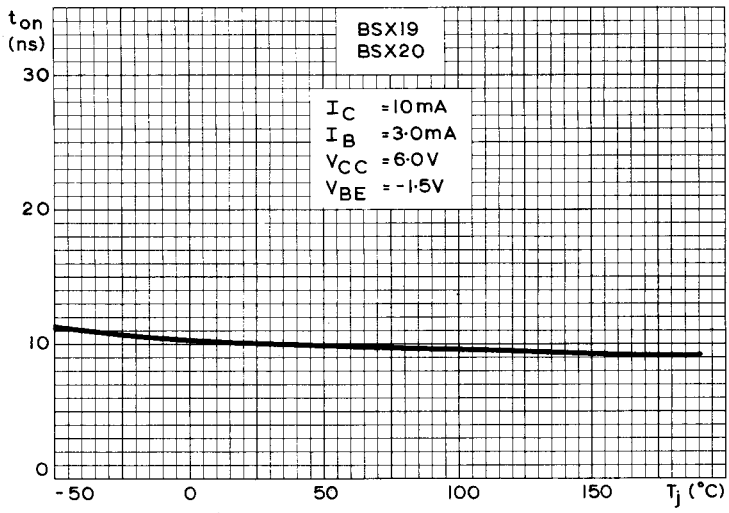




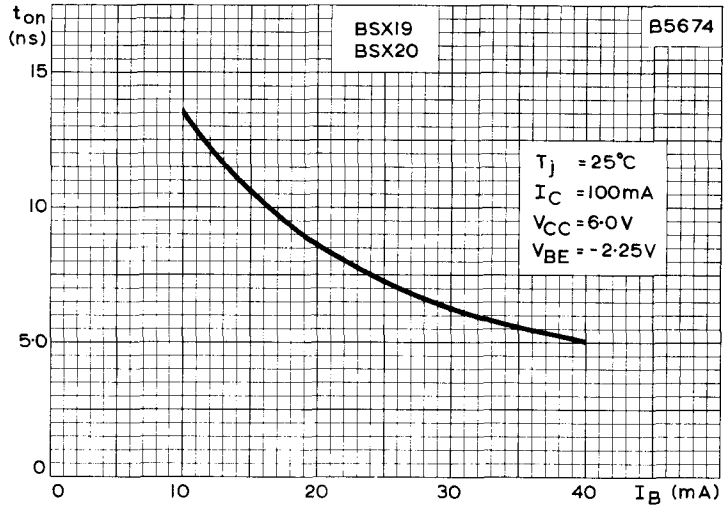
EMITTER CAPACITANCE PLOTTED AGAINST EMITTER-BASE VOLTAGE

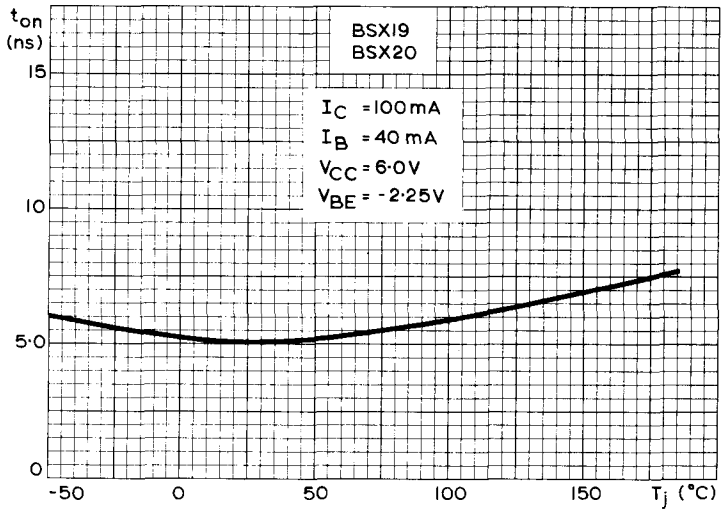
COLLECTOR CAPACITANCE PLOTTED AGAINST COLLECTOR-BASE VOLTAGE



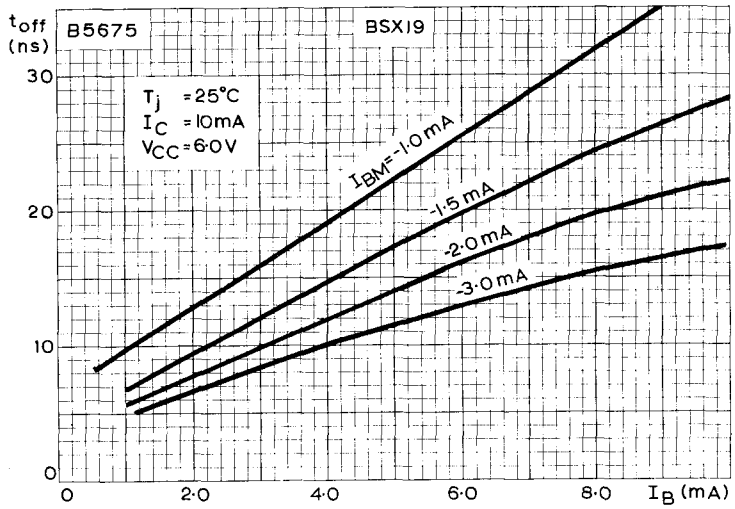


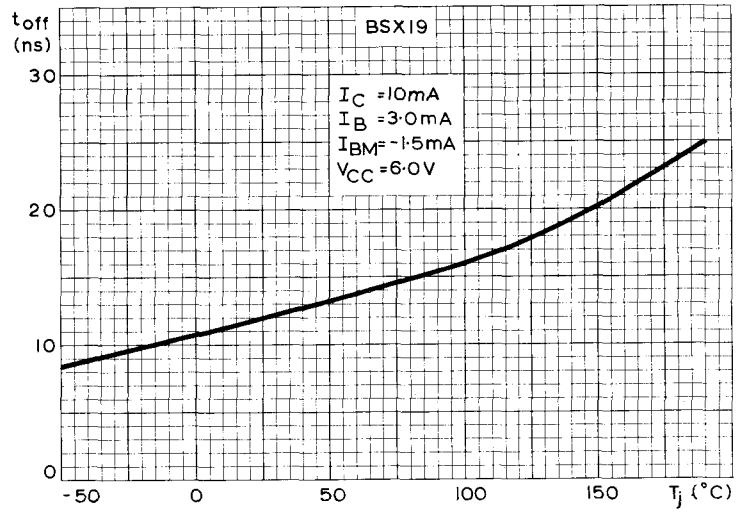
TYPICAL TURN-ON TIME PLOTTED AGAINST BASE CURRENT
TYPICAL TURN-ON TIME PLOTTED AGAINST JUNCTION TEMPERATURE



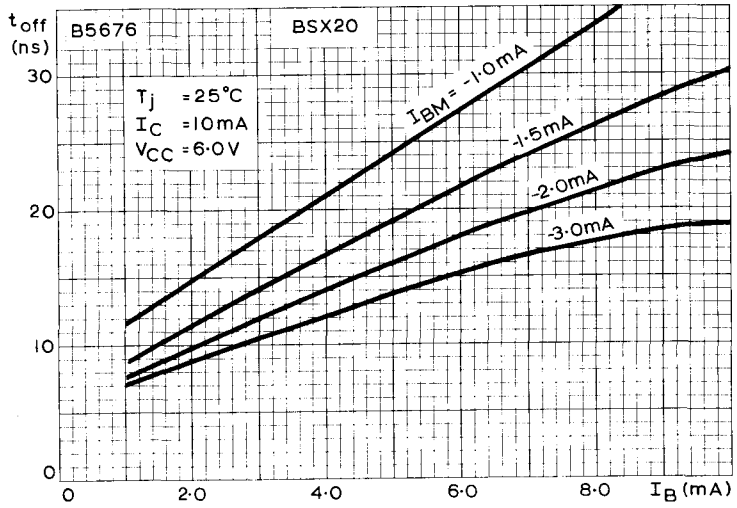


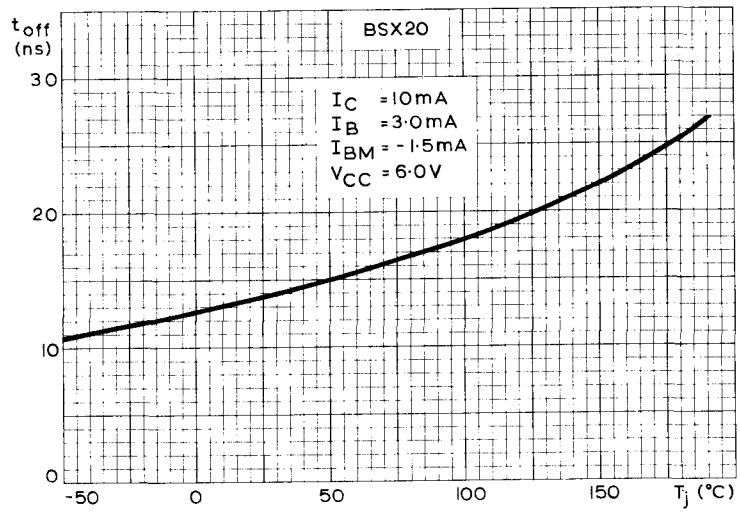
TYPICAL TURN-ON TIME PLOTTED AGAINST BASE CURRENT
TYPICAL TURN-ON TIME PLOTTED AGAINST JUNCTION TEMPERATURE



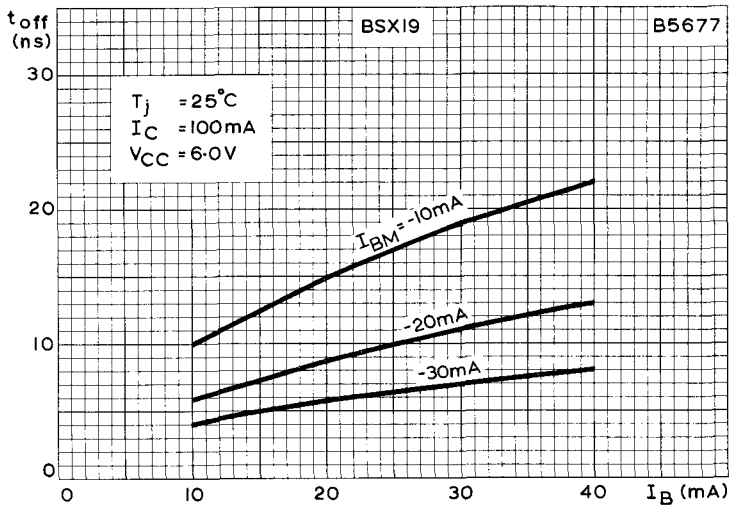


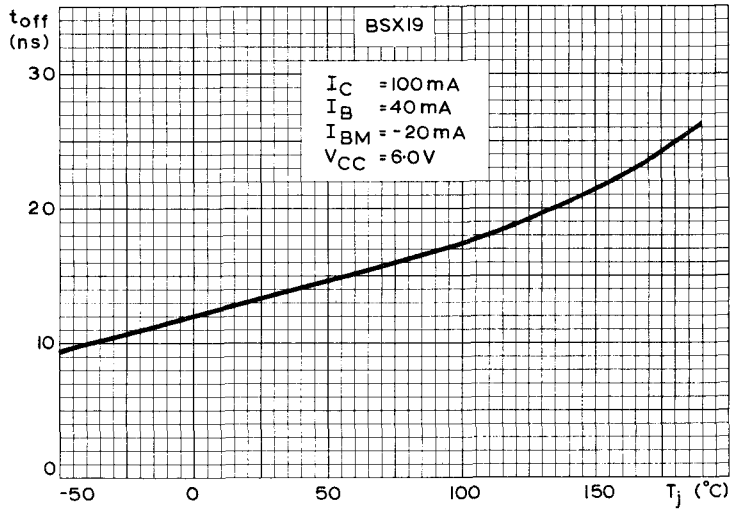
TYPICAL TURN-OFF TIME PLOTTED AGAINST BASE CURRENT
TYPICAL TURN-OFF TIME PLOTTED AGAINST JUNCTION TEMPERATURE



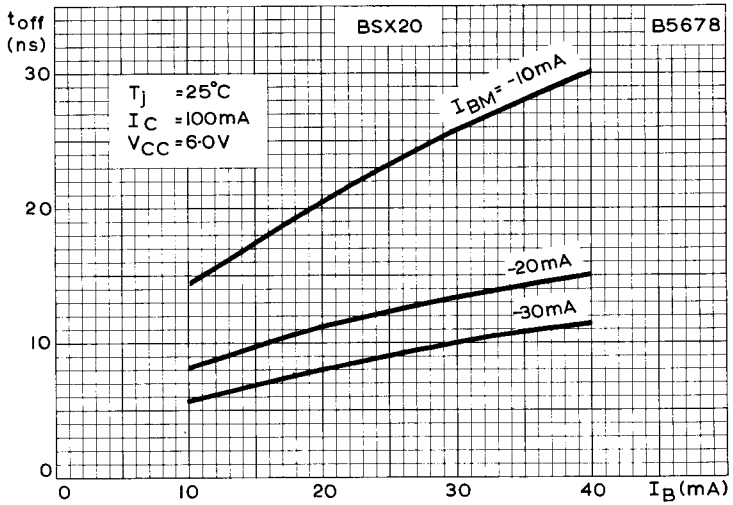


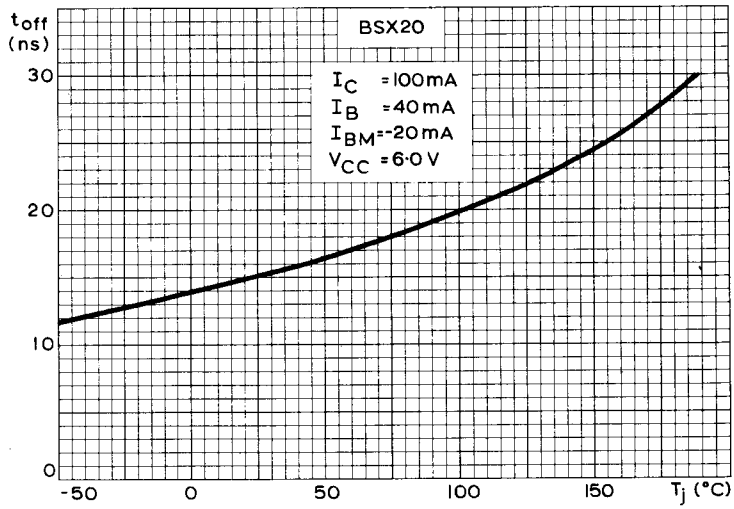
TYPICAL TURN-OFF TIME PLOTTED AGAINST BASE CURRENT
TYPICAL TURN-OFF TIME PLOTTED AGAINST JUNCTION TEMPERATURE



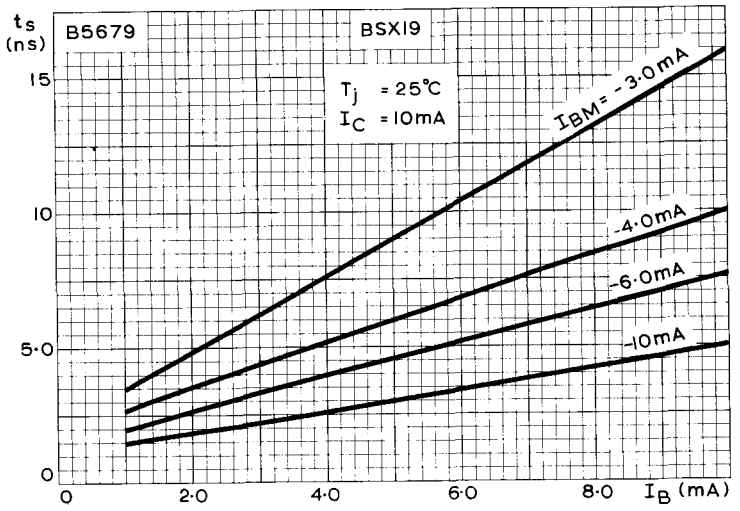


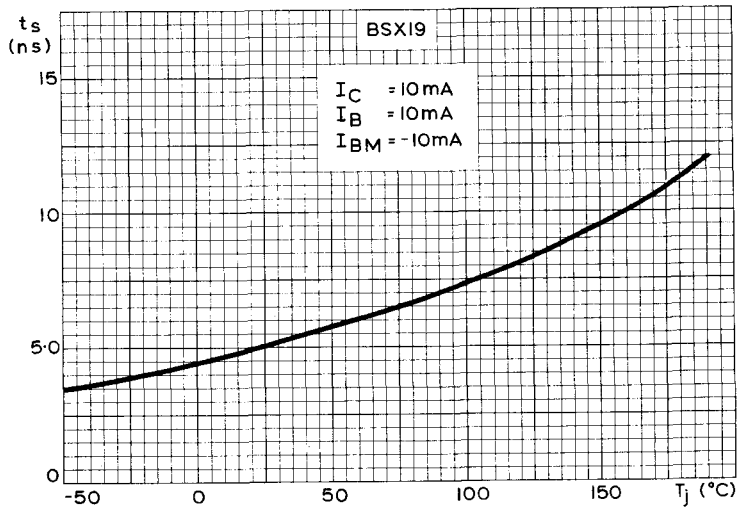
TYPICAL TURN-OFF TIME PLOTTED AGAINST BASE CURRENT
TYPICAL TURN-OFF TIME PLOTTED AGAINST JUNCTION TEMPERATURE



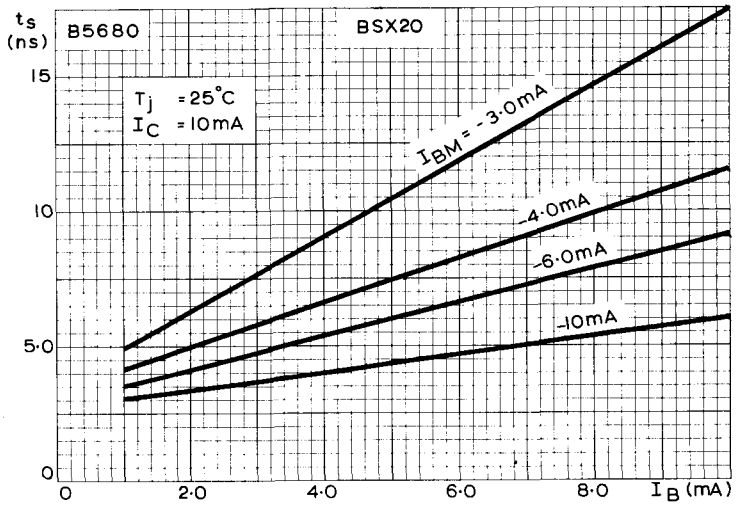


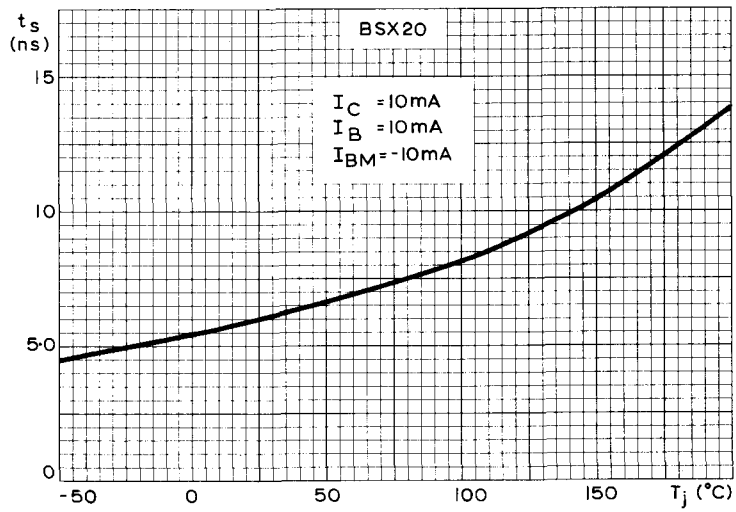
TYPICAL TURN-OFF TIME PLOTTED AGAINST BASE CURRENT
TYPICAL TURN-OFF TIME PLOTTED AGAINST JUNCTION TEMPERATURE





TYPICAL STORAGE TIME PLOTTED AGAINST BASE CURRENT
TYPICAL STORAGE TIME PLOTTED AGAINST JUNCTION TEMPERATURE





TYPICAL STORAGE TIME PLOTTED AGAINST BASE CURRENT
TYPICAL STORAGE TIME PLOTTED AGAINST JUNCTION TEMPERATURE

N-P-N SILICON PLANAR TRANSISTOR

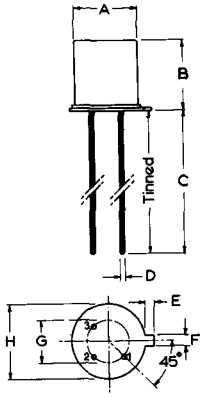
BSX21

N-P-N silicon planar transistor for use in general industrial applications and as a driver with numerical indicator tubes. TO-18 construction with collector connected to the envelope.

QUICK REFERENCE DATA		
V_{CB} max. ($I_E = 0$)	+120	V
V_{CEO} max.	+80	V
I_{CM} max.	50	mA
P_{tot} max. ($T_{amb} = 25^oC$)	300	mW
T_j max.	175	^oC
h_{FE} min. ($I_C = 4.0mA$, $V_{CE} = +3.0V$)	20	
f_T min. ($I_C = 4.0mA$, $V_{CE} = +10V$)	60	MHz

OUTLINE AND DIMENSIONS

Conforming to B.S. 3934 SO-12A/SB3-6A
J.E.D.E.C. TO-18



	Millimetres		
	Min.	Nom.	Max.
A	-	-	4.8
B	-	-	5.3
C	12.7	-	-
D	-	-	0.48
E	-	1.0	-
F	-	1.05	-
G	-	2.54	-
H	5.3	5.55	5.8

Connections
1. Emitter
2. Base
3. Collector connected to envelope

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

†V_{CBO} max. ($I_E = 0$)	+120	V
†V_{CEO} max. ($I_B = 0$)	+80	V
V_{EBO} max. ($I_C = 0$)	+5.0	V
‡I_{CM} max.	50	mA
*$I_{C(AV)}$ max.	50	mA
I_{EM} max.	50	mA
*$I_{E(AV)}$ max.	50	mA
P_{tot} max. ($T_{amb} = 25^oC$)	300	mW

Temperature

T_{stg} min.	-65	^oC
T_{stg} max.	175	^oC
T_j max.	175	^oC

THERMAL CHARACTERISTICS

$R_{th(j-amb)}$ in free air	0.5	degC/mW
$R_{th(j-case)}$	0.15	degC/mW

*Averaged over any 20ms period.

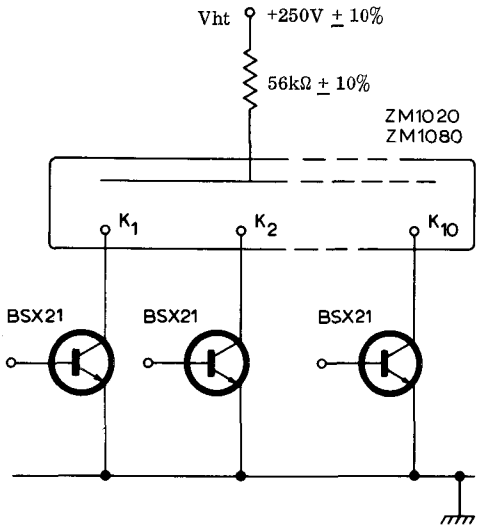
†The BSX21 may be operated in the breakdown region up to $V_{CE} = +160V$, provided that $P_{tot} \leq 100mW$ at $T_{amb} \leq 85^oC$.

‡The transistor can withstand a capacitive load of 500pF, with V_{CE} max. = 150V during switch-on.

ELECTRICAL CHARACTERISTICS ($T_j = 25^oC$ unless otherwise stated)

		Min.	Typ.	Max.	
I_{CBO}	Collector cut-off current				
	$V_{CB} = +50V$, $I_E = 0$	-	0.5	-	μA
	$V_{CB} = +120V$, $I_E = 0$	-	-	40	μA
I_{EBO}	Emitter cut-off current				
	$V_{EB} = +3.0V$, $I_C = 0$	-	0.1	-	μA
$V_{CE(sat)}$	Collector-emitter saturation voltage				
	$I_C = 1.0mA$, $I_B = 100\mu A$	-	+250	-	mV
	$I_C = 10mA$, $I_B = 1.0mA$	-	+1.8	-	V
$V_{BE(sat)}$	Base-emitter saturation voltage				
	$I_C = 1.0mA$, $I_B = 100\mu A$	-	+670	-	mV
	$I_C = 10mA$, $I_B = 1.0mA$	-	+900	-	mV
$V_{CE(sust)}$	Collector-emitter sustaining voltage				
	$I_C = 4.0mA$, $I_B = 0$	+80	-	-	V
V_{BE}	Base-emitter voltage				
	$I_C = 4.0mA$, $V_{CE} = +3.0V$	-	+700	+900	mV
h_{FE}	Static forward current transfer ratio				
	$I_C = 1.0mA$, $V_{CE} = +3.0V$	-	25	-	
	$I_C = 4.0mA$, $V_{CE} = +3.0V$	20	40	-	
	$I_C = 10mA$, $V_{CE} = +3.0V$	-	32	-	
	$I_C = 20mA$, $V_{CE} = +3.0V$	-	7	-	
C_{Tc}	Collector capacitance				
	$I_E = I_e = 0$, $V_{CB} = +10V$,				
	$f = 1.0MHz$	-	3.6	-	pF
C_{Te}	Emitter capacitance				
	$I_C = I_c = 0$, $V_{EB} = +1.0V$				
	$f = 1.0MHz$	-	8.5	-	pF
f_T	Transition frequency				
	$I_C = 4.0mA$, $V_{CE} = +10V$	60	120	-	MHz

TYPICAL CIRCUIT

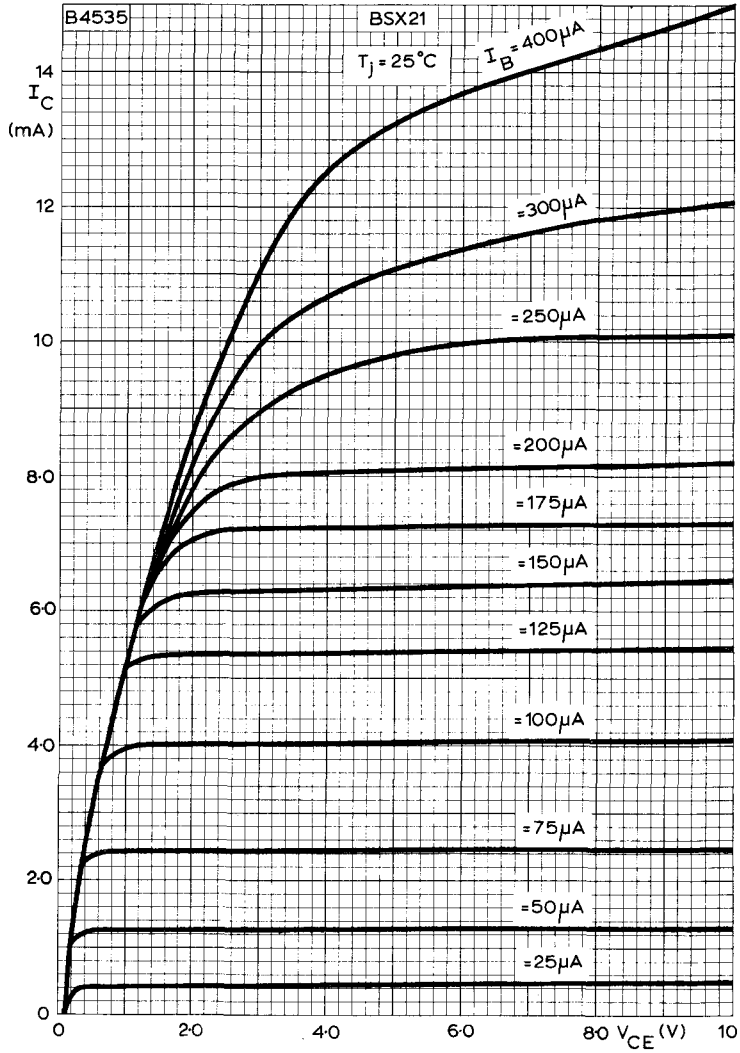


SOLDERING AND WIRING RECOMMENDATIONS

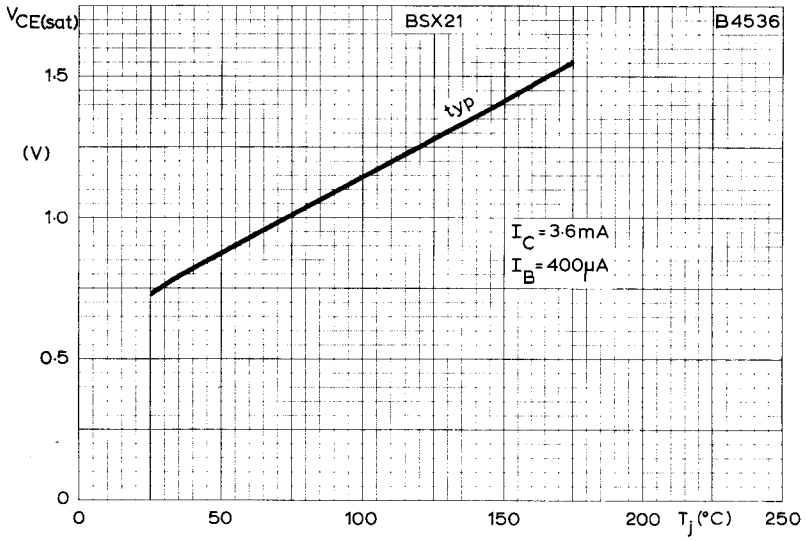
1. When using a soldering iron, transistors may be soldered directly into the circuit, but heat conducted to the junction should if possible be kept to a minimum by the use of a thermal shunt.

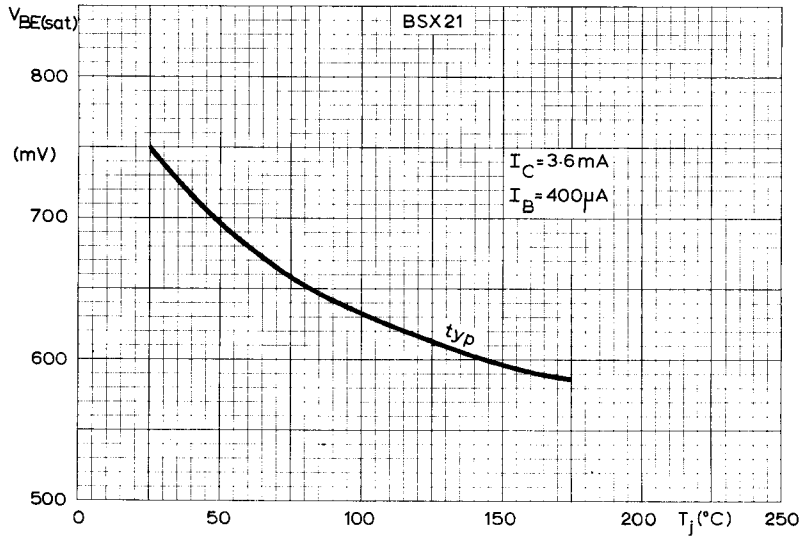
2. Transistors may be dip-soldered at a solder temperature of 245°C for a maximum soldering time of 5 seconds. The case temperature during dip-soldering must not at any time exceed the maximum storage temperature. These recommendations apply to a transistor mounted flush on a board having punched-through holes, or spaced at least 1.5mm above a board having plated-through holes.

3. Care should be taken not to bend the leads nearer than 1.5mm from the seal.

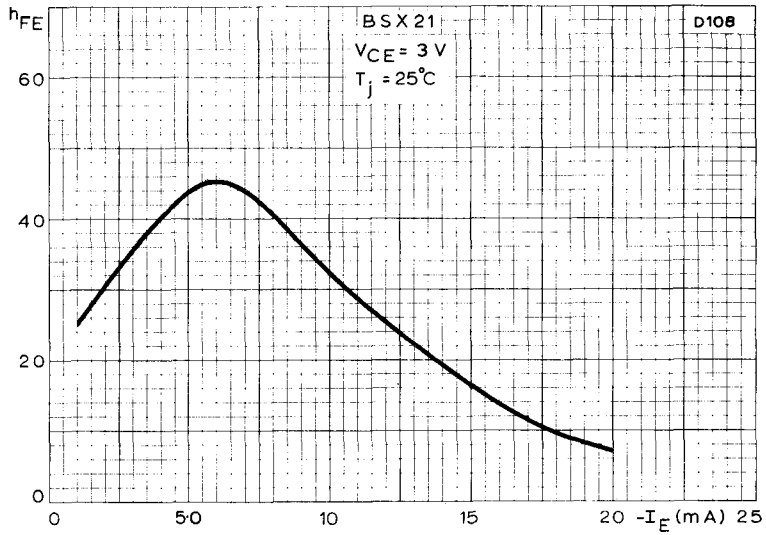


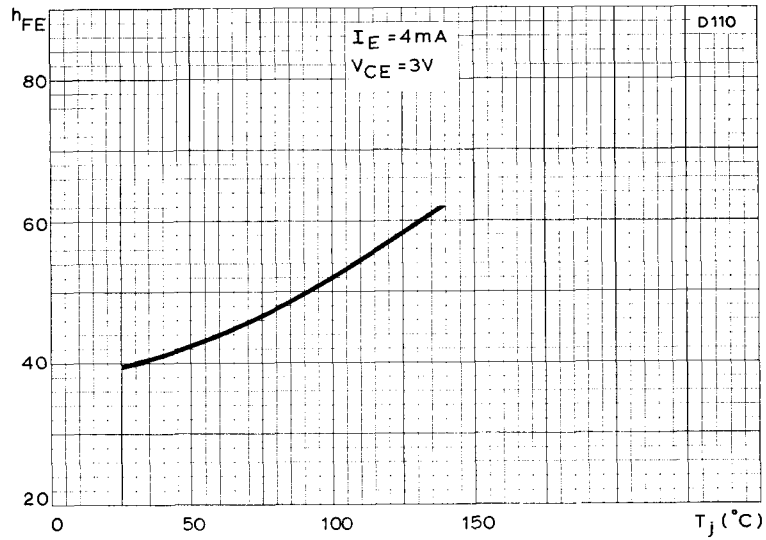
TYPICAL OUTPUT CHARACTERISTIC



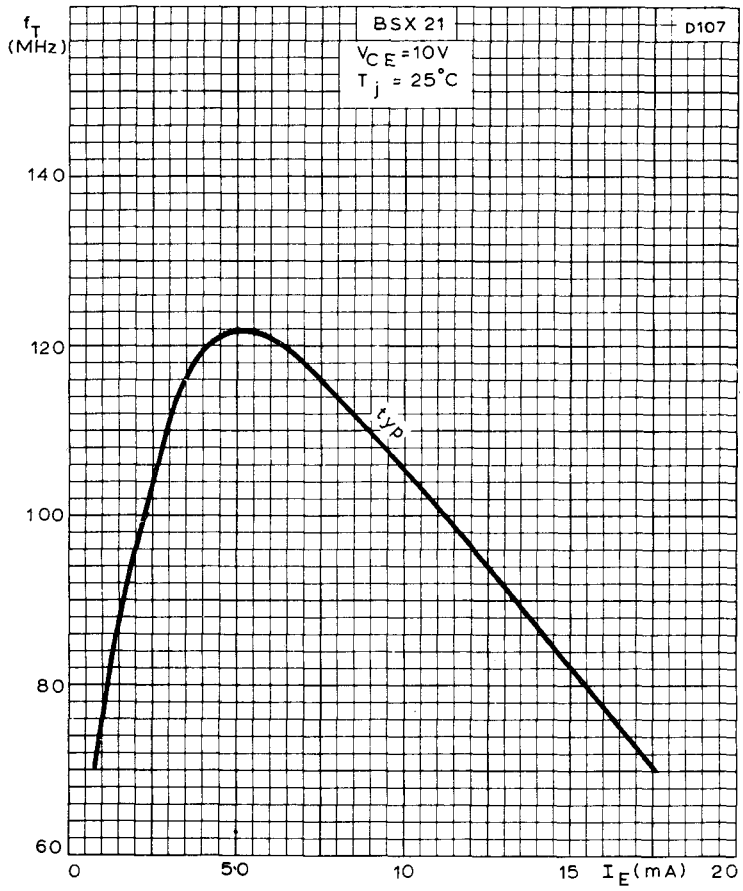


TYPICAL VARIATION OF COLLECTOR-EMITTER AND BASE-EMITTER SATURATION VOLTAGES WITH JUNCTION TEMPERATURE

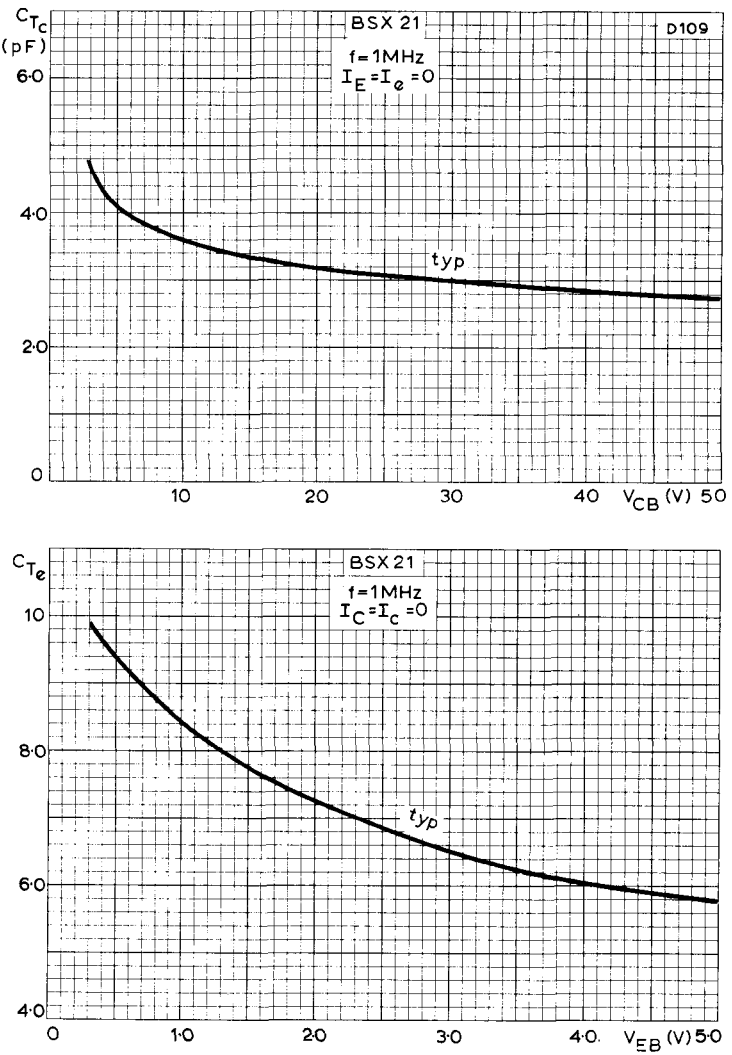




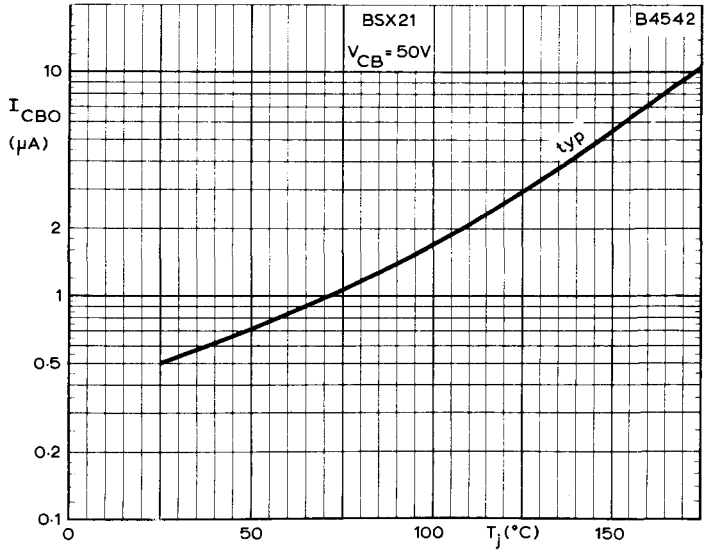
TYPICAL VARIATION OF STATIC FORWARD CURRENT TRANSFER RATIO WITH EMITTER CURRENT AND JUNCTION TEMPERATURE

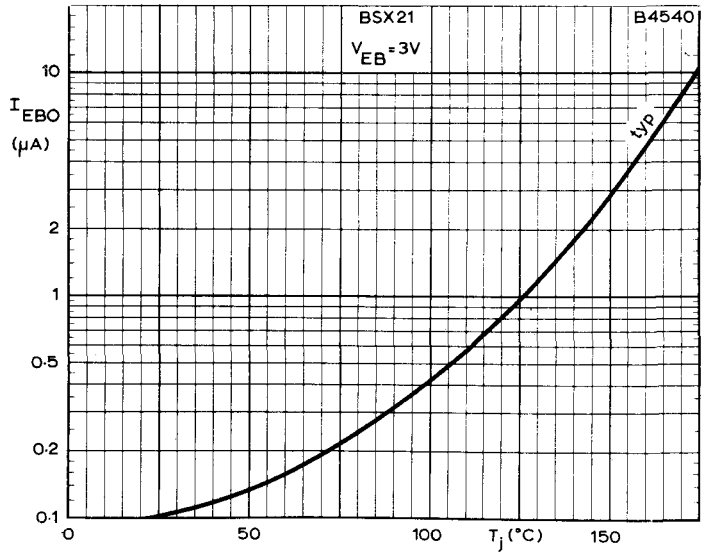


TRANSITION FREQUENCY PLOTTED AGAINST EMITTER CURRENT

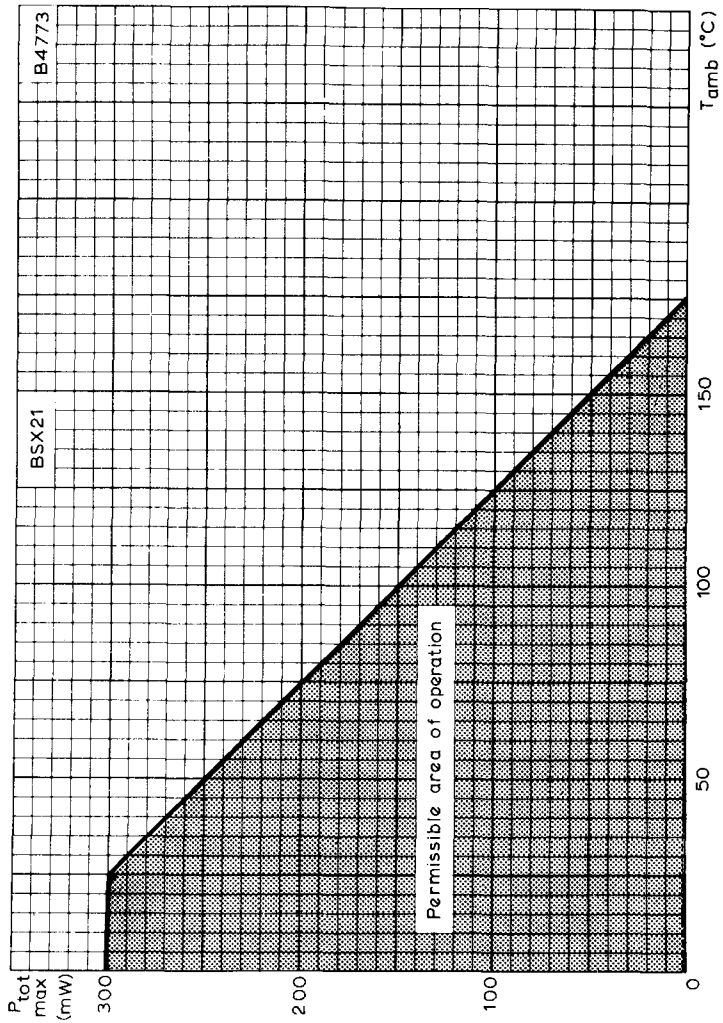


COLLECTOR CAPACITANCE PLOTTED AGAINST COLLECTOR-BASE VOLTAGE AND EMITTER CAPACITANCE PLOTTED AGAINST EMITTER-BASE VOLTAGE





TYPICAL VARIATION OF COLLECTOR-BASE AND EMITTER-BASE CUT-OFF CURRENTS WITH JUNCTION TEMPERATURE



MAXIMUM TOTAL DISSIPATION PLOTTED AGAINST AMBIENT TEMPERATURE

SILICON PLANAR EPITAXIAL N-P-N TRANSISTORS

BSX59
BSX60
BSX61

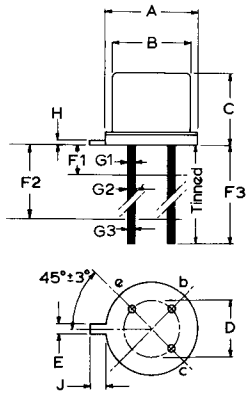
Silicon planar epitaxial n-p-n transistors intended for use in very high speed core driving applications

QUICK REFERENCE DATA	BSX59	BSX60	BSX61	
V_{CBO} max.	70	70	70	V
V_{CEO} max.	45	30	45	V
I_C max.	1.0	1.0	1.0	A
P_{tot} max. ($T_{amb}=25^oC$)	800	800	800	mW
T_j max.	200	200	200	^oC
h_{FE} ($I_C=500mA$, $V_{CE}=1.0V$)	25min.	30-90	25min.	
$V_{CE(sat)}$ max. ($I_C=500mA$, $I_B=50mA$)	0.5	0.5	0.7	V
t_{on} max. ($I_C=500mA$, $I_{Bon}=50mA$, $-V_{BEoff}=2.0V$)	35	40	50	ns
t_{off} max. ($I_C=500mA$, $I_{Bon}=-I_{Boff}=50mA$)	60	70	100	ns

Unless otherwise stated data is applicable to all types

OUTLINE AND DIMENSIONS

Conforming to B.S. 3934 SO-3/SB3-3A
J.E.D.E.C. TO-5



	Millimetres		
	Min.	Nom.	Max.
A	9.10	-	9.40
B	8.2	-	8.50
C	6.10	-	6.60
D	-	5.08	-
E	0.71	-	0.86
F1	-	-	0.51
F2	12.7	-	-
F3	38.1	-	41.3
G1	-	-	1.01
G2	0.41	-	0.48
G3	-	-	0.53
H	-	0.4	-
J	0.74	-	1.01

The collector is connected to the envelope

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{CBO} max.		70	V
V_{CEO} max.	BSX59	45	V
	BSX60	30	V
	BSX61	45	V
V_{EBO} max.		5.0	V
I_C max.		1.0	A
I_B max.		0.2	A
P_{tot} max. (T_{amb}=25°C)		800	mW

Temperature

T_{stg} min.	-65	°C
T_{stg} max.	200	°C
T_j max.	200	°C

THERMAL CHARACTERISTICS

$\Theta_{j\text{-amb}}$ (in free air)	0.22	degC/mW
$\Theta_{j\text{-mb}}$	0.035	degC/mW

ELECTRICAL CHARACTERISTICS (T_j=25°C unless otherwise stated)

			Min.	Typ.	Max.	
I_{CBO}	Collector cut-off current					
	V_{CB}=40V, I_E=0		-	50	500	nA
	V_{CB}=40V, I_E=0, T_j=150°C		-	100	300	μA
I_{EBO}	Emitter cut-off current					
	V_{EB}=4.0V, I_C=0	BSX59,60	-	50	300	nA
		BSX61	-	50	500	nA
	V_{EB}=4.0V, I_C=0, T_j=150°C		-	5.0	50	μA
	Currents with reverse biased emitter junction					
I_{CEX}	V_{CE}=40V, $-V_{BE}$=4.0V	BSX59,60	-	50	500	nA
		BSX61	-	50	1000	nA
	V_{CE}=40V, $-V_{BE}$=4.0V, T_j=150°C					
		BSX59,60	-	100	300	μA
		BSX61	-	100	500	μA
$-I_{BEX}$	V_{CE}=40V, $-V_{BE}$=4.0V	BSX59,60	-	50	500	nA
		BSX61	-	50	1000	nA
	V_{CE}=40V, $-V_{BE}$=4.0V, T_j=150°C					
		BSX59,60	-	100	300	μA
		BSX61	-	100	500	μA

ELECTRICAL CHARACTERISTICS (cont'd)

			Min.	Typ.	Max.	
$V_{(BR)CBO}$	Collector-base breakdown voltage					
	$I_C = 10\mu A$, $I_E = 0$	BSX59	70	120	-	V
		BSX60	70	110	-	V
		BSX61	70	100	-	V
	Collector-emitter breakdown voltage					
$V_{(BR)CES}$	$I_C = 100\mu A$, $V_{BE} = 0$	BSX59	60	110	-	V
		BSX60,61	60	100	-	V
$V_{(BR)CEO}$	$I_C = 10mA$, $I_B = 0$	BSX59,61	45	55	-	V
		BSX60	30	50	-	V
$V_{(BR)CEX}$	$-V_{BB} = 3.5V$, $R_B = 70\Omega$	BSX59,61			See note 1	
$V_{CE(sat)}$	Collector-emitter saturation voltage					
	$I_C = 150mA$, $I_B = 15mA$	BSX59	-	0.24	0.3	V
		BSX60	-	0.21	0.3	V
		BSX61	-	0.18	0.5	V
	$I_C = 500mA$, $I_B = 50mA$	BSX59	-	0.44	0.5	V
		BSX60	-	0.42	0.5	V
		BSX61	-	0.4	0.7	V
	$I_C = 1.0A$, $I_B = 100mA$	BSX59	-	0.58	1.0	V
		BSX60	-	0.56	1.0	V
		BSX61	-	0.56	1.3	V
$V_{BE(sat)}$	Base-emitter saturation voltage					
	$I_C = 150mA$, $I_B = 15mA$		-	0.8	1.0	V
	$I_C = 500mA$, $I_B = 50mA$	BSX59	0.85	1.0	1.2	V
		BSX60	0.7	1.0	1.3	V
		BSX61	0.77	1.0	1.3	V
	$I_C = 1.0A$, $I_B = 100mA$		-	1.2	1.8	V
h_{FE}	Static forward current transfer ratio					
	$I_C = 150mA$, $V_{CE} = 1.0V$	BSX59	30	70	-	
		BSX60	30	100	-	
		BSX61	30	110	-	

NOTE

1. No breakdown may occur when the transistor is switched from $I_C = 1.0A$ to $V_{CE} = 60V$ with $-I_{Boff} = 50mA$.

ELECTRICAL CHARACTERISTICS (cont'd)

			Min.	Typ.	Max.	
h_{FE}	Static forward current transfer ratio					
	I_C=500mA, V_{CE}=1.0V	BSX59, 61	25	-	-	
		BSX60	30	-	90	
	I_C=1.0A, V_{CE}=5.0V	BSX59	20	40	-	
		BSX60	25	50	-	
		BSX61	20	55	-	
h_{fe}	Small signal forward current transfer ratio I_C=50mA, V_{CE}=10V, f=100MHz		2.5	4.75	-	
C_{ibo}	Input capacitance $-V_{BE}$=0.5V, I_C=0, f=1.0MHz		-	36	50	pF
C_{obo}	Output capacitance V_{CB}=10V, I_E=0, f=1.0MHz		-	5.75	10	pF
Q_s	Recovered charge (see fig.1) I_C=500mA, I_B=50mA,					
	V_{CC}=30V	BSX60	-	3.8	5.0	nC
t_{on}	Turn-on time (see fig.2) I_C=500mA, I_{Bon}=50mA, $-V_{BEoff}$=2.0V,					
	V_{CC}=50V	BSX59	-	17	35	ns
	V_{CC}=30V	BSX60	-	17	40	ns
	V_{CC}=50V	BSX61	-	18	50	ns
t_{off}	Turn-off time (see fig.2) I_C=500mA, I_{Bon}=$-I_{Boff}$=50mA,					
	V_{CC}=50V	BSX59	-	45	60	ns
	V_{CC}=30V	BSX60	-	58	70	ns
	V_{CC}=50V	BSX61	-	70	100	ns

Recovered charge test circuit and waveforms

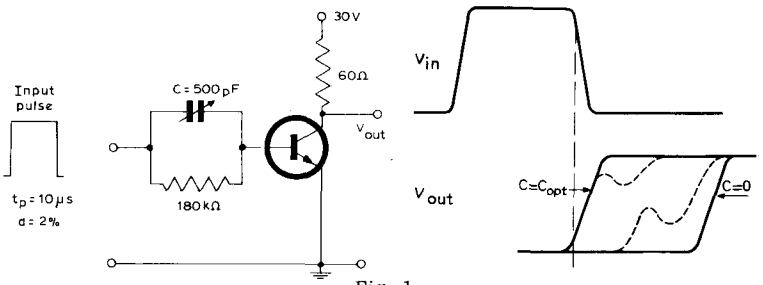


Fig. 1

Adjust C from zero to C_{opt}

$$Q_s = C_{opt} \times V_{in}$$

Turn-on and turn-off test circuit and waveforms

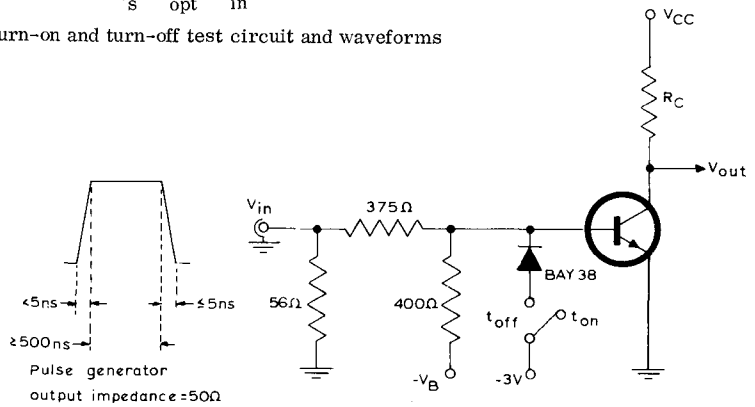
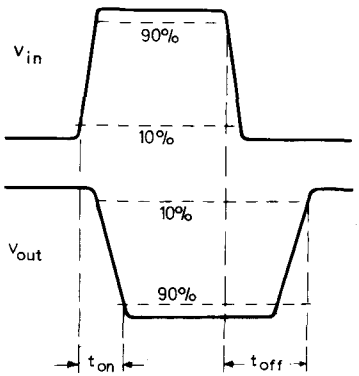


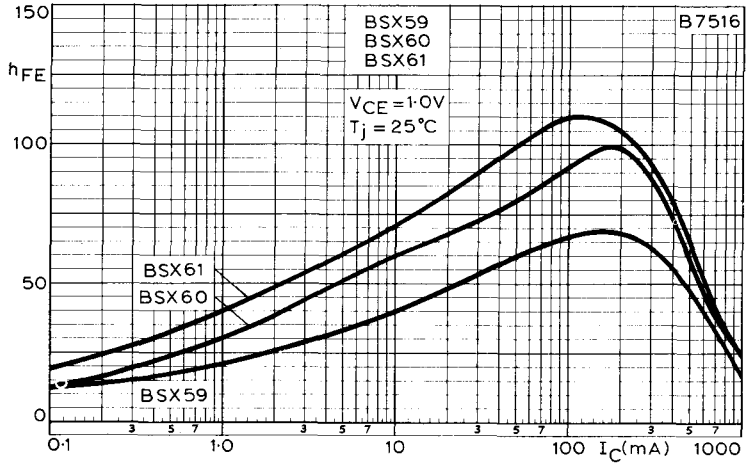
Fig. 2

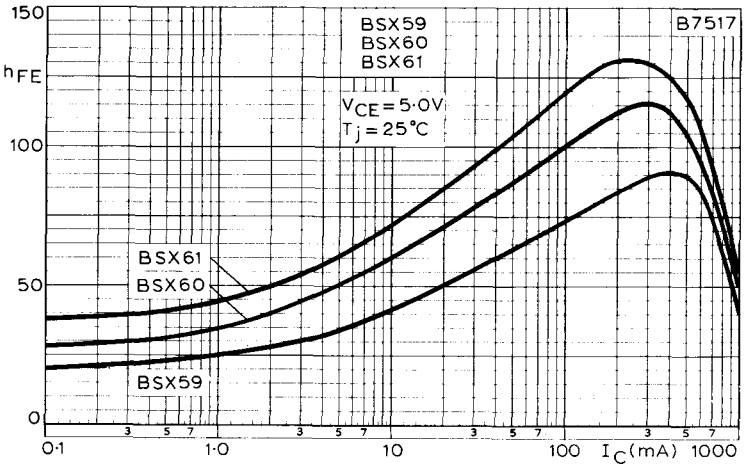
Measurement		BSX59 BSX61	BSX60	
	V_{CC}	50	30	V
	R_C	100	60	Ω
t_{on}	$-V_B$	4.0		V
	V_{in}	24.75		V
t_{off}	$-V_B$	16.7		V
	V_{in}	37.5		V



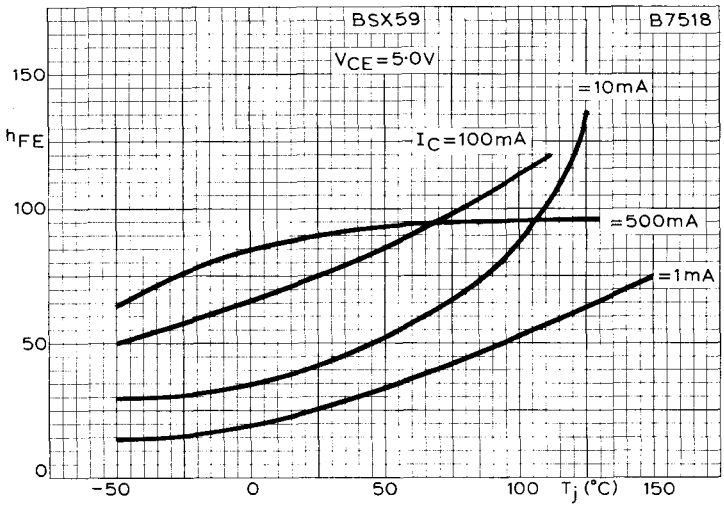
SILICON PLANAR EPITAXIAL N-P-N TRANSISTORS

BSX59
BSX60
BSX61

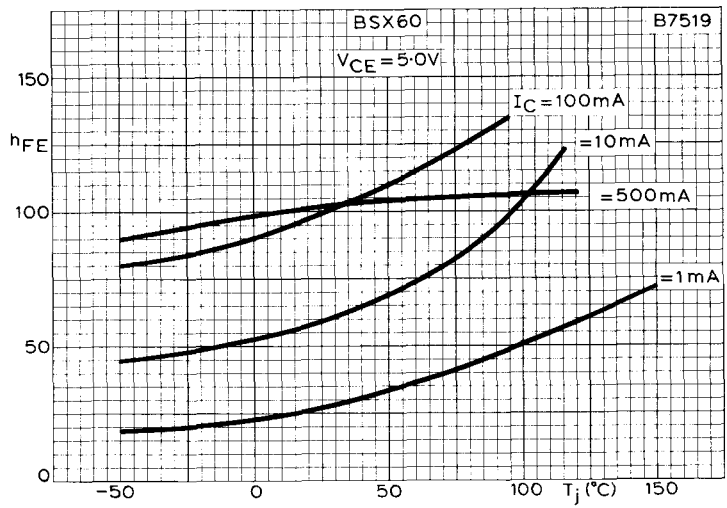




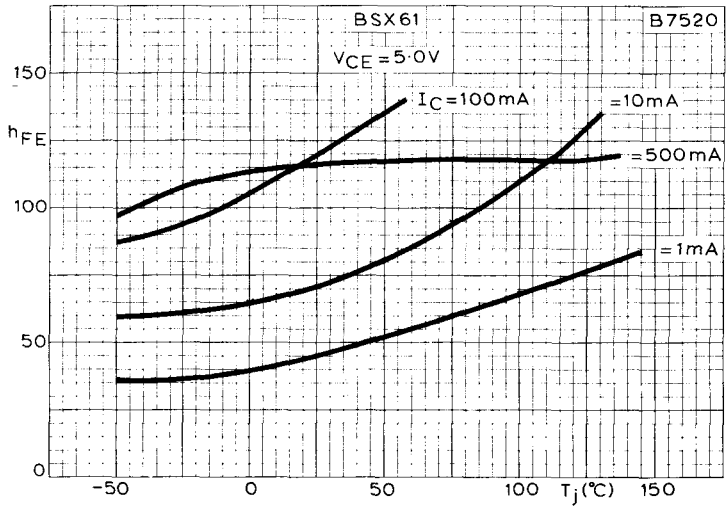
TYPICAL VARIATION OF STATIC FORWARD CURRENT TRANSFER RATIO WITH COLLECTOR CURRENT AT V_{CE} = 1.0 and 5.0V RESPECTIVELY



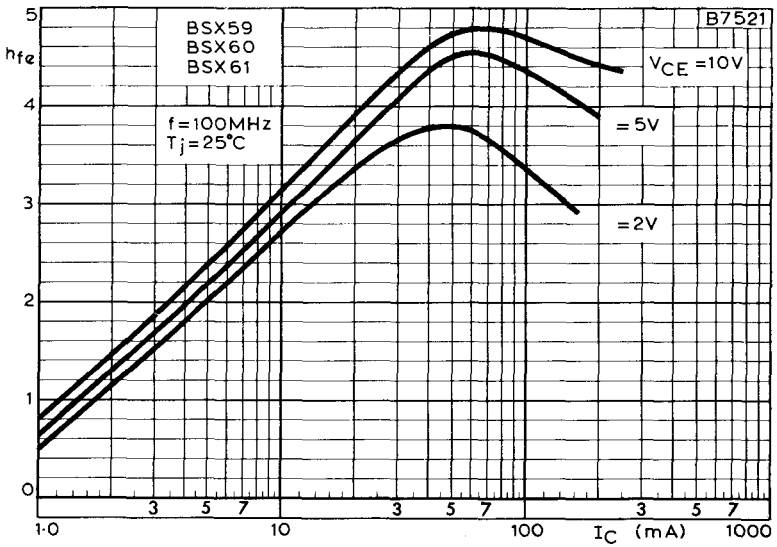
TYPICAL VARIATION OF STATIC FORWARD CURRENT TRANSFER RATIO WITH JUNCTION TEMPERATURE ; BSX59



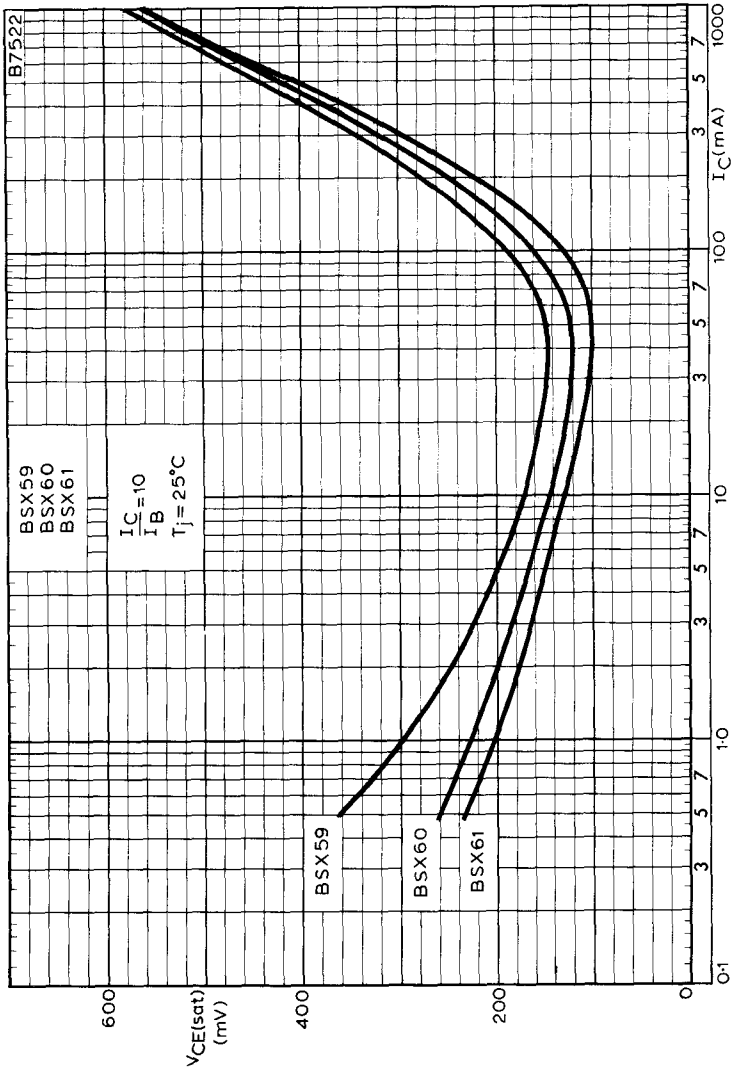
TYPICAL VARIATION OF STATIC FORWARD CURRENT TRANSFER RATIO WITH JUNCTION TEMPERATURE; BSX60



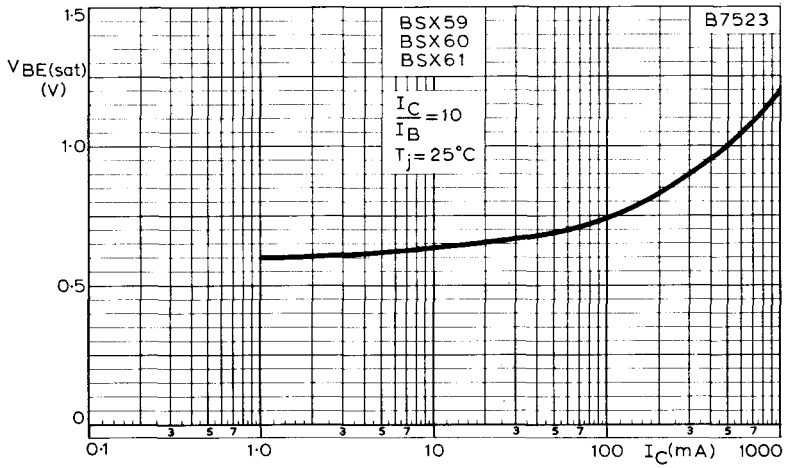
TYPICAL VARIATION OF STATIC FORWARD CURRENT TRANSFER RATIO WITH JUNCTION TEMPERATURE; BSX61

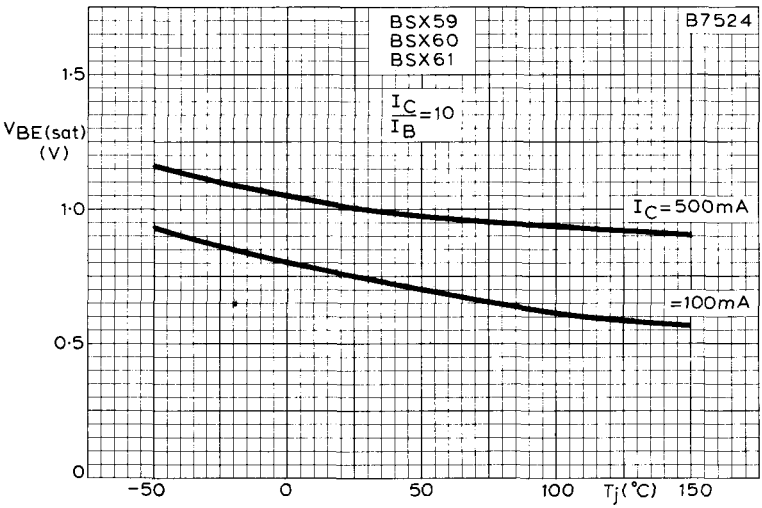


TYPICAL VARIATION OF SMALL SIGNAL FORWARD CURRENT TRANSFER RATIO WITH COLLECTOR CURRENT

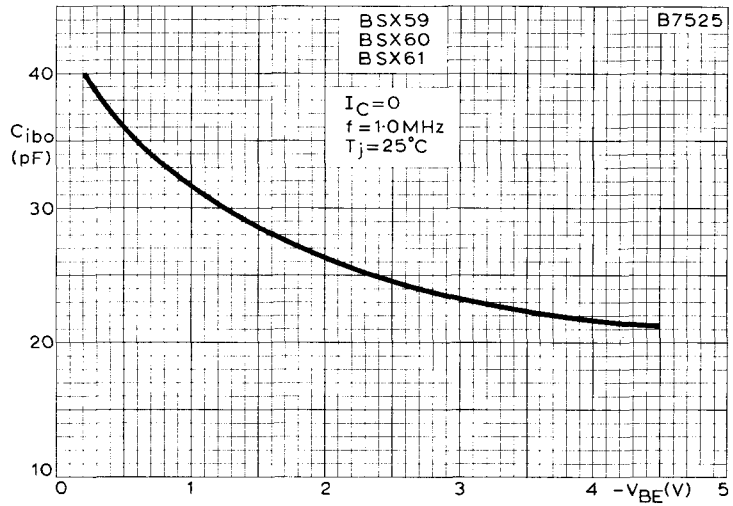


TYPICAL VARIATION OF COLLECTOR-EMITTER SATURATION VOLTAGE WITH COLLECTOR CURRENT

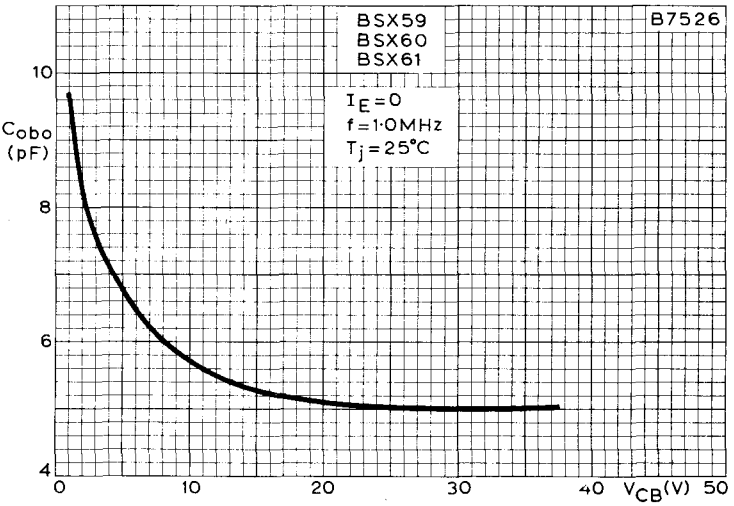




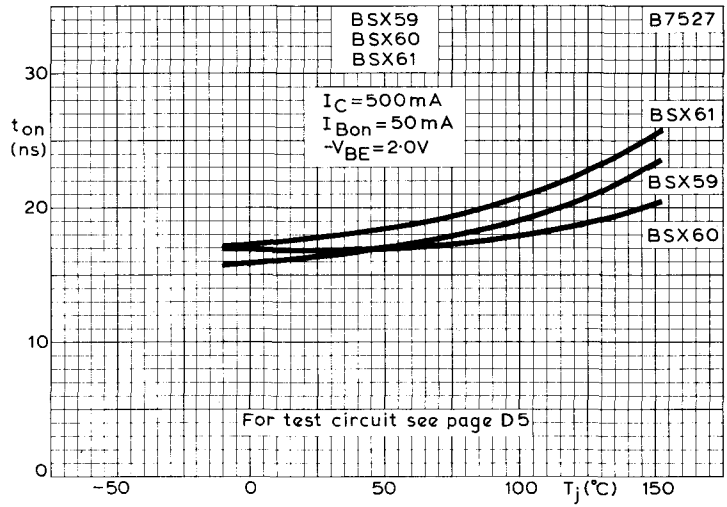
TYPICAL VARIATION OF BASE-EMITTER SATURATION VOLTAGE WITH COLLECTOR CURRENT AND JUNCTION TEMPERATURE RESPECTIVELY

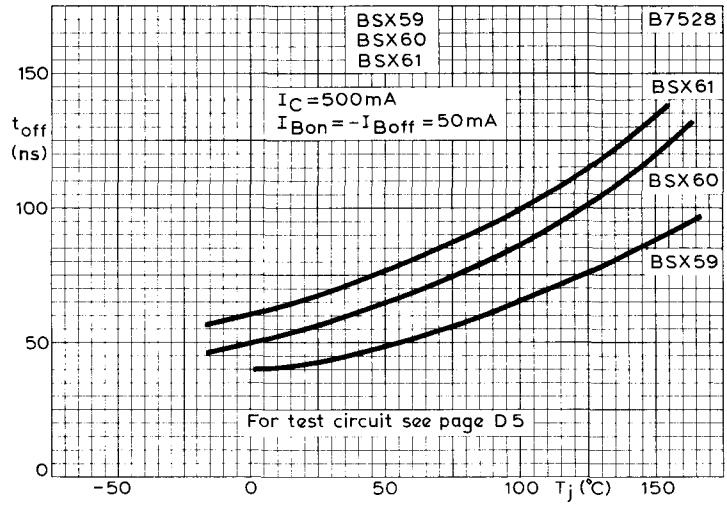


TYPICAL VARIATION OF INPUT CAPACITANCE WITH BASE-EMITTER VOLTAGE

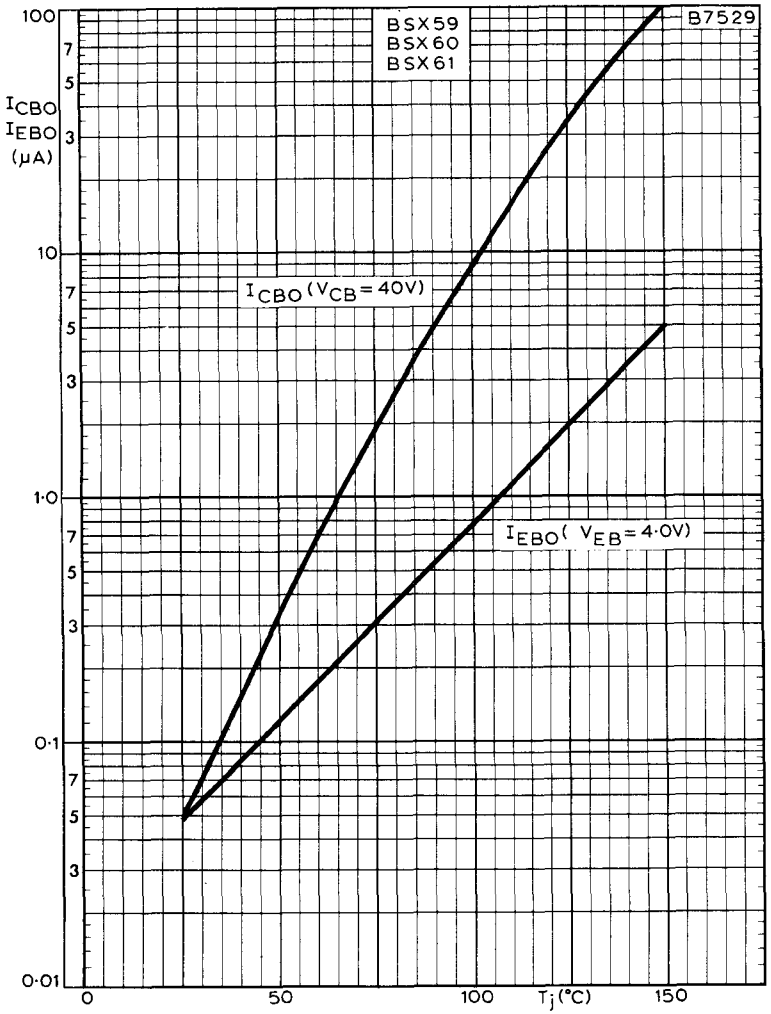


TYPICAL VARIATION OF OUTPUT CAPACITANCE WITH COLLECTOR-BASE VOLTAGE





TYPICAL VARIATION OF TURN-ON AND TURN-OFF TIME WITH JUNCTION TEMPERATURE



TYPICAL VARIATION OF COLLECTOR AND EMITTER CUT-OFF CURRENT WITH JUNCTION TEMPERATURE

SILICON PLANAR EPITAXIAL N-P-N TRANSISTOR

BSY95A

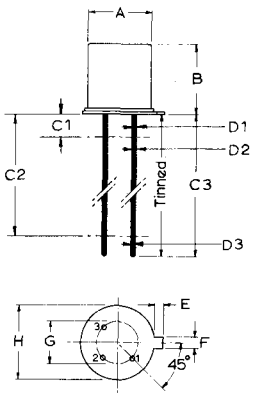
Silicon planar epitaxial n-p-n transistor for general purpose low level switching applications.

QUICK REFERENCE DATA

V_{CBO} max.	20	V
V_{CEO} max.	15	V
I_{CM} max.	200	mA
P_{tot} max. ($T_{amb} \leq 25^{o}C$)	300	mW
h_{FE} (I_C=10mA)	50-200	
f_T min. (I_C=10mA, V_{CE}=9.0V, f=100MHz)	200	MHz
t_s max.	50	ns

OUTLINE AND DIMENSIONS

Conforming to J.E.D.E.C. TO-18
B.S. 3934 SO-12A/SB3-6A



Viewed from underside

	Millimetres		
	Min.	Typ.	Max.
A	4.53	-	4.8
B	4.66	-	5.33
C1	-	-	0.51
C2	12.7	-	-
C3	12.7	-	15
D1	-	-	1.01
D2	0.41	-	0.48
D3	-	-	0.53
E	0.84	-	1.17
F	0.92	-	1.16
G	-	2.54	-
H	5.31	-	5.84

Connections 1. Emitter 3. Collector connected to envelope
2. Base

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{CBO} max.	20	V
V_{CEO} max.	15	V
V_{EBO} max.	5.0	V
*$I_{C(AV)}$ max.	100	mA
I_{CM} max.	200	mA
P_{tot} max. ($T_{amb} \leq 25^{o}C$)	300	mW

*Averaged over any 20ms period.

Temperature

T_{stg} min.	-65	^{o}C
T_{stg} max.	175	^{o}C
T_{j} max. (operating)	175	^{o}C

THERMAL CHARACTERISTIC

$R_{th(j-amb)}$	0.5	degC/mW

ELECTRICAL CHARACTERISTICS ($T_{amb}=25^{o}C$ unless otherwise stated)

		Min.	Max.	
I_{CBO}	Collector cut-off current $V_{CB}=16V$, $I_{E}=0$	-	50	nA
$V_{BR(CBO)}$	Collector-base breakdown voltage $I_{C}=1.0\mu A$	20	-	V
I_{EBO}	Emitter cut-off current $V_{EB}=1.5V$, $I_{C}=0$	-	25	nA
$V_{(BR)EBO}$	Emitter-base breakdown voltage $I_{E}=10\mu A$	5.0	-	V
I_{CEO}	Collector-emitter cut-off current $V_{CE}=12V$, $I_{B}=0$	-	250	nA
$V_{(BR)CEO}$	Collector-emitter breakdown voltage $I_{C}=10mA$**	15	-	V
f_{T}	Transition frequency $I_{C}=10mA$, $V_{CE}=9.0V$, $f=100MHz$	200	-	MHz

**Pulsed: Pulse width=300μs, duty cycle <2%.

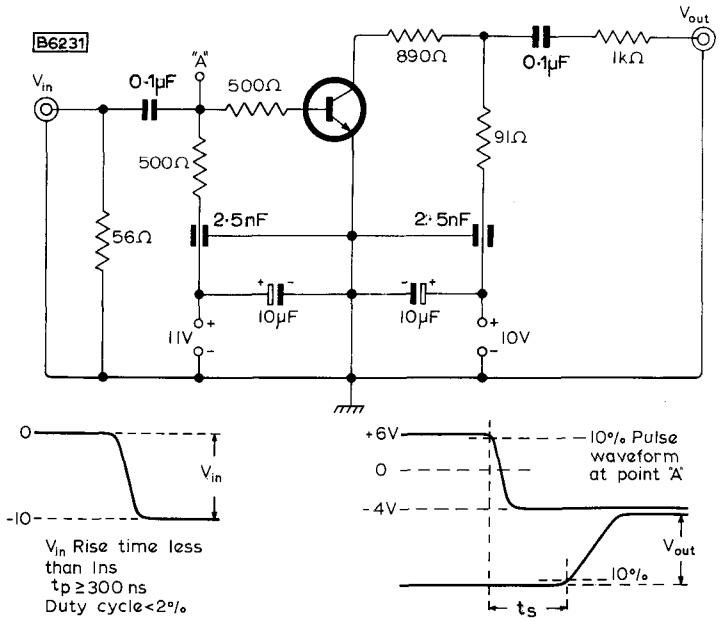
		Min.	Max.	
h_{FE}	Common emitter forward current transfer ratio			
	I_C=1.0mA, V_{CE}=0.35V	30	-	
	I_C=10mA, V_{CE}=0.35V	50	200	
$V_{CE(sat)}$	Collector-emitter saturation voltage			
	I_C=10mA, I_B=0.2mA	-	0.35	V
$V_{BE(sat)}$	Base-emitter saturation voltage			
	I_C=10mA, I_B=0.2mA	0.67	0.87	V
C_{ob}	Collector-base capacitance V_{CB}=9.0V, I_E=0			
	f=1.0MHz	-	6.0	pF
t_s	Storage time			
	I_C=10mA	-	50	ns

See test circuit on page 4

SOLDERING AND WIRING RECOMMENDATIONS

1. When using a soldering iron, transistors may be soldered directly into the circuit, but heat conducted to the junction should if possible be kept to a minimum by the use of a thermal shunt.
2. Transistors may be dip-soldered at a solder temperature of 245°C for a maximum soldering time of 5 seconds. The case temperature during soldering must not at any time exceed the maximum storage temperature. These recommendations apply to a transistor mounted flush on a board having punched-through holes, or spaced at least 1.5mm above a board having plated-through holes.
3. Care should be taken not to bend the leads nearer than 1.5mm from the seal.
4. If devices are stored at temperatures above 100°C before incorporation into equipment, some deterioration of the external surface is likely to occur which may make soldering into the circuit difficult. Under these circumstances the leads should be retinned using a suitable activated flux.

STORAGE TIME TEST CIRCUIT



Input and output waveforms

HIGH VOLTAGE N-P-N SILICON POWER TRANSISTOR

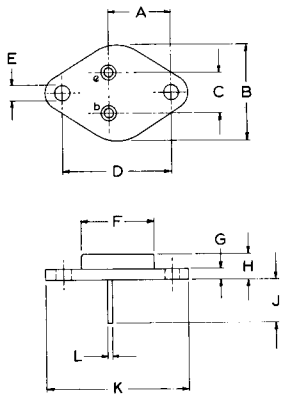
BU126

High voltage n-p-n silicon power transistor intended for use in the switched mode power supply of television receivers.

QUICK REFERENCE DATA		
V_{CESM} max. (V_{BE} = 0)	750	V
V_{CEXM} max. (-V_{BE} = 1.5V)	750	V
I_{CM} max. (peak value)	6	A
P_{tot} max. ($T_{mb} \leq 50^{o}C$)	30	W
$V_{CE(sat)}$ max. (I_C = 2.5A, I_B = 0.25A)	10	V
t_f typ. (I_{CM} = 2.5A, $I_{B(end)}$ = 0.25A)	0.15	μs

OUTLINE AND DIMENSIONS

Conforms to BS 3934 SO-5A/SB2-2
J.E.D.E.C. TO-3



	Millimetres		
	Min.	Nom.	Max.
A	-	16.9	-
B	-	-	26.6
C	-	10.9	-
D	-	30.1	-
E	4.0	-	4.2
F	-	-	20.3
G	-	3.15	-
H	-	-	9.5
J	11	-	13
K	-	-	39.5
L	-	1.0	-

Collector electrically connected to the envelope

ACCESSORIES

56201 consisting of: - 56201A (insulating bushes) and 56201B (mica washer)
56214 lead washer

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{CESM}	max. (V_{BE} = 0) (peak value)	750	V
V_{CEXM}	max. (-V_{BE} = 1.5V) (peak value)	750	V
V_{CEO}	max. (open base)	300	V
I_C	max. (d.c.)	3	A
I_{CM}	max. (peak value)	6	A
$-I_{CM}$	max. (peak value)	3	A
I_B	max. (d.c.)	2	A
I_{BM}	max. (peak value)	2	A
$-I_{B(AV)}$	max. (d.c. or averaged over any 20ms period)	100	mA
$-I_{BM}$	max. (peak value, turn-off current)	1.5	A
P_{tot}	max. ($T_{mb} \leq 50^oC$)	30	W

Temperature

T_{stg}	range	-65 to +125	^oC
T_j	max.	+125	^oC

THERMAL CHARACTERISTICS

$R_{th(j-mb)}$		2.5	$^oC/W$
$R_{th(mb-hs)}$	with mica washer and lead washer	0.75	$^oC/W$
$R_{th(mb-hs)}$	with lead washer only	0.5	$^oC/W$

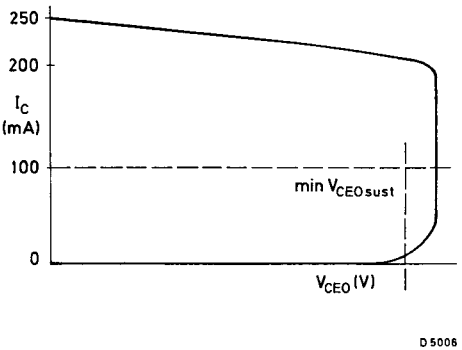
ELECTRICAL CHARACTERISTICS ($T_j = 25^oC$ unless otherwise stated)

		Min.	Typ.	Max.	
I_{CES}	Collector cut-off current †				
	V_{CE} = 750V; V_{BE} = 0	-	-	0.5	mA
	V_{CE} = 750V; V_{BE} = 0, $T_j = 125^oC$	-	-	2	mA
I_{EBO}	Emitter cut-off current				
	I_C = 0; V_{EB} = 6V	-	-	5	mA
h_{FE}	Large signal forward current transfer ratio				
	I_C = 1A; V_{CE} = 5V	15	-	60	
$V_{CE(sat)}$	Collector-emitter saturation voltage				
	I_C = 2.5A; I_B = 0.25A	-	-	10	V
	I_C = 4A; I_B = 1A	-	-	5	V

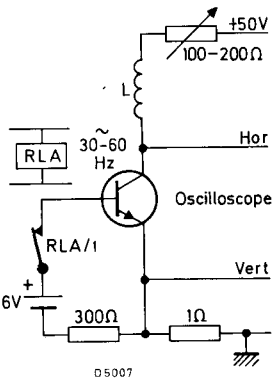
†Measured with a half sinewave voltage (curve tracer).

ELECTRICAL CHARACTERISTIC (contd.)

		Min.	Typ.	Max.	
$V_{BE(sat)}$	Base-emitter saturation voltage I_C = 2.5A, I_B = 0.25A	-	-	1.5	V
$V_{CEO(sust)}$	Collector-emitter sustaining voltage I_B = 0; I_C = 100mA; L = 25mH	300	-	-	V



Oscilloscope display for V_{CEO} sust



Test circuit for V_{CEO} sust

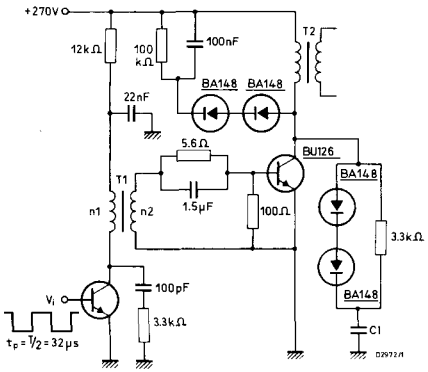
ELECTRICAL CHARACTERISTICS (contd.)

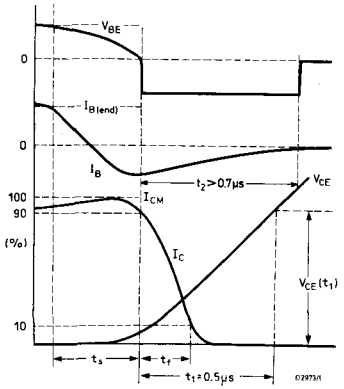
		Min.	Typ.	Max.	
f_T	Transition frequency $I_C = 0.2A$, $V_{CE} = 10V$, f = 1MHz	-	8	-	MHz
C_{Tc}	Collector capacitance $I_E = I_e = 0$, $V_{CB} = 10V$, f = 1MHz	-	85	-	pF
C_{Te}	Emitter capacitance $I_C = I_c = 0$, $V_{EB} = 2V$, f = 1kHz	-	1.4	-	nF

Turn-off time
$I_{CM} = 2.5A$, $I_{B(end)} = 0.25A$

t_s	Storage time	-	1.2	-	μs
t_f	Fall time	-	0.15	-	μs

Practical turn-off circuit

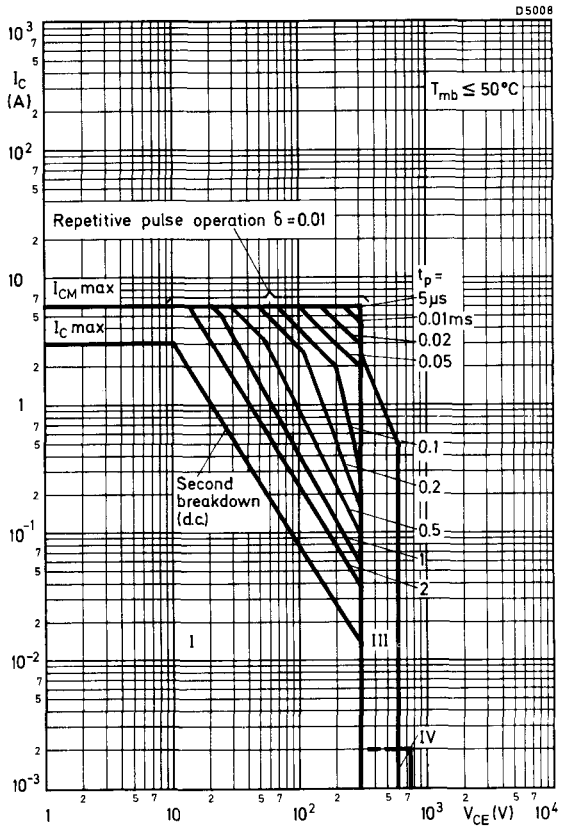




		Min.	Typ.	Max.	
$V_{CE}(t_1)$	Allowable value of V_{CE} after 0.5μs	-	-	500	V

T1 Core EI 25
n1 = 350 turns, 100mH
n2 = 32 turns
Leakage inductance at secondary 3μH

The value of C_1 depends on the stray capacitance of T_2 and on the capacitive loading of the secondary (typical value for C_1 is 1.5nF).



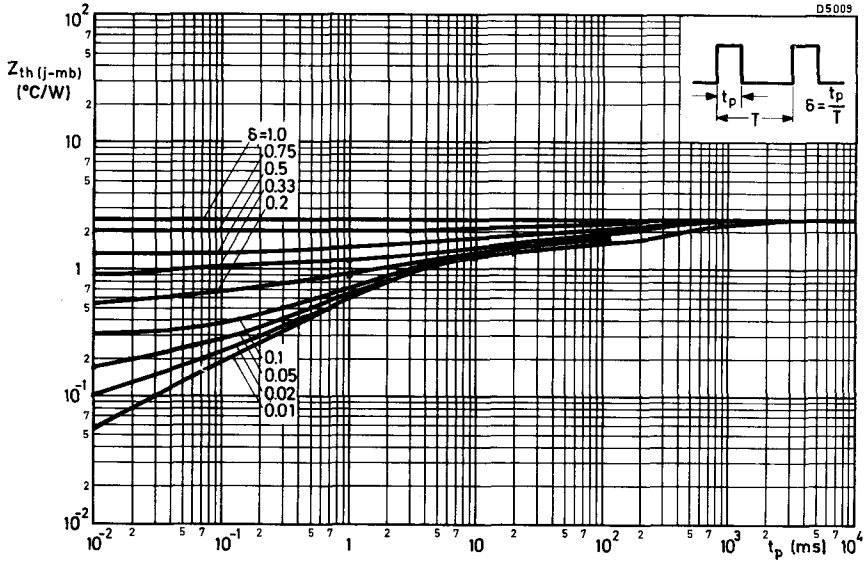
Safe Operating Area (Regions I, II and III forward biased)

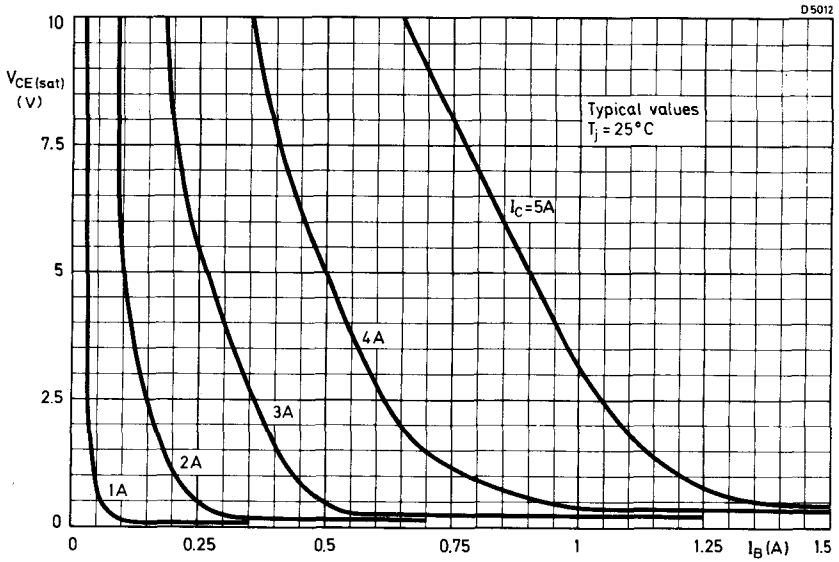
I Region of permissible d.c. operation

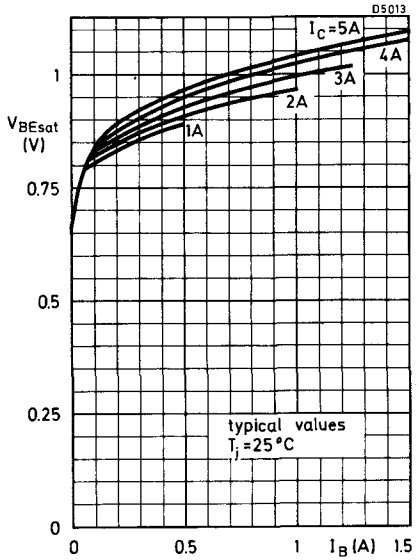
II Permissible extension for repetitive pulse operation

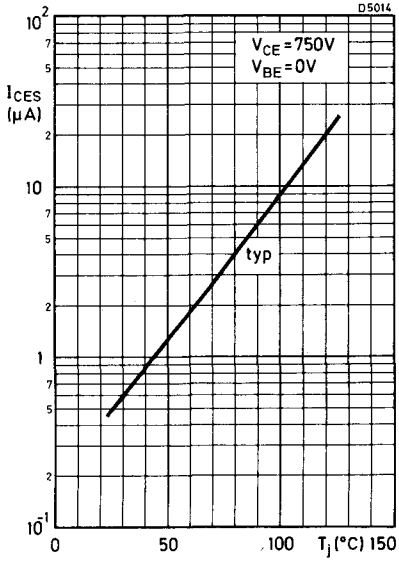
III Area of permissible operation during turn-on in switched mode power supply circuits, provided $t_p \leq 0.6\mu s$ and $R_{BE} \leq 100\Omega$

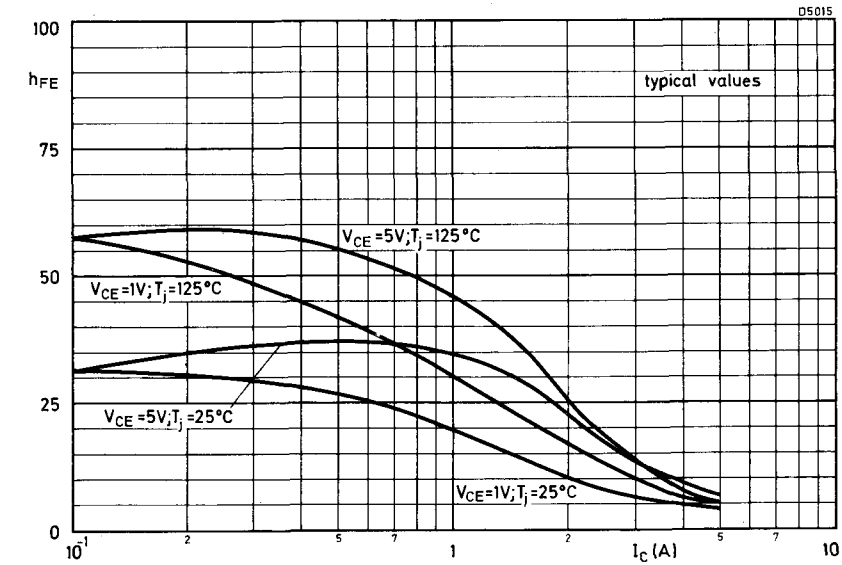
IV Repetitive pulse operation in this region is allowable, provided $V_{BE} \leq 0$ and $t_p \leq 2ms$

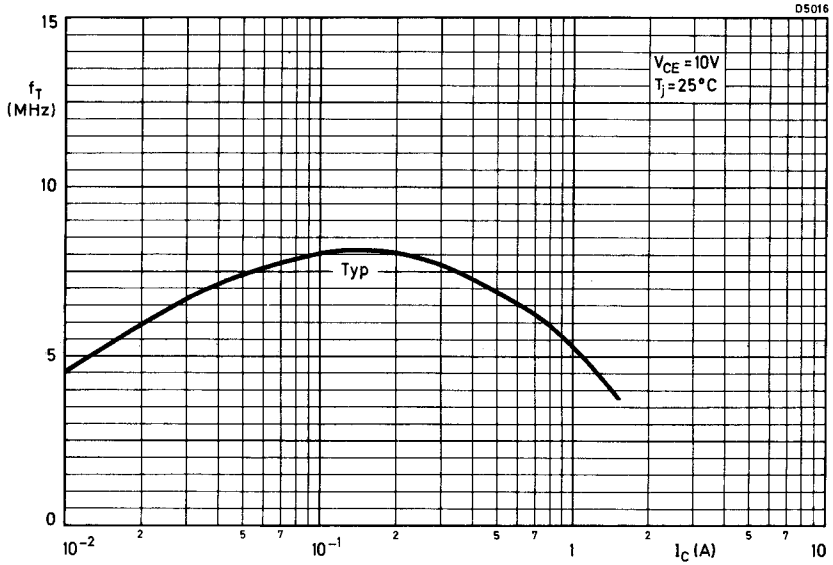

D5009
$Z_{th\ (j\text{-}mb)}$ (°C/W)
δ=1.0
0.75
0.5
0.33
0.2
0.1
0.05
0.02
0.01
t_p
T
$\delta = \frac{t_p}{T}$
t_p (ms)

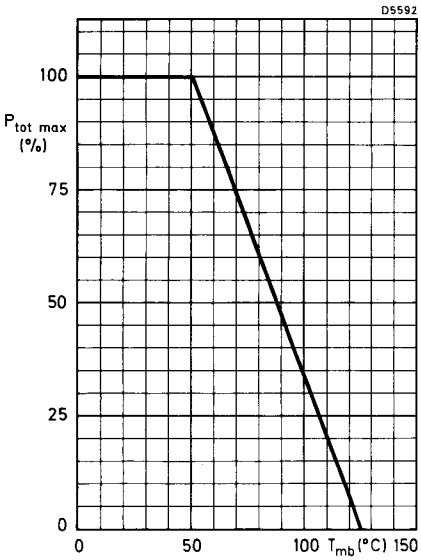

D5012
$V_{CE\ (sat)}$ (V)
Typical values
T_j = 25°C
I_C=5A
4A
3A
2A
1A
I_B (A)


D5013
I_C=5A
4A
3A
2A
1A
V_{BEsat} (V)
1
0.75
0.5
0.25
0
typical values
T_j=25°C
0
0.5
1
I_B (A)
1.5


D5014
V_{CE}=750V
V_{BE}=0V
I_{CES} (μA)
10^2
10
1
10^{-1}
typ
0
50
100
T_j (°C)
150


D5015
h_{FE}
100
75
50
25
0
typical values
V_{CE}=5V;T_j=125°C
V_{CE}=1V;T_j=125°C
V_{CE}=5V;T_j=25°C
V_{CE}=1V;T_j=25°C
10^{-1}
1
10
I_C (A)


D5016
15
f_T (MHz)
10
5
0
V_{CE} = 10V
T_j = 25°C
Typ
10^{-2}
2
5
7
10^{-1}
2
5
7
1
2
5
7
10
I_C (A)


D5592
100
$P_{tot\ max}$ (%)
75
50
25
0
0
50
100
T_{mb} (°C)
150

APPLICATION INFORMATION (Note 1)

Switched-mode power supply circuits

Important factors in the design of switched-mode power supply circuits are the power losses and heatsink requirements of the output transistor and the base drive condition during turn-off. The basic arrangements for parallel and series-type switched-mode circuits are shown in Figs. 1, 2 and 3, together with the basic waveforms.
In power supply circuits for colour receivers the duty cycle δ varies between 0.4 and 0.6. Fig. 4 gives the nominal value of the recommended base current I_{Bend} versus the maximum peak collector current (which occurs at maximum load and minimum input voltage). Fig. 5 shows the base current waveform during turn-off.
Fig. 6 gives the total device dissipation P_{tot} versus the maximum peak collector current.
The max. permissible thermal resistance for the heatsink can be calculated from:

$$R_{th(mb-a)max\ (Note\ 2)} = \frac{T_{j\,max} - T_{amb}}{P_{tot}} - R_{th\ j-mb}$$

For the BU126: $T_{j\,max} = 125^{o}C$ and $R_{th\ j-mb} = 2.5^{o}C/W$

To ensure thermal stability, the thermal resistance of the heatsink used must not exceed the value plotted in Fig. 7.

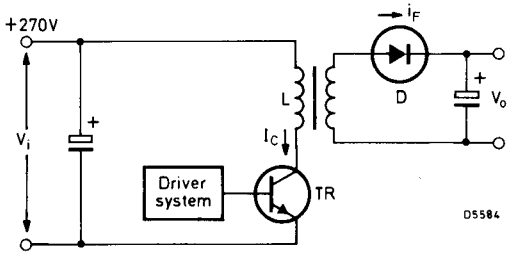


Fig. 1 Parallel type switched-mode power supply, basic circuit arrangement.

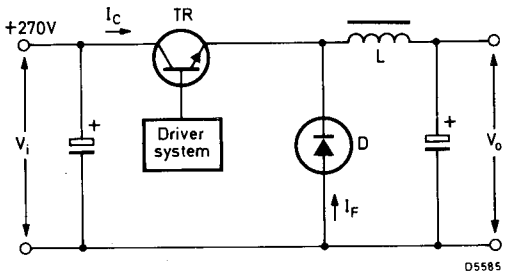


Fig. 2 Series type switched-mode power supply, basic circuit arrangement.

NOTES

1. Detailed application information available on request.
2. Including additional thermal resistances resulting from mounting hardware.

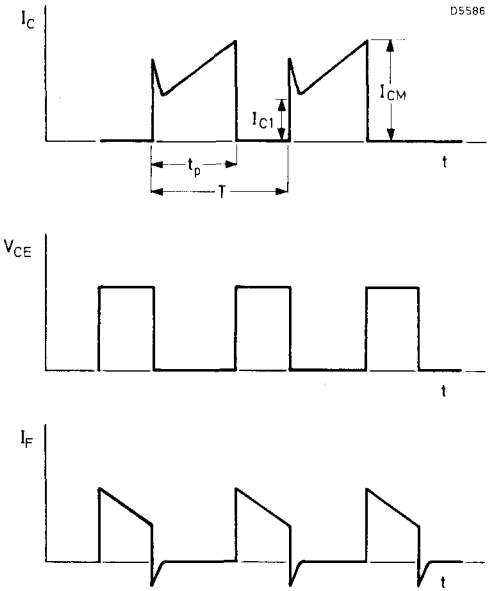


Fig. 3 Waveforms applying to switched-mode power supplies.

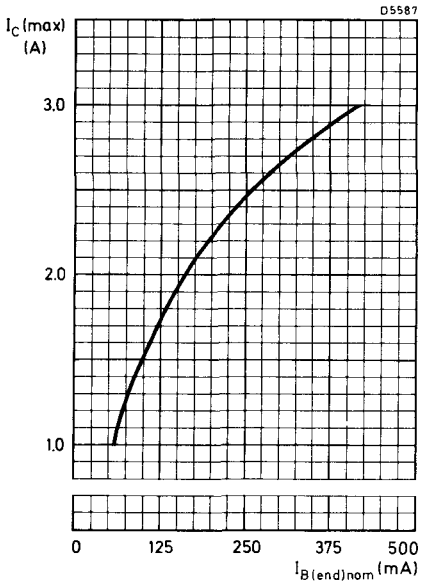


Fig. 4 Recommended nominal value of base current versus max. peak collector current.
Applies for ratio $I_{CM}/I_{C1} \geq 2$ (Fig. 3).

APPLICATION INFORMATION
(continued)

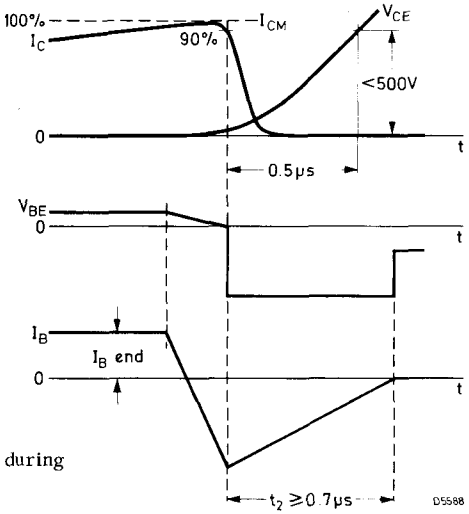


Fig. 5 Basic waveforms during current turn-off

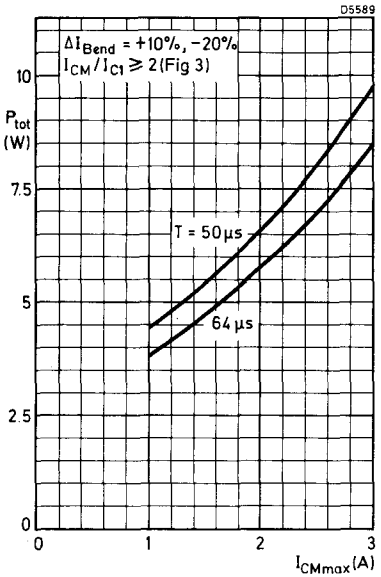


Fig. 6 Total transistor dissipation versus max. peak collector current.

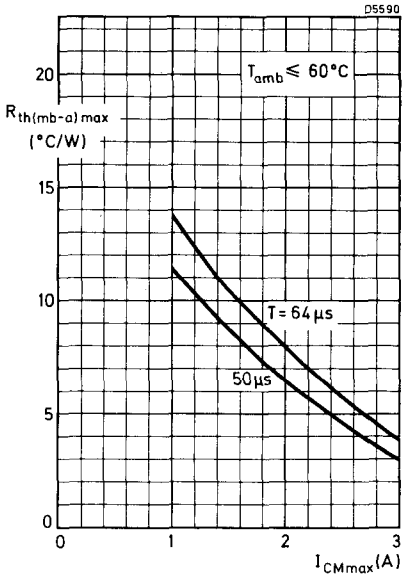
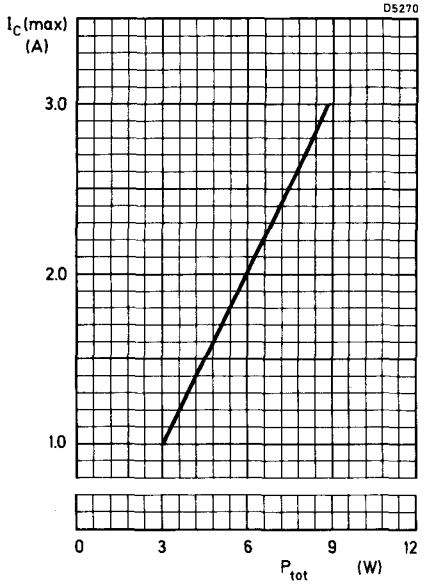
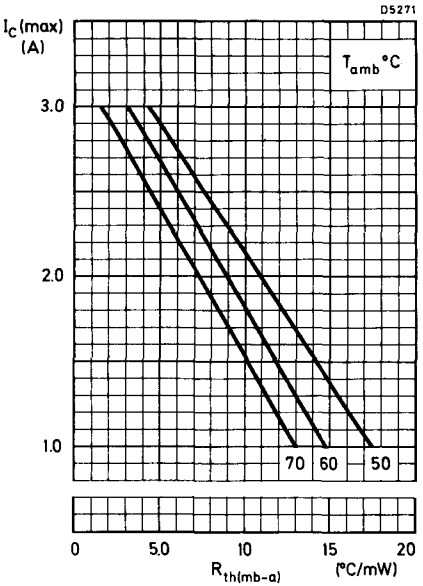
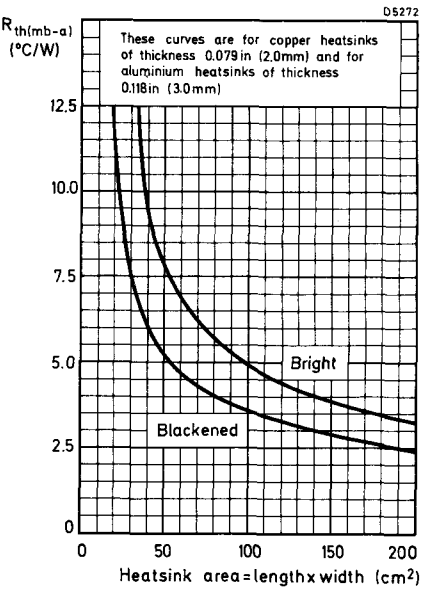


Fig. 7 Max. allowable value of $R_{th(mb-a)}$ to ensure thermal stability.


D5270
I_C (max) (A)
3.0
2.0
1.0
0
3
6
9
12
P_{tot} (W)


D5271
I_C (max) (A)
T_{amb} °C
3.0
2.0
1.0
70
60
50
0
5.0
10
15
20
$R_{th(mb-a)}$ (°C/mW)


D5272
$R_{th(mb-a)}$ (°C/W)
These curves are for copper heatsinks of thickness 0.079in (2.0mm) and for aluminium heatsinks of thickness 0.118in (3.0mm)
12.5
10.0
7.5
5.0
2.5
0
Bright
Blackened
0
50
100
150
200
Heatsink area = length x width (cm^2)

HIGH VOLTAGE SILICON POWER TRANSISTOR

BU133

High voltage n-p-n power transistor intended for general purpose consumer applications.

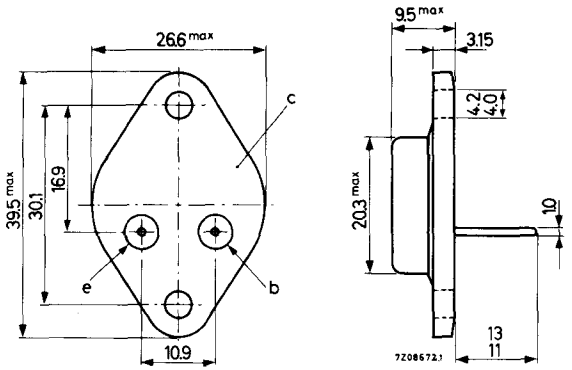
QUICK REFERENCE DATA				
Collector-emitter voltage (V_{BE} = 0) (peak value)	V_{CESM}	max.	750	V
Collector current (peak value)	I_{CM}	max.	6	A
Total power dissipation up to T_{mb} = 50°C	P_{tot}	max.	30	W
Collector-emitter saturation voltage I_C = 2.5A; I_B = 0.25A	$V_{CE\,sat}$	<	10	V
Fall time I_{CM} = 2.5A; I_{B1} = -I_{B2} = 0.5A; V_{CC} = 125V	t_f	typ.	0.5	μs

MECHANICAL DATA

Dimensions in mm

Collector connected to case

TO-3



Accessories available: 56201 and 56214

RATINGS Limiting values of operation according to the absolute maximum system.

Voltages				
Collector-emitter voltage (V_{BE} = 0) (peak value)	V_{CESM}	max.	750	V
Collector-emitter voltate ($-V_{BE}$ = 1.5V) (peak value)	V_{CEXM}	max.	750	V
Collector-emitter voltage (open base)	V_{CEO}	max.	250	V
Currents				
Collector current (d.c.)	I_C	max.	3	A
Collector current (peak value)	I_{CM}	max.	6	A
Reverse collector current (peak value)	$-I_{CM}$	max.	3	A
Base current (d.c.)	I_B	max.	2	A
Base current (peak value)	I_{BM}	max.	2	A
Reverse base current (d.c. or average over any 20 ms period)	$-I_{B(AV)}$	max.	100	mA
Reverse base current (peak value) (note 1)	$-I_{BM}$	max.	1.5	A
Power dissipation				
Total power dissipation up to T_{mb} = 50°C	P_{tot}	max.	30	W
Temperatures				
Storage temperature	T_{stg}	-65 to +125		°C
Junction temperature	T_j	max.	125	°C

THERMAL RESISTANCE

From junction to mounting base	$R_{th(j-mb)}$	=	2.5 °C/W
From mounting base to heatsink with mica washer and lead washer (56201 and 56214)	$R_{th\ mb-h}$	=	0.75°C/W
with lead washer (56214) only	$R_{th\ mb-h}$	=	0.5 °C/W

Notes

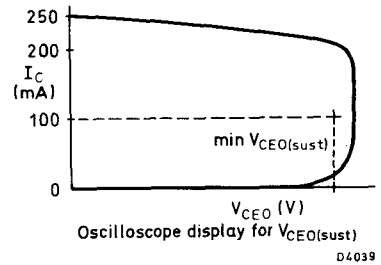
1. Turn-off current.

HIGH VOLTAGE SILICON POWER TRANSISTOR

BU133

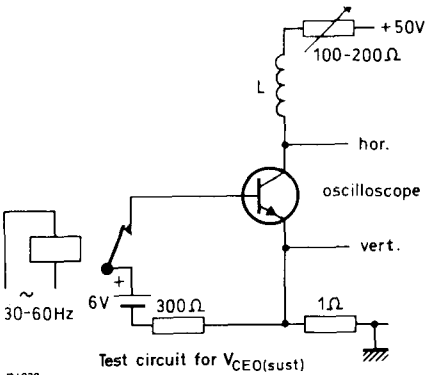
CHARACTERISTICS $T_j = 25^oC$ unless otherwise specified

Collector cut-off current (note 2)				
$V_{CEM} = 750V$; $V_{BE} = 0$	I_{CES}	<	0.5	mA
$V_{CEM} = 750V$; $V_{BE} = 0$, $T_j = 125^oC$	I_{CES}	<	2	mA
Emitter cut-off current				
$I_C = 0$; $V_{EB} = 6V$	I_{EBO}	<	5	mA
D.C. current gain				
$I_C = 1A$; $V_{CE} = 5V$	h_{FE}	15 to 80		
Saturation voltages				
$I_C = 2.5A$; $I_B = 0.25A$	$V_{CE\ sat}$	<	10	V
	$V_{BE\ sat}$	<	1.5	V
Collector-emitter sustaining voltage				
$I_B = 0$; $I_C = 100mA$; L = 25mH	$V_{CEO\ sust}$	>	250	V



Oscilloscope display for $V_{CEO(sust)}$

D4039



Test circuit for $V_{CEO(sust)}$

D4038

Notes

2. Measured with a half sine wave voltage (curve tracer).

CHARACTERISTICS (contd.) $T_j = 25^oC$ unless otherwise specified

Transition frequency at f = 1MHz

$I_C = 0.2A$; $V_{CE} = 10V$	f_T	typ.	8	MHz

Collector capacitance at f = 1MHz

$I_E = I_e = 0$; $V_{CB} = 10V$	C_c	typ.	85	pF

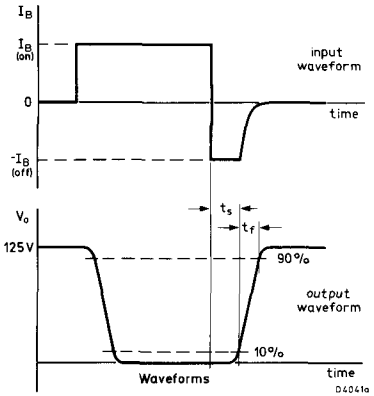
Emitter capacitance at f = 1kHz

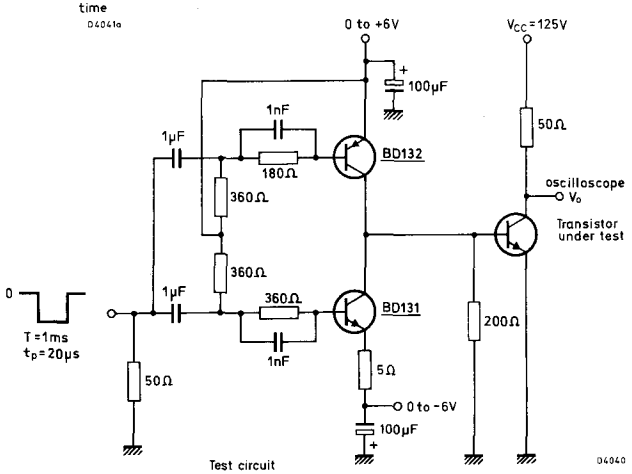
$I_C = I_c = 0$; $V_{EB} = 2V$	C_e	typ.	1.4	nF

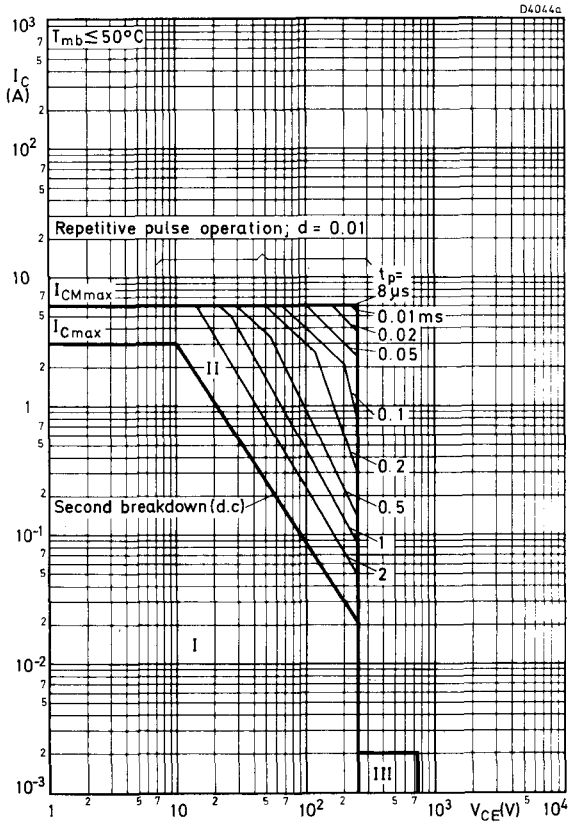
Switching times

$I_C = 2.5A$; $I_{B1} = -I_{B2} = 0.5A$; $V_{CC} = 125V$

turn-off storage time	t_s	typ.	2	ns
turn-off fall time	t_f	typ.	0.5	μs
turn-off fall time, $T_{mb} = 95^oC$	t_f	<	2	μs





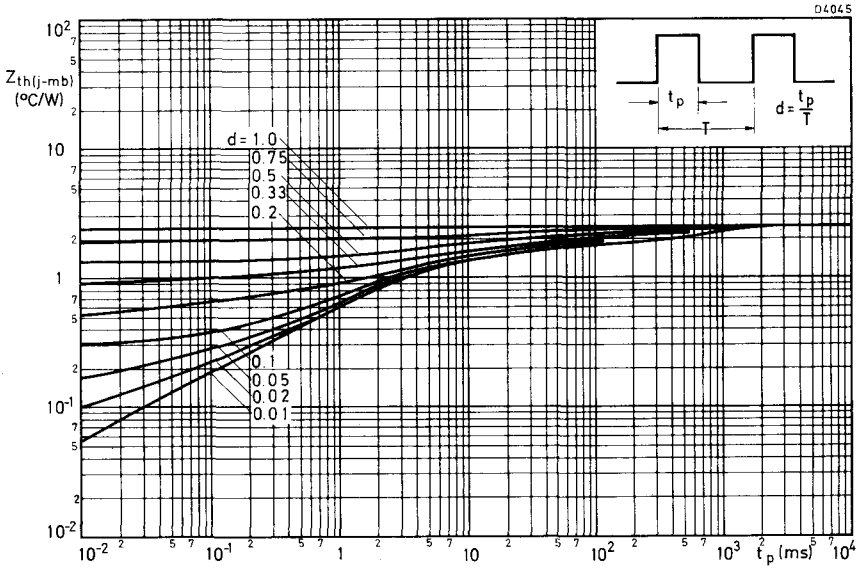


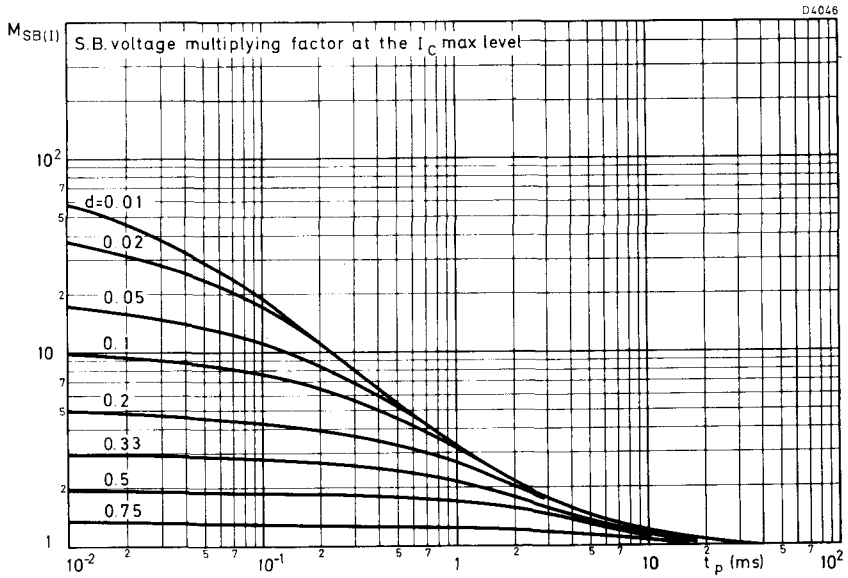
Safe Operating Area (Regions I and II forward biased)

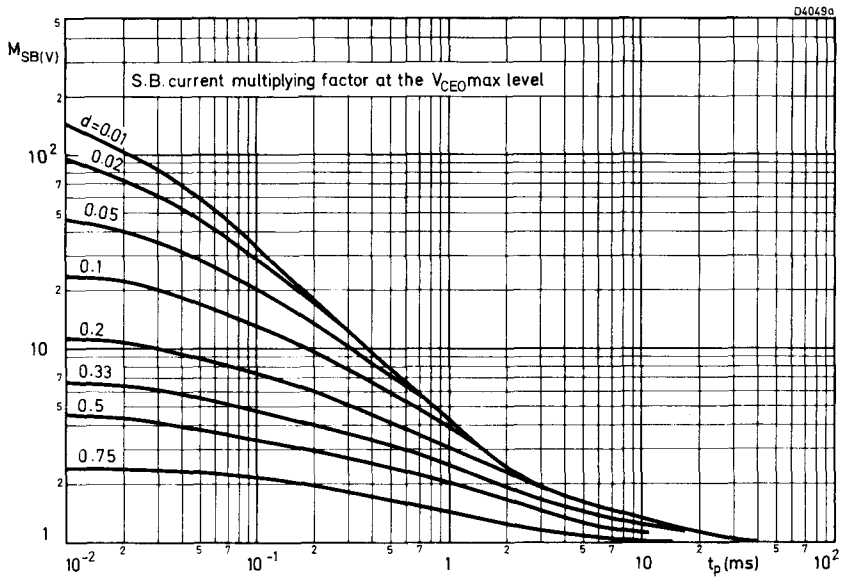
I Region of permissible d. c. operation

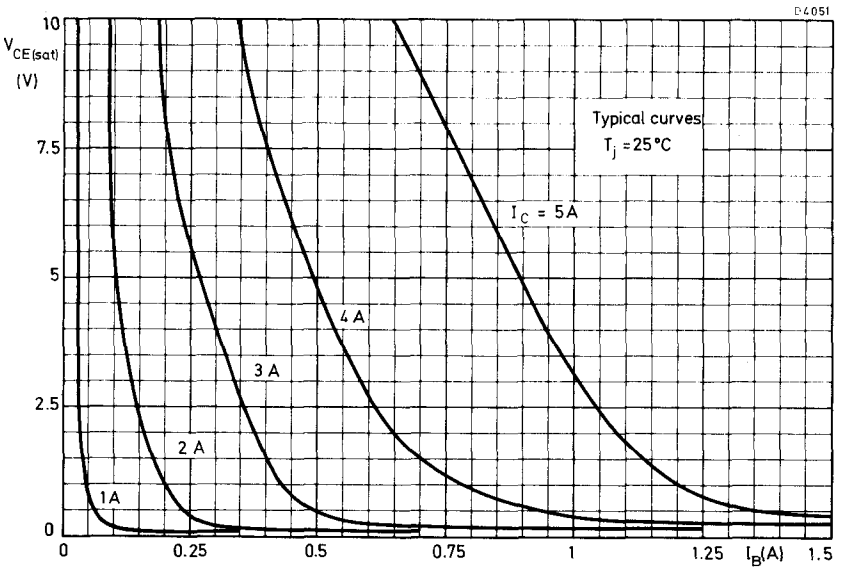
II Permissible extension for repetitive pulsed operation

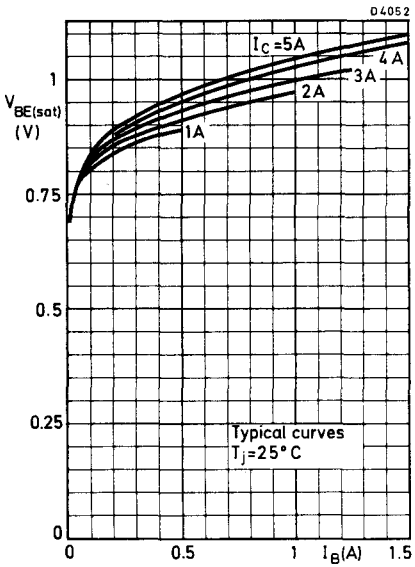
III Repetitive pulsed operation in this region is allowable, provided $V_{BE} \leq 0V$ and $t_p \leq 2ms$

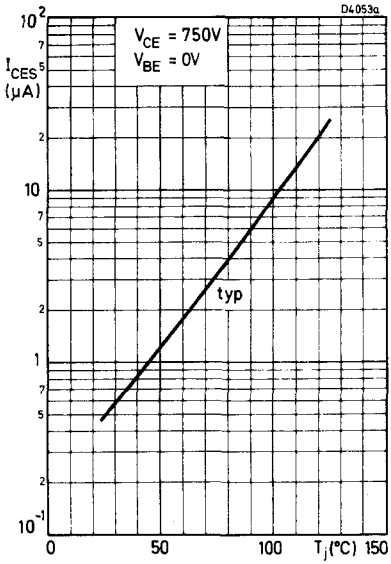

D4045
$Z_{th(j-mb)}$ (°C/W)
d = 1.0
0.75
0.5
0.33
0.2
0.1
0.05
0.02
0.01
t_p
T
$d = \frac{t_p}{T}$
t_p (ms)

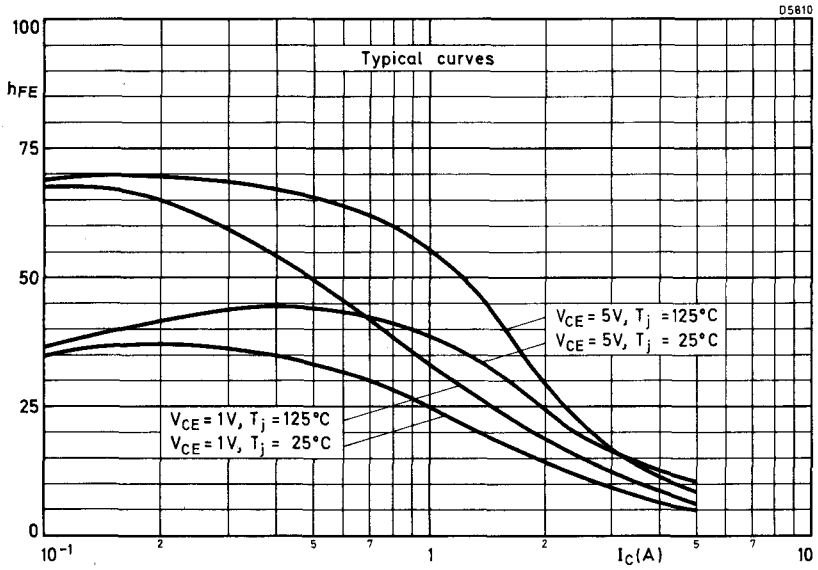

D4046
$M_{SB(I)}$
S.B. voltage multiplying factor at the I_C max level
d=0.01
0.02
0.05
0.1
0.2
0.33
0.5
0.75
t_p (ms)

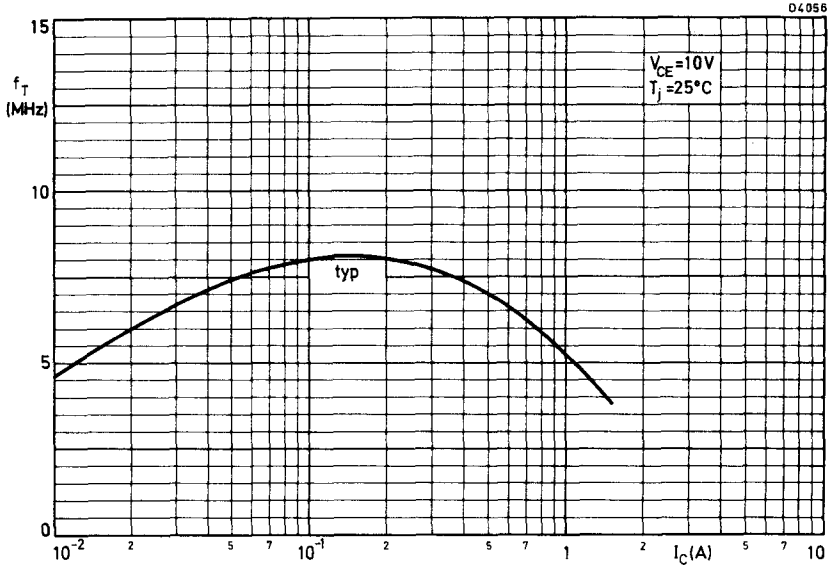

D4049a
$M_{SB(V)}$
S.B. current multiplying factor at the V_{CEO} max level
d=0.01
0.02
0.05
0.1
0.2
0.33
0.5
0.75
10^2
10
1
10^{-2}
10^{-1}
1
10
t_p (ms)
10^2


D4051
$V_{CE(sat)}$ (V)
Typical curves
T_j = 25 °C
I_C = 5A
4 A
3 A
2 A
1A
10
7.5
5
2.5
0
0
0.25
0.5
0.75
1
1.25
I_B(A)
1.5


D4052
I_C=5A
4A
3A
2A
1A
$V_{BE(sat)}$ (V)
1
0.75
0.5
0.25
0
0
0.5
1
I_B(A)
1.5
Typical curves
T_j=25°C


D4053a
V_{CE} = 750V
V_{BE} = 0V
I_{CES} (μA)
10^2
7
5
2
10
7
5
2
1
7
5
2
10^{-1}
typ
0
50
100
T_j(°C)
150


D5810
Typical curves
h_{FE}
100
75
50
25
0
V_{CE} = 5V, T_j =125°C
V_{CE} = 5V, T_j = 25°C
V_{CE} = 1V, T_j =125°C
V_{CE} = 1V, T_j = 25°C
10^{-1}
2
5
7
1
2
5
7
10
I_C(A)


D4056
15
10
5
0
f_T (MHz)
V_{CE}=10V
T_j=25°C
typ
10^{-2}
2
5
7
10^{-1}
2
5
7
1
2
5
7
10
I_C(A)

HIGH VOLTAGE SILICON TRANSISTORS

BU204
BU205
BU206

TENTATIVE DATA

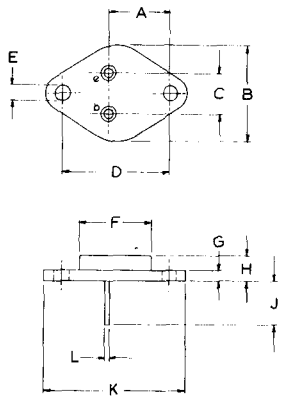
The BU204, 205 and 206 are N-P-N High voltage power transistors intended for use in line output stages of television receivers.

QUICK REFERENCE DATA

	BU204	BU205	BU206	
V_{CESM} max.	1300	1500	1700	V
I_C max. (d.c.)	2.5	2.5	2.5	A
P_{tot} max. ($T_{mb} \leq 90^oC$)	10	10	10	W
h_{FE} min.(V_{CE} = 5V; I_C = 2A)	2	2	1.8	
t_f typ. (I_C = 2A; I_B = 1A)	0.75	0.75	0.75	μs

OUTLINE AND DIMENSIONS

Conforms to BS3934 SO-5A/SB2-2
J.E.D.E.C. TO-3



	Millimetres		
	Min.	Nom.	Max.
A	-	16.9	-
B	-	-	26.6
C	-	10.9	-
D	-	30.1	-
E	4.0	-	4.2
F	-	-	20.3
G	-	3.15	-
H	-	-	9.5
J	11	-	13
K	-	-	39.5
L	-	1.0	-

Accessories available (High voltage types)

56336A insulated bushes, 56336B mica washer,

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

	BU204	BU205	BU206	
V_{CESM} max. (V_{BE} = 0)	1300	1500	1700	V
V_{CERM} max. ($R_{BE} \leq 100\Omega$)	1300	1500	1700	V
V_{CEO} max. (open base)	600	700	800	V
I_C max. (d.c.)	2.5	2.5	2.5	V
I_{CM} max. (peak value)	3.0	3.0	3.0	A
I_{BM} max. (peak value)	2.5	2.5	2.5	A
$-I_{BM}$ max. (peak value)* note 1	1.5	1.5	1.5	A
P_{tot} power dissipation (max) $T_{mb} \leq 90^{o}C$	10	10	10	W

TRANSIENT RATINGS (During flashover)

V_{CE} "Flashover"	1500	1650	1750	V
I_C "Flashover"	5	5	5	A

Temperature

T_{stg} range	-65 to +115	^{o}C
T_j (operating) max.	115	^{o}C

THERMAL CHARACTERISTICS

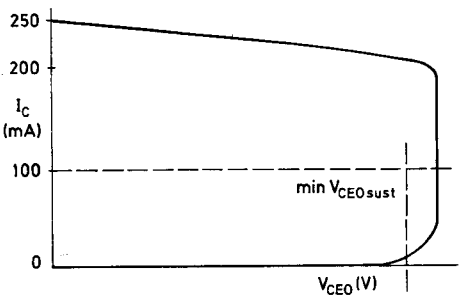
$R_{th(j-mb)}$	2.5	$^{o}C/W$
$R_{th(mb-h)}$ using mica washer 56336B	1.0	$^{o}C/W$

*Note 1

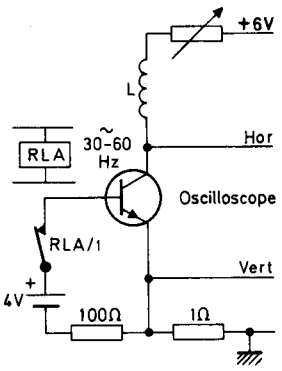
Turn off current in line deflection circuits.

ELECTRICAL CHARACTERISTICS (T_j = 25°C unless otherwise stated)

		BU204	BU205	BU206	
I_{CES}	Collector cut-off current (max) V_{BE} = 0; V_{CE} = V_{CESM}	1.0	1.0	1.0	mA
h_{FE} (min)	Static forward current transfer ratio (I_C = 2A; V_{CE} = 5V)	2	2	1.8	
$+V_{EBO}$	Emitter-base voltage (I_C = 0; I_E = 10mA) (min)	5	5	5	V
	(I_C = 0; I_E = 100mA) (typ)	7	7	7	V
$V_{CE(sat)}$	Collector emitter saturation voltage (max) (I_C = 2A; I_B = 1.0A)	5	5	-	V
	(I_C = 2A; I_B = 1.1A)	-	-	5	V
$V_{BE(sat)}$	Base-emitter saturation voltage (max) (I_C = 2A; I_B = 1.0A)	1.5	1.5	-	V
	(I_C = 2A; I_B = 1.1A)	-	-	1.5	V
$V_{CEO(sust)}$	Collector-emitter sustaining voltage (min) (I_B = 0; I_C = 100mA; L = 25mH)	600	700	800	V



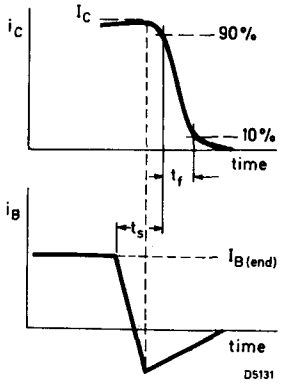
D5129

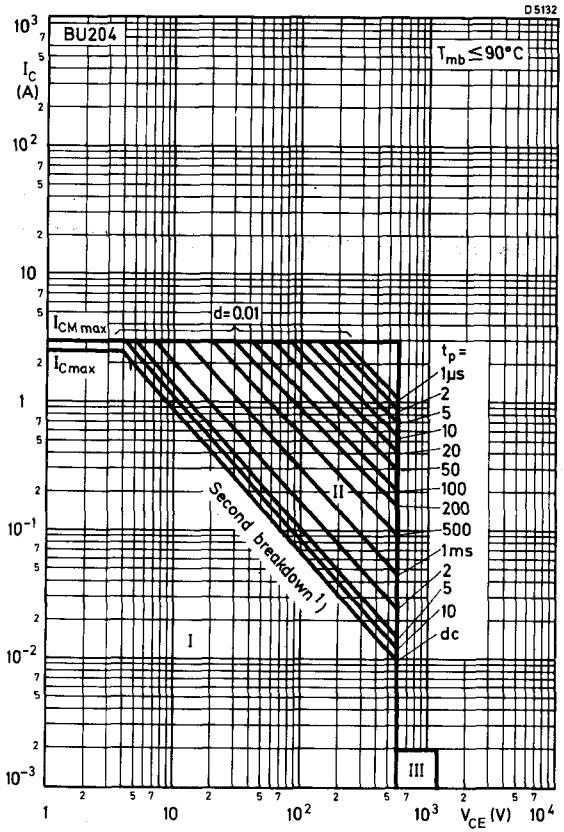


D5130

ELECTRICAL CHARACTERISTICS (cont)

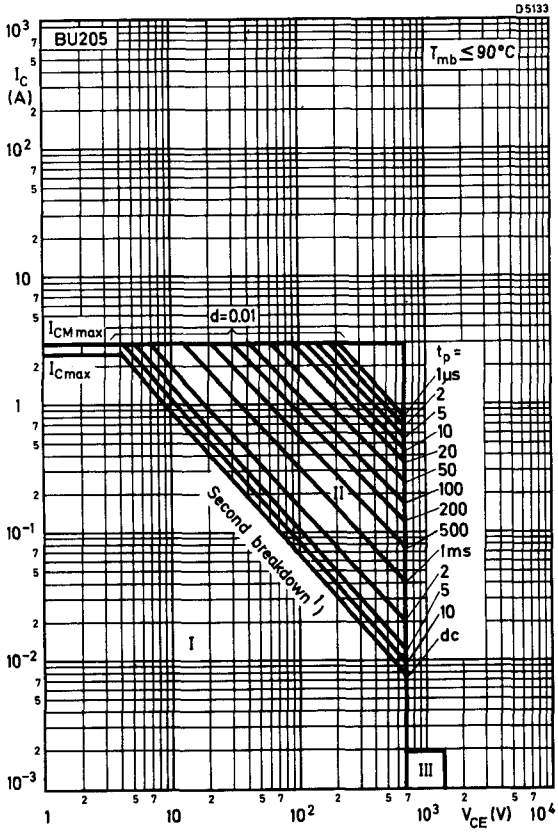
		BU204	BU205	BU206	
f_T	Transition frequency (typ) ($f = 5MHz$; $I_C = 0.1A$; $V_{CE} = 5V$)	7.5	7.5	7.5	MHz
C_{Tc}	Collector capacitance (typ) ($f = 1MHz$; $I_E = I_e = 0$; $V_{CB} = 10V$)	65	65	65	pF
	Switching times (in line deflection circuit) ($I_C = 2A$; $I_{B(end)} = 1A$; $L_B = 25\mu H$)				
t_f	Fall time (typ)	0.75	0.75	0.75	μs
t_s	Storage time (typ)	10	10	10	μs





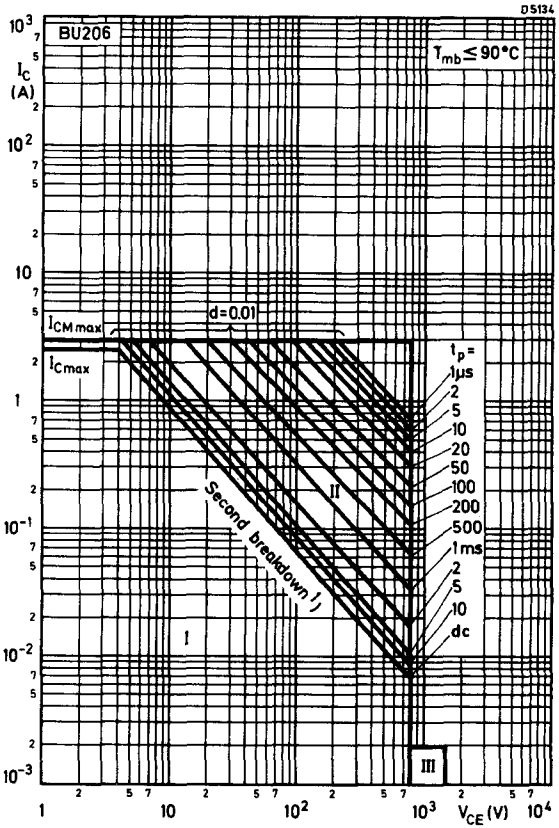
Safe Operation Area with the transistor forward biased.

I Region of permissible d. c. operation.
II Permissible extension for repetitive pulse operation.
III Repetitive pulse operation in this region is allowable, provided $R_{BE} \leq 100\Omega$; $t_p \leq 20\mu s$; $\delta \leq 0.25$.



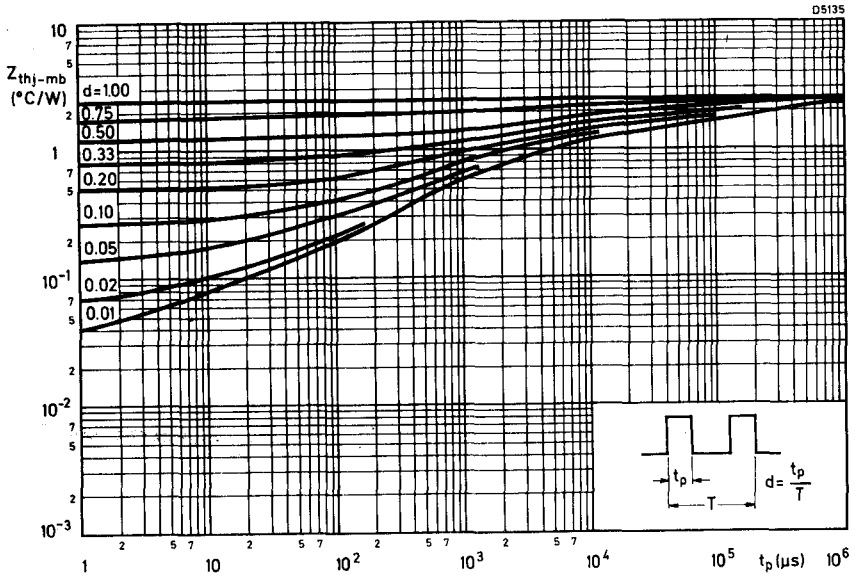
Safe Operation Area with the transistor forward biased.

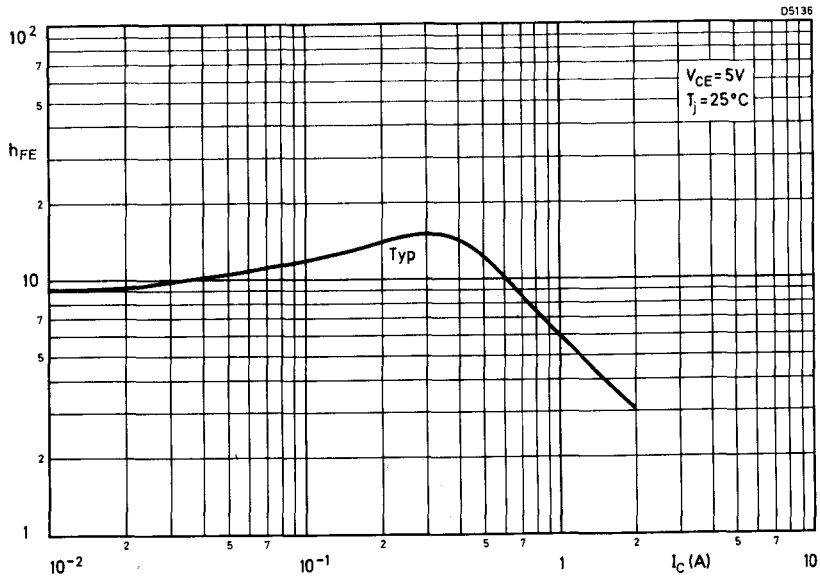
I Region of permissible d. c. operation.
II Permissible extension for repetitive pulse operation.
III Repetitive pulse operation in this region is allowable, provided $R_{BE} \leq 100\Omega$; $t_p \leq 20\mu s$; $\delta \leq 0.25$.

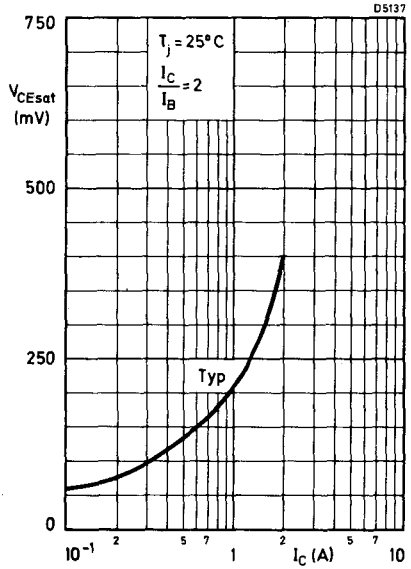


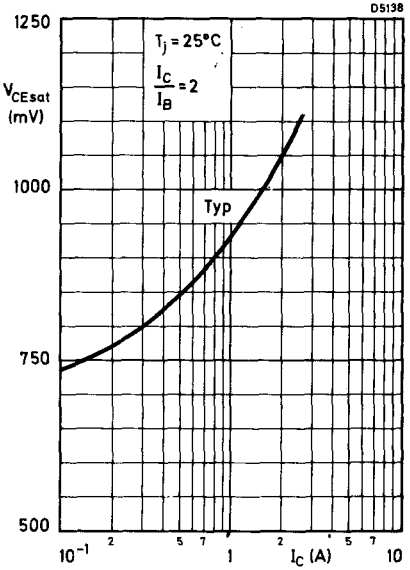
Safe Operating Area with the transistor forward biased.

I Region of permissible d.c. operation.
II Permissible extension for repetitive pulse operation.
III Repetitive pulse operation in this region is allowable, provided $R_{BE} \leq 100\Omega$; $t_p \leq 20\mu s$; $\delta \leq 0.25$.


D5135
Z_{thj-mb} (°C/W)
d=1.00
0.75
0.50
0.33
0.20
0.10
0.05
0.02
0.01
t_p
T
$d = \frac{t_p}{T}$
t_p (μs)


D5136
h_{FE}
V_{CE} = 5V
T_j = 25°C
Typ
I_C (A)


D5137
750
500
250
0
V_{CEsat} (mV)
T_j = 25°C
$\frac{I_C}{I_B}$ = 2
Typ
10^{-1}
2
5
7
1
2
5
7
10
I_C (A)


D5138
1250
1000
750
500
V_{CEsat} (mV)
T_j = 25°C
$\frac{I_C}{I_B}$ = 2
Typ
10^{-1}
2
5
7
1
2
5
7
10
I_C (A)

HIGH VOLTAGE SILICON TRANSISTORS

BU207
BU208
BU209

TENTATIVE DATA

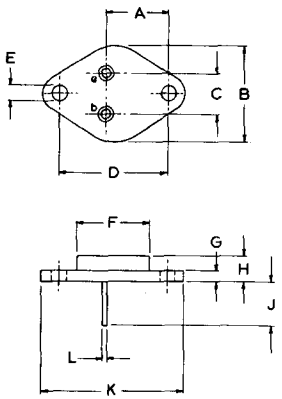
The BU207, 208 and 209 are N-P-N High voltage power transistors in metal envelopes intended for use in line output stages of colour television receivers.

QUICK REFERENCE DATA

		BU207	BU208	BU209	
V_{CESM} max.	(V_{BE} = 0; peak value)	1300	1500	1700	V
I_C max.	(d.c.)	5	5	4	A
P_{tot} max.	($T_{mb} \leq 95^oC$)	12.5	12.5	12.5	W
h_{FE} (min)	(I_C = 4.5A; V_{CE} = 5V)	2.25	2.25	-	
	(I_C = 3A; V_{CE} = 5V)	-	-	2.25	
t_f (typ)	(I_C = 4.5A; I_B = 1.8A)	0.9	0.7	-	μs
	(I_C = 3A; I_B = 1.3A)	-	-	0.7	μs

OUTLINE AND DIMENSIONS.

Conforms to BS3934 SO-5A/SB2-2
J.E.D.E.C. TO-3.



	Millimetres		
	Min.	Nom.	Max.
A	-	16.9	-
B	-	-	26.6
C	-	10.9	-
D	-	30.1	-
E	4.0	-	4.2
F	-	-	20.3
G	-	3.15	-
H	-	-	9.5
J	11	-	13
K	-	-	39.5
L	-	1.0	-

Accessories available (High voltage types)

56336A insulated bushes, 56336B mica washer.

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

	BU207	BU208	BU209	
V_{CESM} max. (V_{BE} = 0, peak value)	1300	1500	1700	V
V_{CERM} max. ($R_{BE} \leq 100\Omega$, peak value)	1300	1500	1700	V
V_{CEO} max. (open base)	600	700	800	V
I_C max. (d.c.)	5	5	4	A
I_{CM} max. (peak value)	7.5	7.5	6	A
I_{BM} max. (peak value)	4	4	4	A
$-I_{B(AV)}$ max. (d.c. or average over any 20ms period)	100	100	100	mA
$-I_{BM}$ max. (peak value, see note 1)	2.5	2.5	2.5	A
P_{tot} max. ($T_{mb} \leq 95^{o}C$)	12.5	12.5	12.5	W

TRANSIENT RATINGS (During flashover)

V_{CE} "Flashover"	1500	1650	1750	V
I_C "Flashover"	10	10	10	A

Temperature

T_{stg} range	-65 to +115	^{o}C
T_j (operating) max.	115	^{o}C

THERMAL CHARACTERISTIC

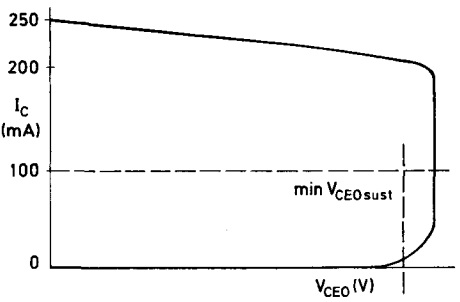
$R_{th(j-mb)}$ max.	1.6	$^{o}C/W$
$R_{th(mb-h)}$ with mica washer 56336B	1.0	$^{o}C/W$

Note 1

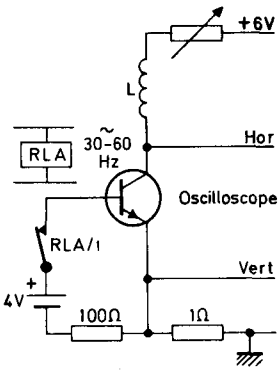
Turn off-current in line deflection circuits.

ELECTRICAL CHARACTERISTICS ($T_j = 25^oC$ unless otherwise stated)

		BU207	BU208	BU209	
I_{CES} max.	Collector cut-off current ($V_{BE} = 0$; $V_{CE} = V_{CESM}$ max)	1.0	1.0	1.0	mA
h_{FE} min.	Static forward current transfer ratio ($I_C = 4.5A$; $V_{CE} = 5V$)	2.25	2.25	-	
	($I_C = 3.0A$; $V_{CE} = 5V$)			2.25	
$+V_{EBO}$	Emitter-base voltage ($I_C = 0$; $I_E = 10mA$) min.	5	5	5	V
	($I_C = 0$; $I_E = 100mA$) typ.	7	7	7	V
$V_{CE(sat)}$ max.	Collector-emitter saturation voltage ($I_C = 4.5A$; $I_B = 2A$)	5	5	-	V
	($I_C = 3A$; $I_B = 1.3A$)	-	-	5	V
$V_{BE(sat)}$ max.	Base-emitter saturation voltage ($I_C = 4.5A$; $I_B = 2A$)	1.5	1.5	-	V
	($I_C = 3A$; $I_B = 1.3A$)	-	-	1.5	V
$V_{CEO(sust)}$	Collector-emitter sustaining voltage $I_B = 0$; $I_C = 100mA$; $L = 25mH$	600	700	800	V



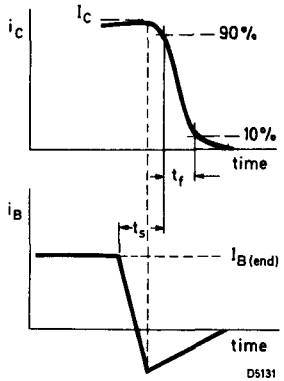
D5129

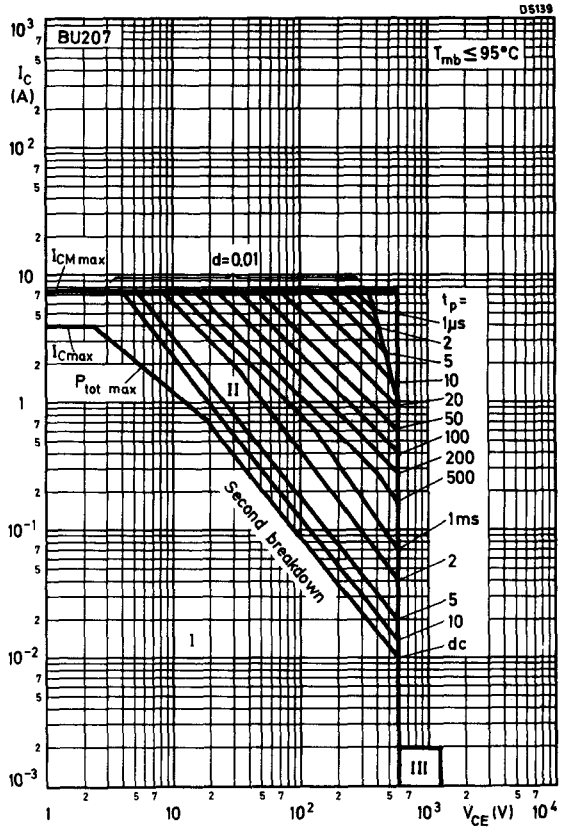


D5130

ELECTRICAL CHARACTERISTICS (cont)

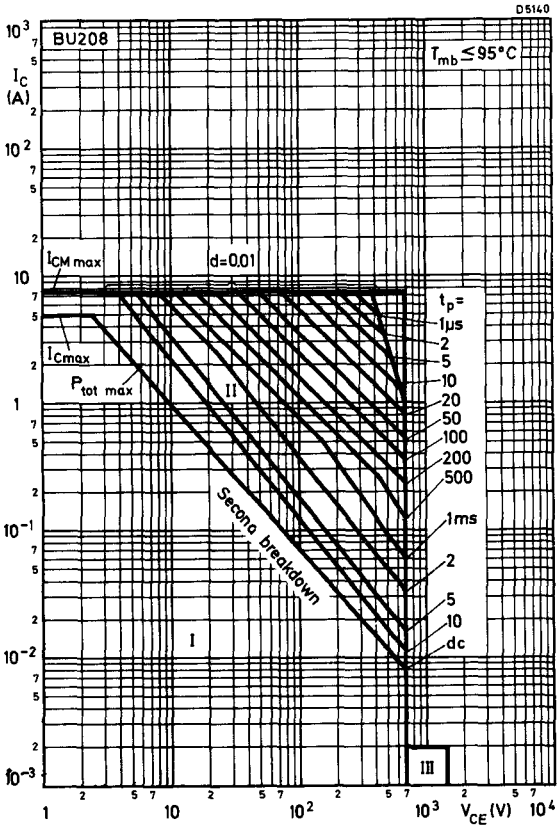
		BU207	BU208	BU209	
f_T (typ)	Transition frequency ($f = 5MHz$; $I_C = 0.1A$, $V_{CE} = 5V$)	7	7	7	MHz
C_{Tc} (typ)	Collector capacitance ($f = 1MHz$; $I_E = I_e = 0$; $V_{CB} = 10V$)	125	125	125	pF
	Switching times (in line deflection circuit) ($L_B = 10\mu H$)				
t_f (typ)	Fall time				
	$I_C = 4.5A$; $I_{B(end)} = 1.8A$	0.9	0.7	-	μs
	$I_C = 3.0A$; $I_{B(end)} = 1.3A$	-	-	0.7	μs
t_s (typ)	Storage time				
	$I_C = 4.5A$; $I_{B(end)} = 1.8A$	10	10	-	μs
	$I_C = 3.0A$; $I_{B(end)} = 1.3A$	-	-	10	μs





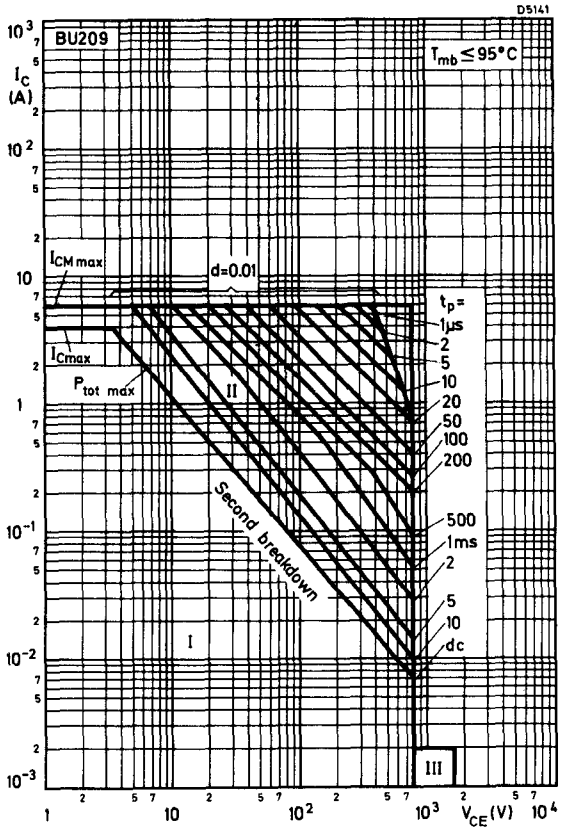
Safe Operating Area with the transistor forward biased.

I Region of permissible d.c. operation.
II Permissible extension for repetitive pulse operation.
III Repetitive pulse operation in this region is allowable, provided $R_{BE} \leq 100\Omega$; $t_p \leq 20\mu s$; $\delta \leq 0.25$.



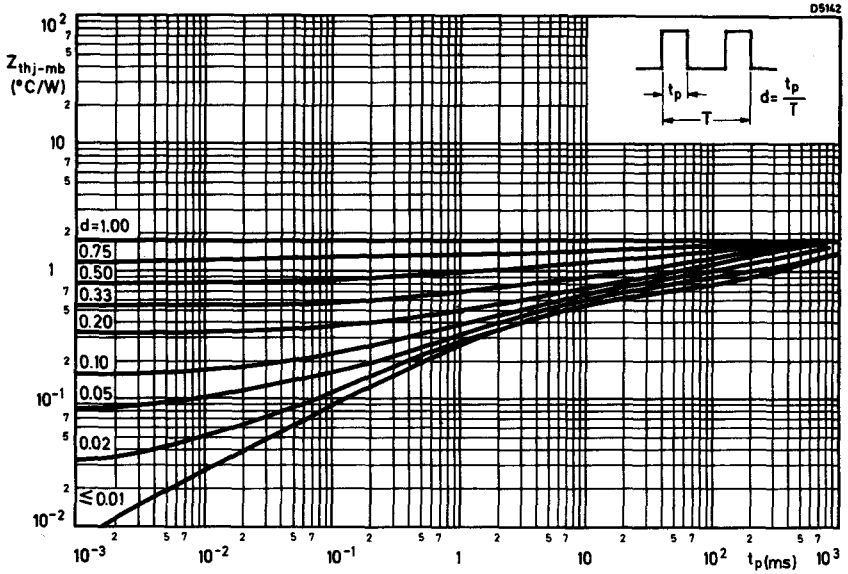
Safe Operating Area with the transistor forward biased.

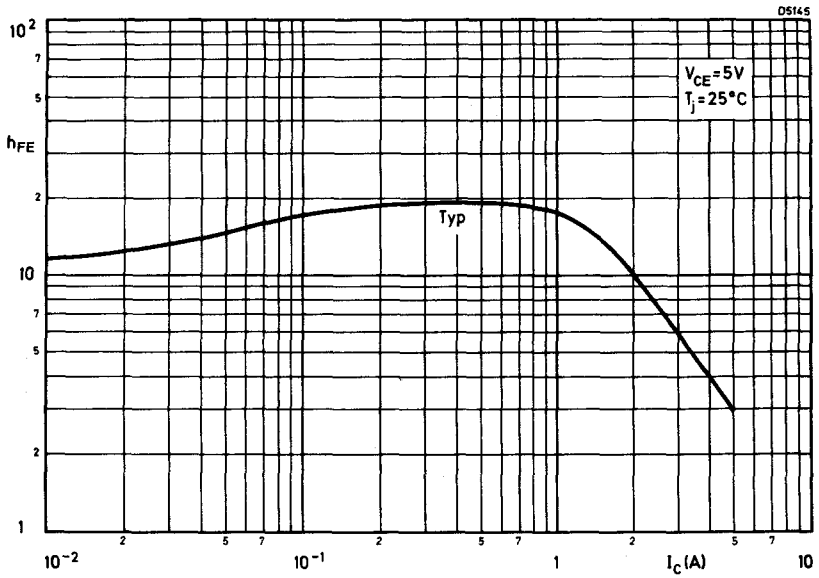
I Region of permissible d. c. operation.
II Permissible extension for repetitive pulse operation.
III Repetitive pulse operation in this region is allowable, provided $R_{BE} \leq 100\Omega$; $t_p \leq 20\mu s$; $\delta \leq 0.25$.

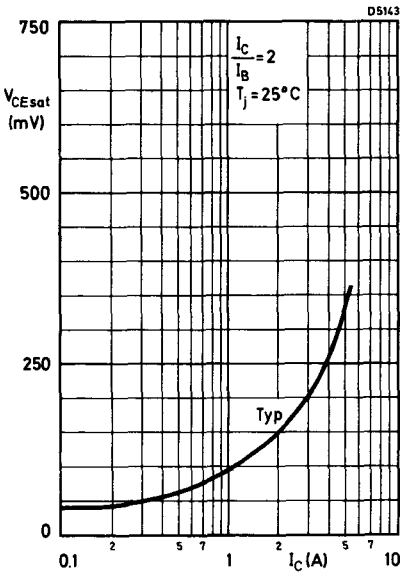


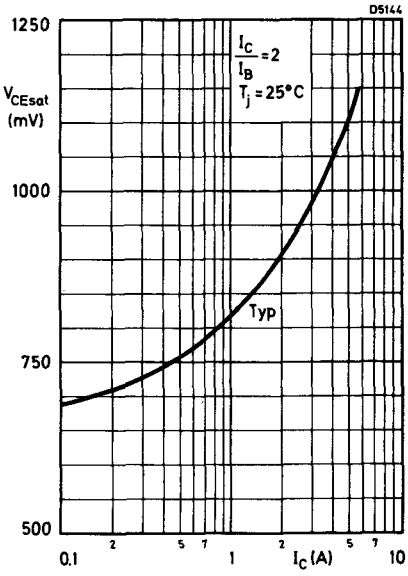
Safe Operating Area with the transistor forward biased.

I Region of permissible d. c. operation.
II Permissible extension for repetitive pulse operation.
III Repetitive pulse operation in this region is allowable, provided $R_{BE} \leq 100\Omega$; $t_p \leq 20\mu s$; $\delta \leq 0.25$.


DS142
Z_{thj-mb} (°C/W)
10^2
10
1
10^{-1}
10^{-2}
d=1.00
0.75
0.50
0.33
0.20
0.10
0.05
0.02
≦0.01
t_p
T
d= $\frac{t_p}{T}$
10^{-3}
10^{-2}
10^{-1}
1
10
10^2
t_p(ms)
10^3


DS145
h_{FE}
10^2
10
1
V_{CE}=5V
T_j=25°C
Typ
10^{-2}
10^{-1}
1
I_C(A)
10


D5143
750
500
250
0
V_{CEsat} (mV)
$\frac{I_C}{I_B} = 2$
$T_j = 25°C$
Typ
0.1
2
5
7
1
2
5
7
10
I_C (A)


D5144
1250
1000
750
500
V_{CEsat} (mV)
$\frac{I_C}{I_B} = 2$
$T_j = 25°C$
Typ
0.1
2
5
7
1
2
5
7
10
I_C (A)

OC28 OC29 OC35 OC36

QUICK REFERENCE DATA

Power junction transistors of the p-n-p alloy type intended for use in medium and high voltage and high current switching applications. Matched pairs of each type are available under the type number 2-OC

	OC28	OC29	OC35	OC36	
V_{CB} max. (I_E = 0A)	–80	–60	–60	–80	V
V_{CE} max. (I_E = 0.5A)	–60	–48	–48	–60	V
V_{CE} max. (I_E = 6.0A)	–60	–32	–32	–32	V
h_{FE} (I_C = 1.0A)	20–55	45–130	25–75	30–110	

Unless otherwise shown, data is applicable to all types

ABSOLUTE MAXIMUM RATINGS

The equipment designer must ensure that no transistor exceeds these ratings. In arriving at the actual operating conditions, variations in supply voltages, component tolerances and ambient temperatures must also be taken into account.

Collector voltage

	OC28	OC29	OC35	OC36	
V_{CB} max. (I_E = 0A)	–80	–60	–60	–80	V
V_{CE} max. (I_E = 0.5A)	–60	–48	–48	–60	V
V_{CE} max. (I_E = 6.0A)	–60	–32	–32	–32	V

Collector current

I_{CM} max.	10	A
†$I_{C(AV)}$ max.	8.0	A

Emitter current

I_{EM} max.	12	A
†$I_{E(AV)}$ max.	9.0	A

Reverse emitter-base voltage

V_{EB} max. (I_C = 0A)	–40	–20	–20	–40	V

Base current

I_{BM} max.	2.0	A
†$I_{B(AV)}$ max.	1.0	A

Total Dissipation at $T_{case} \leqslant 45°C$ 30 W

$T_{case} > 45°C$ $\quad P_{tot}$ max. $= \dfrac{T_j \text{ max} - T_{case}}{\theta_{j-case}}$

†Averaged over any 20ms period.

Temperature ratings

T_{stg} max.	75	°C
T_{stg} min.	−55	°C
T_j max. (Continuous operation)	90	°C
‡T_j max. (Intermittent operation total duration 200 hours)	100	°C
$\theta_{j\text{-case}}$ max.	1.5	°C/W
$\theta_{case\text{-heat sink}}$ max. (when mounted with metal washer 0.127mm thick and with mica washer)	0.5	°C/W

‡Likelihood of full performance of a circuit at this temperature is also dependent on the type of application.

CHARACTERISTICS at T_{case} = 25°C

			Typical production spread Min.	Typ.	Max.	
Common base						
Collector leakage current (V_{CB} = −500mV, I_E = 0mA)	I_{CBO}		—	—	100	μA
(V_{CB} = −14V, I_E = 0mA, T_{case} = 100°C)			—	—	20	mA
(V_{CB} = −60V, I_E = 0mA, T_{case} = 100°C)		OC29, OC35	—	8.5	30	mA
(V_{CB} = −80V, I_E = 0mA T_{case} = 100°C)		OC28, OC36	—	12	30	mA
Emitter cut-off voltage (V_{CB} = −48V, I_E = 0mA, T_{case} = 100°C)	V_{EB}		—	—	−500	mV
Common emitter						
Collector knee voltage at I_C = 6A (see Fig. 1)	$V_{CE(knee)}$		—	−0.5	−1.0	V

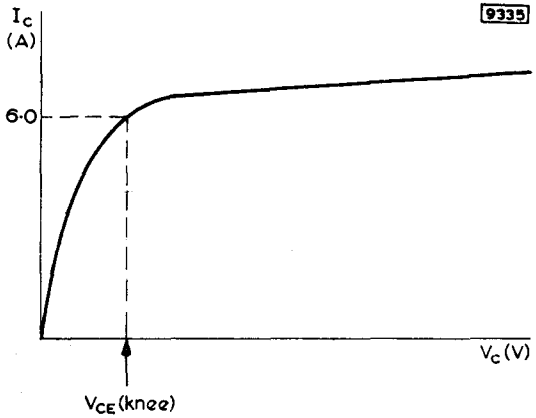


Fig. 1

		OC28		OC29		OC35		OC36		
Base current	I_B	*min.*	*max.*	*min.*	*max.*	*min.*	*max.*	*min.*	*max.*	
(V_{CB} = 0V, I_E = 1A)		17.5	50	7.2	21.5	13	38	9	33	mA
(V_{CB} = 0V, I_E = 6A)		190	375	73	165	130	285	90	285	mA
Base input voltage	V_{BE}									
(V_{CB} = 0V, I_E = 1A)		←			800				→	mV
(V_{CB} = 0V, I_E = 6A)		–0.6	–1.6	—	–1.6	–0.4	–1.4	—	–1.6	V
Current amplification factor	h_{FE}									
(V_{CE} = –14V, I_C = 30mA)		20	—	—		—		—		
(V_{CE} = –1V, I_C = 1A)		20	55	45	130	25	75	30	110	
(V_{CE} = –1V, I_C = 6A)		15	30	35	80	20	45	20	65	

BASIC PARAMETERS

Cut-off frequency					
(V_{CB} = –6V, I_E = 300mA)	f_{hfb}	—	250	—	kc/s
Collector depletion capacitance					
(V_{CB} = –12V, I_E = 0mA)	c_{tc}	—	160	—	pF
Emitter depletion capacitance					
(V_{EB} = –6V, I_E = 0mA)	c_{te}	—	165	—	pF
Time constant, current feed	$\frac{\beta}{\omega 1}$				
(V_{CE} = –4V, I_{CM} = 1A)		—	45	70	μs
(V_{CE} = –4V, I_{CM} = 6A)		—	30	50	μs
Desaturation time constant					
(V_{CE} = 0V, I_{BM} = 50mA)	τ_s	—	30	50	μs

Typical operation in on-off power switching circuit

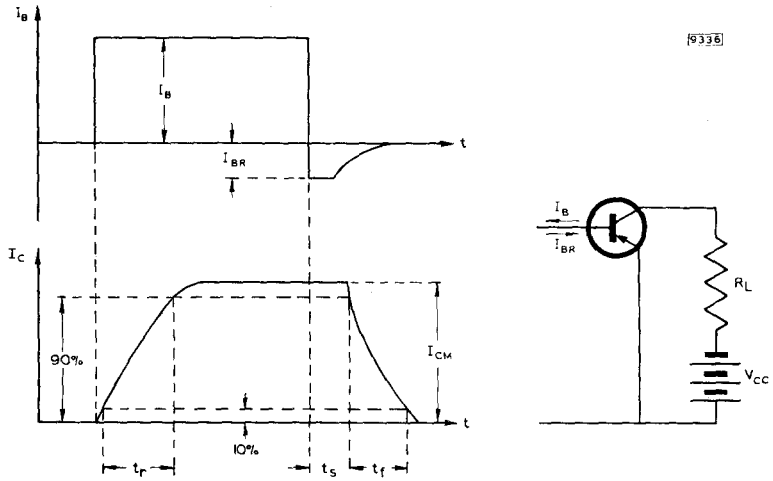


Fig. 2

D.C. supply voltage	V_{CC}	14				28			V
Load resistance	R_L	14		2.3		28		4.7	Ω
peak collector current	I_{CM}	1.0		6.0		1.0		6.0	A
		OC29	OC35	OC29	OC35	OC28	OC36	OC28	OC36
'Turn On' base current	I_B	35	55	260	400	70	50	480	400 mA
'Reverse' base current	I_{BR}	8.7	13.7	65	100	17.5	12.5	120	100 mA
Switching times									
Rise time	t_r	20		20		20		20	µs
Storage time	t_s	15		15		15		15	µs
Fall time	t_f	40		35		40		35	µs

Rise time $t_r = \frac{\beta}{\omega 1} \log_e \frac{h_{FE} |I_B|}{h_{FE} |I_B| - |I_{CM}|}$

Fall time $t_f = \frac{\beta}{\omega 1} \log_e \left[1 + \frac{|I_{CM}|}{h_{FE} |I_{BR}|} \right]$

Storage time $t_s = \tau_s \log_e \frac{|I_B| + |I_{BR}|}{\frac{|I_{CM}|}{h_{FE}} + |I_{BR}|}$

CHARACTERISTICS OF MATCHED PAIR

(measured at $T_{case} = 25°C$)

Ratio of the current amplification factors of the two transistors

at $V_{CB} = 0V$, $I_C = 300mA$	1.2 : 1	
$V_{CB} = 0V$, $I_C = 6A$	1.2 : 1	

Difference between the base-emitter voltages of the two transistors

at $V_{CB} = -14V$, $I_C = 30mA$	<35	mV
$V_{CB} = 0V$, $I_C = 6A$	<300	mV

OPERATING NOTES

1. **Dissipation and heat sink considerations**

The maximum total dissipation P_{tot} max. $= (V_{CE} \times I_C) + (V_{BE} \times I_B)$, is given by the relationship:—

$$P_{tot} \text{ max.} = \frac{T_j \text{ max.} - T_{amb}}{\theta_m + \theta_i + \theta_h}$$

Where $\theta_m + \theta_i + \theta_h$ is equal to $\theta_{j\ amb}$.
The various components of $\theta_{j\ amb}$ are illustrated below:

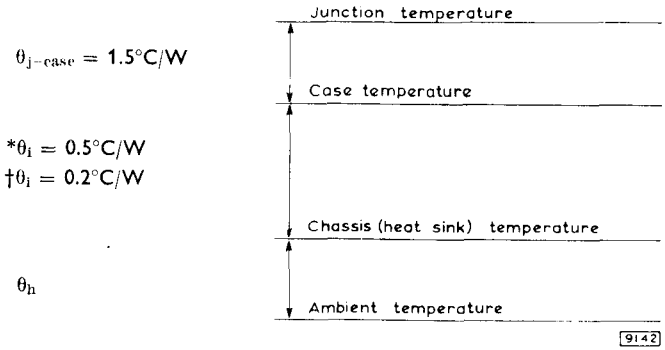


Fig. 3

*When mounted with a metal washer 0.127mm thick and a mica washer, or with a mica washer only and silicone grease, $\theta_i = 0.5°C/W$. This value applies when the transistor is bolted down evenly on a flat heat sink. The metal washer is advantageous in taking up any irregularities in the heat sink surfaces.

†When mounted directly on the chassis with a thin film of silicone grease between the contacting surfaces, $\theta_i = 0.2°C/W$. This value applies when the transistor is bolted down evenly on a flat heat sink.

θ_h depends on the cooling conditions under which the transistor is used, i.e., dimensions, position and surface conditions of heat sink, etc. An air-cooled heat sink (7in. × 7in. × 1/16in. blackened aluminium) will have a value of $\theta_h = 2.2°C/W$.

θ_h can be determined for a given collector dissipation and ambient temperature by measuring the case temperature.

$$\theta_h = \frac{T_{case} - T_{amb}}{P_{tot}} - \theta_i °C/W$$

The following example illustrates the temperatures which occur at various points on the transistor at $p_C = 10W$, $T_j = 90°C$, $\theta_h = 2.2°C/W$.

T_j	$= 90°C$
T_{case}	$= 90-(10 \times 1.5) = 75°C$
$T_{heat\ sink}$	$= 75-(10 \times 0.5) = 70°C$
T_{amb}	$= 70-(10 \times 2.2) = 48°C$

The suitability of any design can be checked by measuring, with a thermocouple, the case temperature of the transistor operating at the selected collector dissipation and maximum ambient temperature. The point defined by the case temperature and the total dissipation must lie within the shaded area shown on the graph on page C10. If the point lies outside the shaded area the design is inadmissible and the dissipation must be reduced or the heatsink improved. The selected total dissipation should be the maximum attained by any transistor in the design being checked.

2. Transistors may be soldered directly into the circuit but the heat conducted to the junction should be kept to a minimum by the use of a thermal shunt.

3. Transistors may be dip soldered at a solder temperature of 240°C for a maximum of 10 seconds up to a point 2mm from the seal.

4. Care must be taken to ensure good thermal contact between the transistor and heat sink. Burrs or thickening at the edges of the four holes must be removed and the transistor bolted down on a plane surface.

MECHANICAL DATA

Dimensions – see page D8.

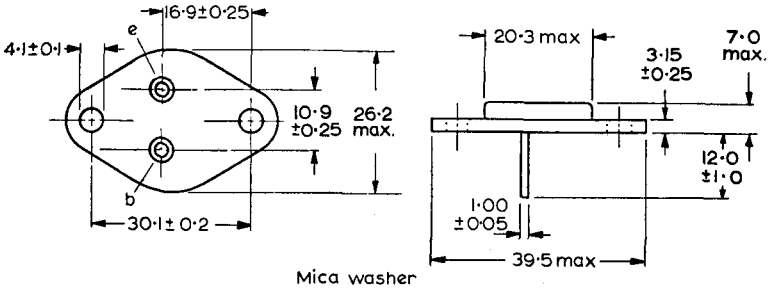
Average weight { 0.66 oz / 18.6 g

ACCESSORIES

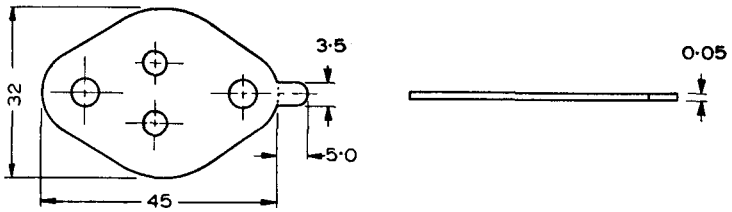
Accessories must be specifically ordered.

Accessory	Code No.	Notes
2 insulating bushes	56201a	Obtainable in packs for 10 or 100 transistors.
1 mica washer	56201b	
1 metal washer	56214	

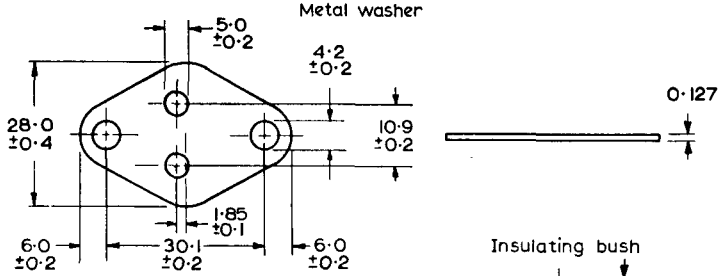
Transistor

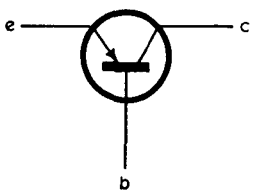


Mica washer

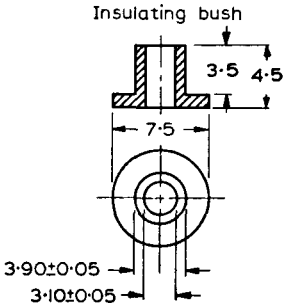


Metal washer



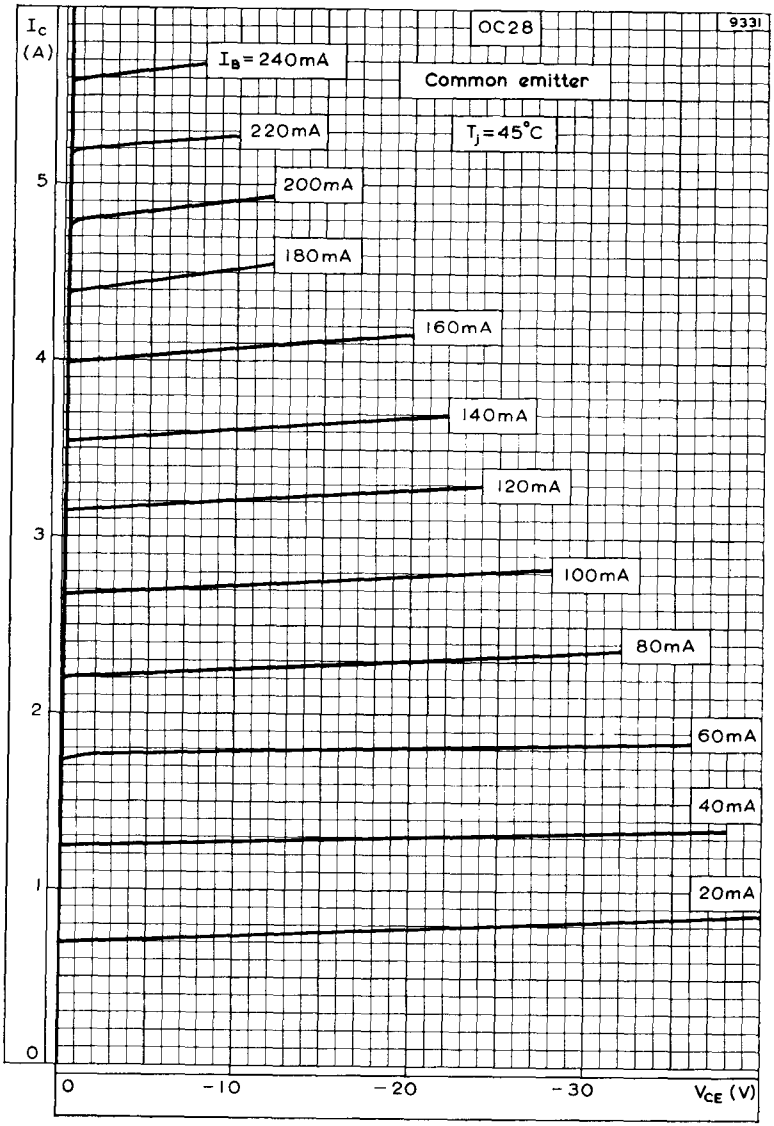


Insulating bush

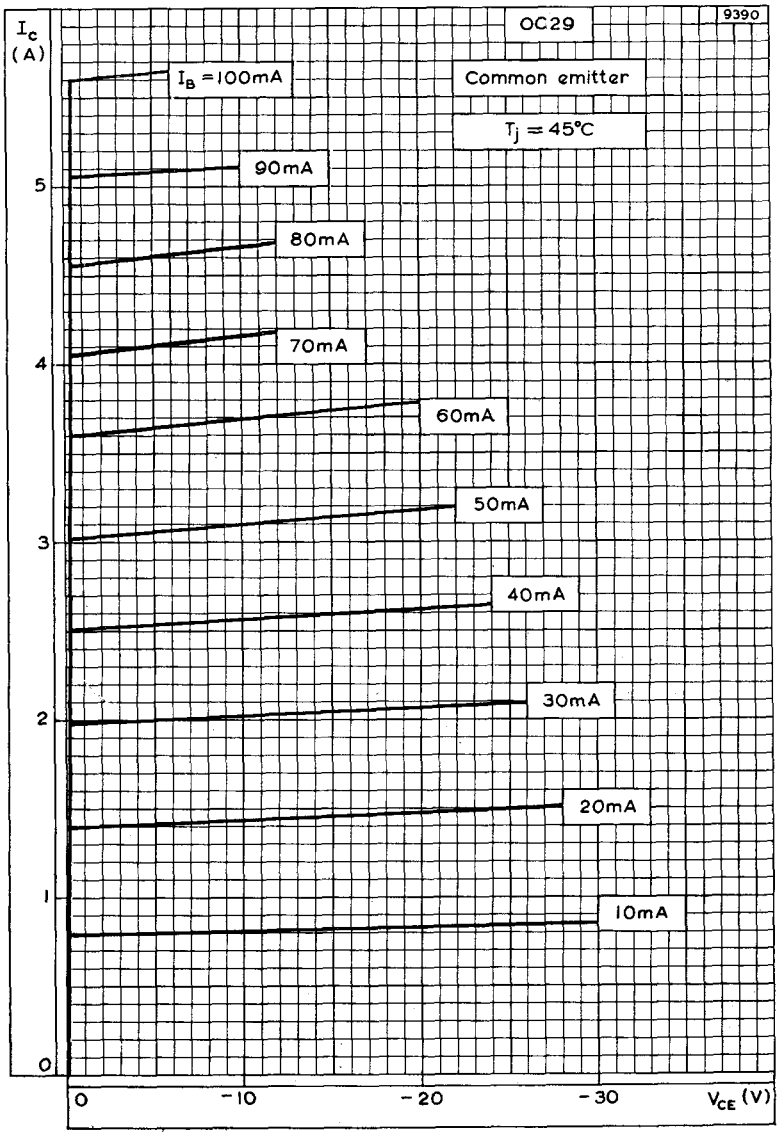


8484

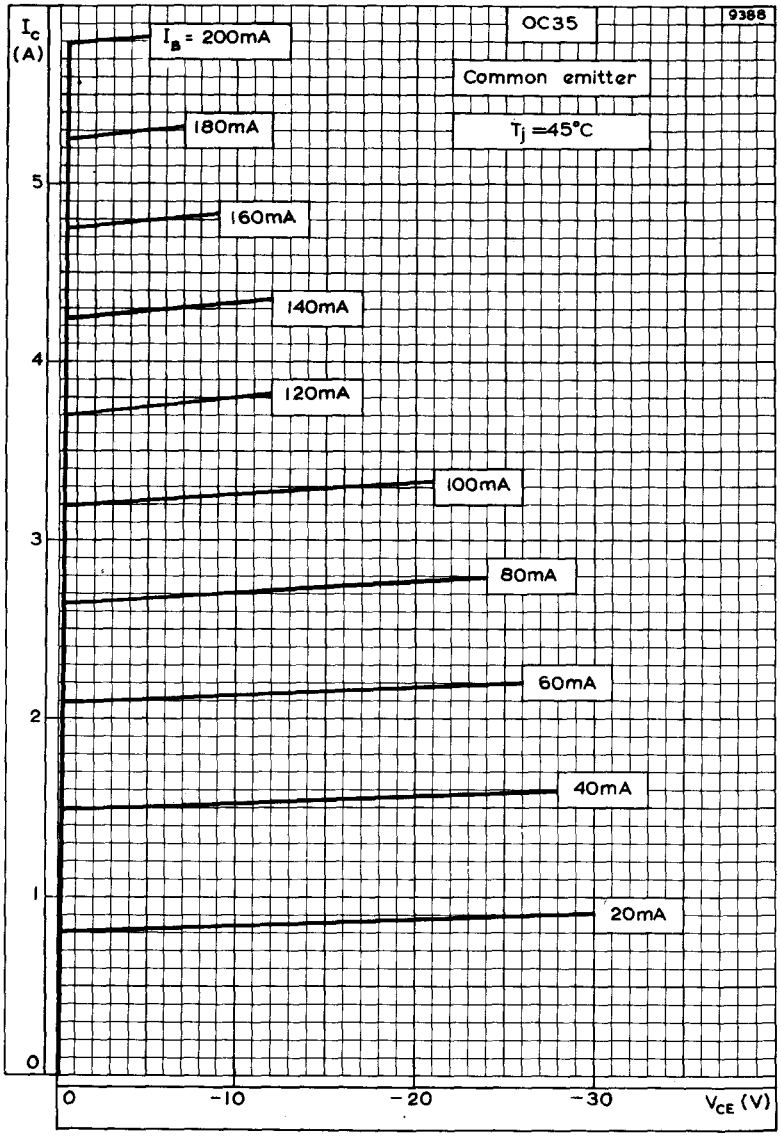
All dimensions in mm



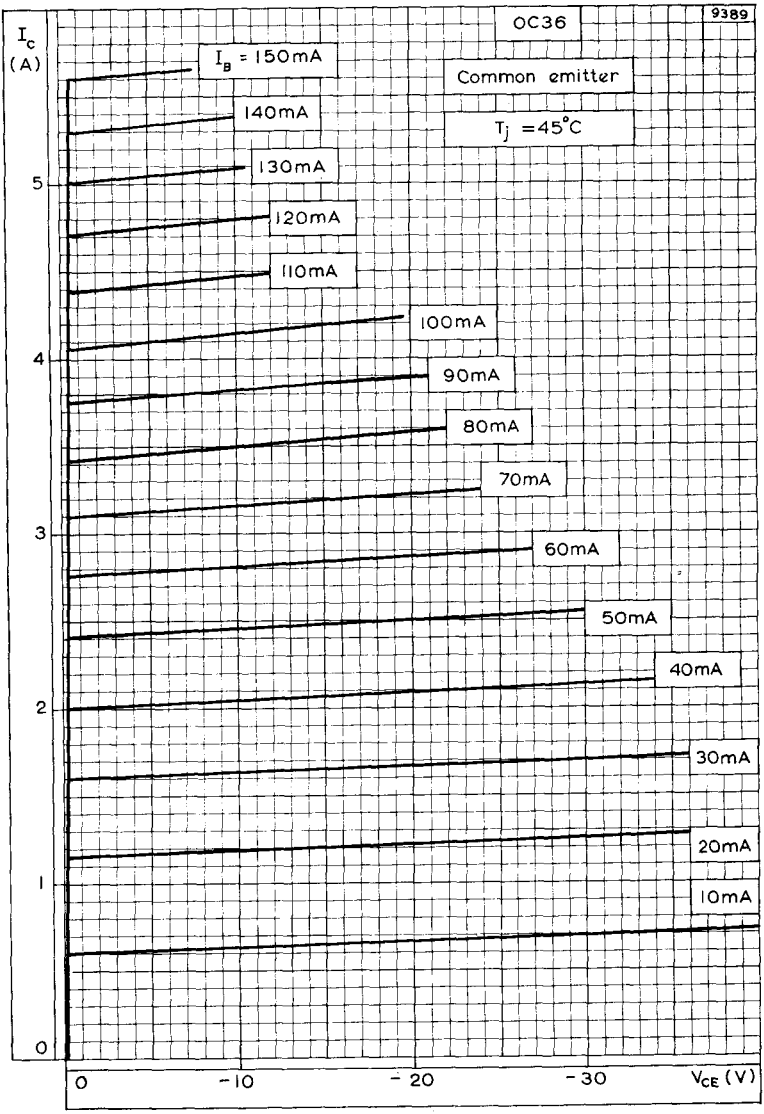
OUTPUT CHARACTERISTIC FOR OC28. COMMON EMITTER



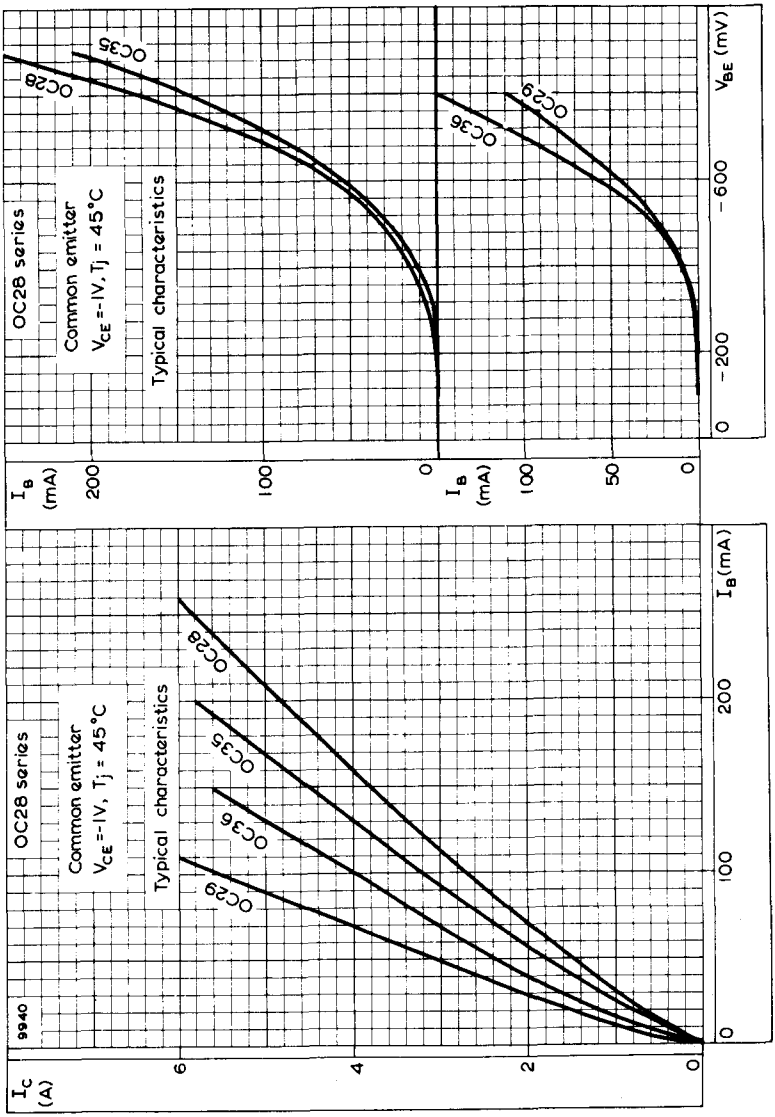
OUTPUT CHARACTERISTIC FOR OC29. COMMON EMITTER



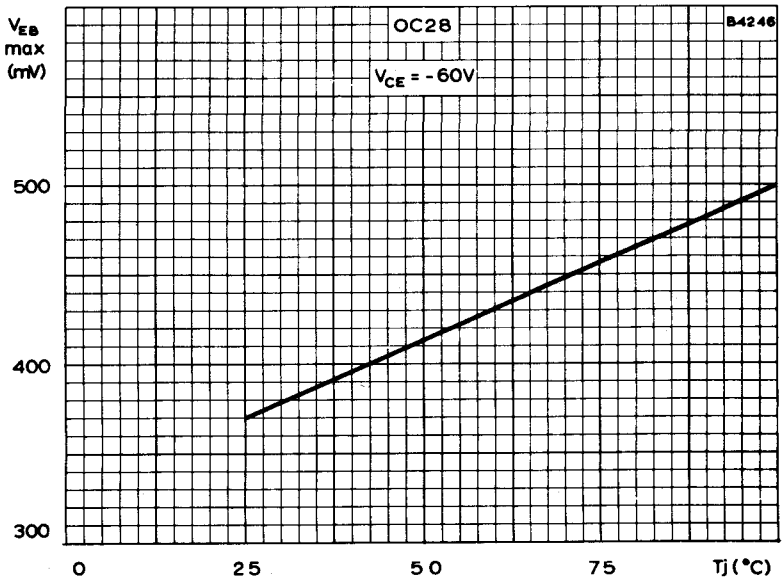
OUTPUT CHARACTERISTIC FOR OC35. COMMON EMITTER

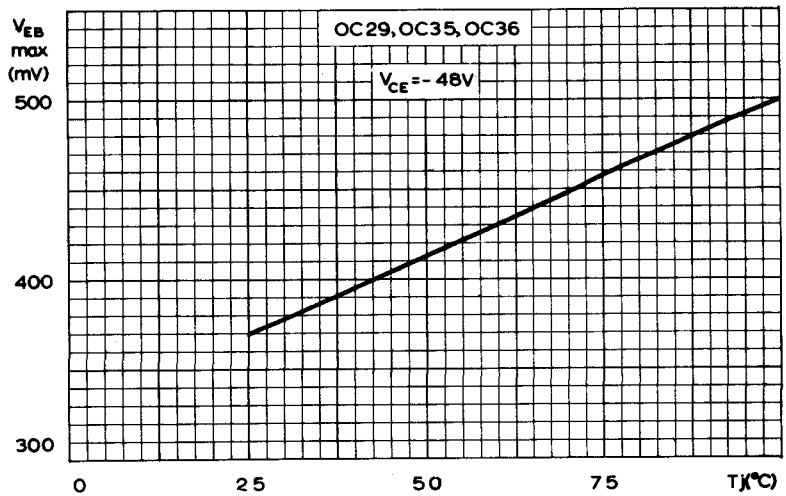


OUTPUT CHARACTERISTIC FOR OC36. COMMON EMITTER

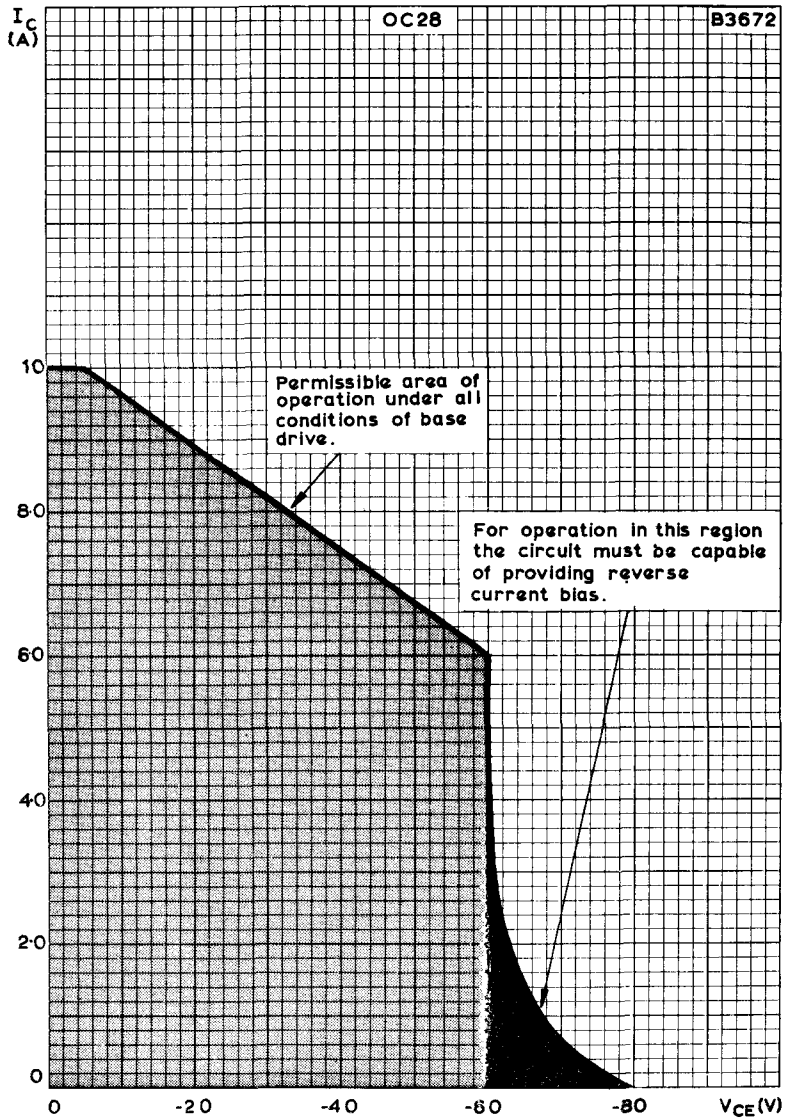


TRANSFER AND INPUT CHARACTERISTICS. COMMON EMITTER

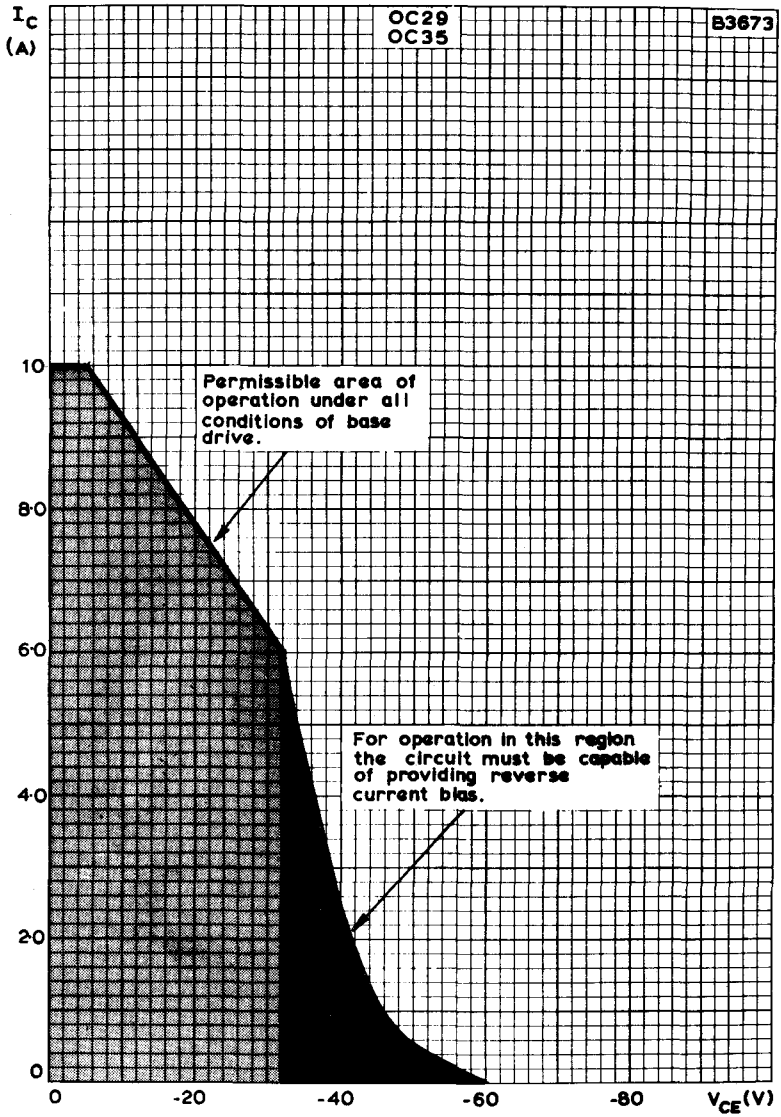




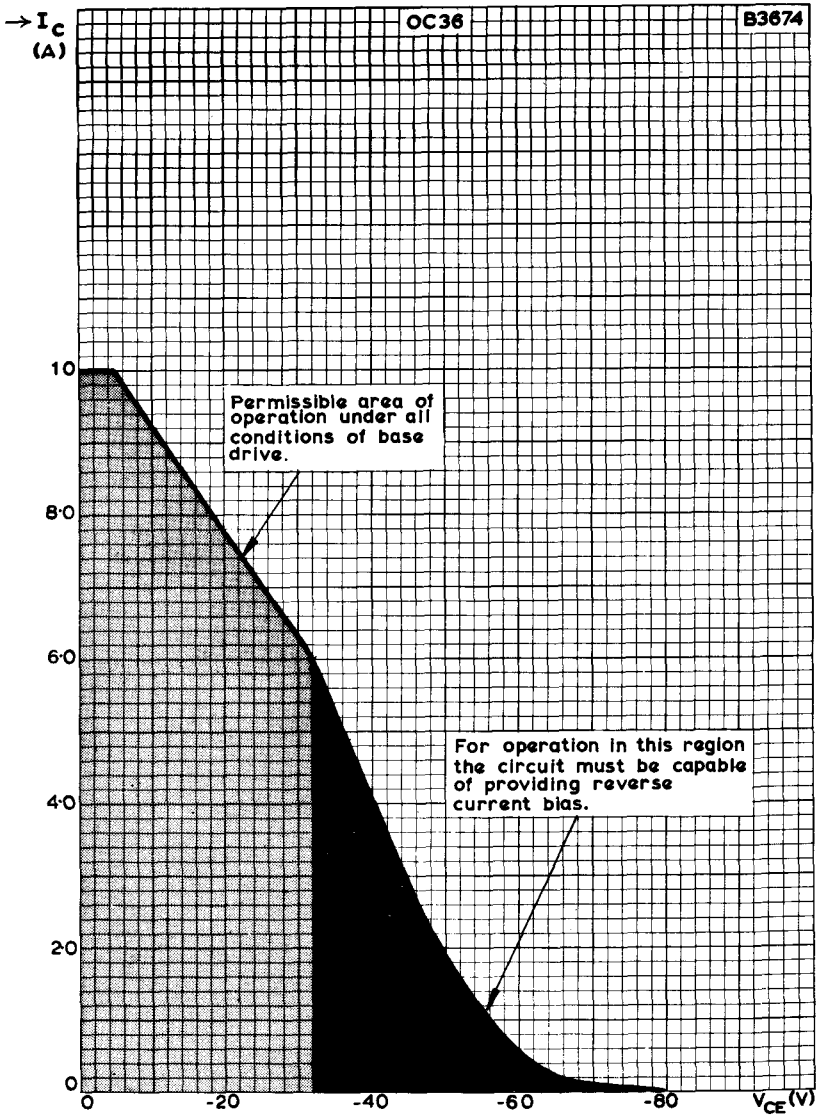
VARIATION OF MAXIMUM EMITTER-BASE CUT-OFF VOLTAGE WITH JUNCTION TEMPERATURE



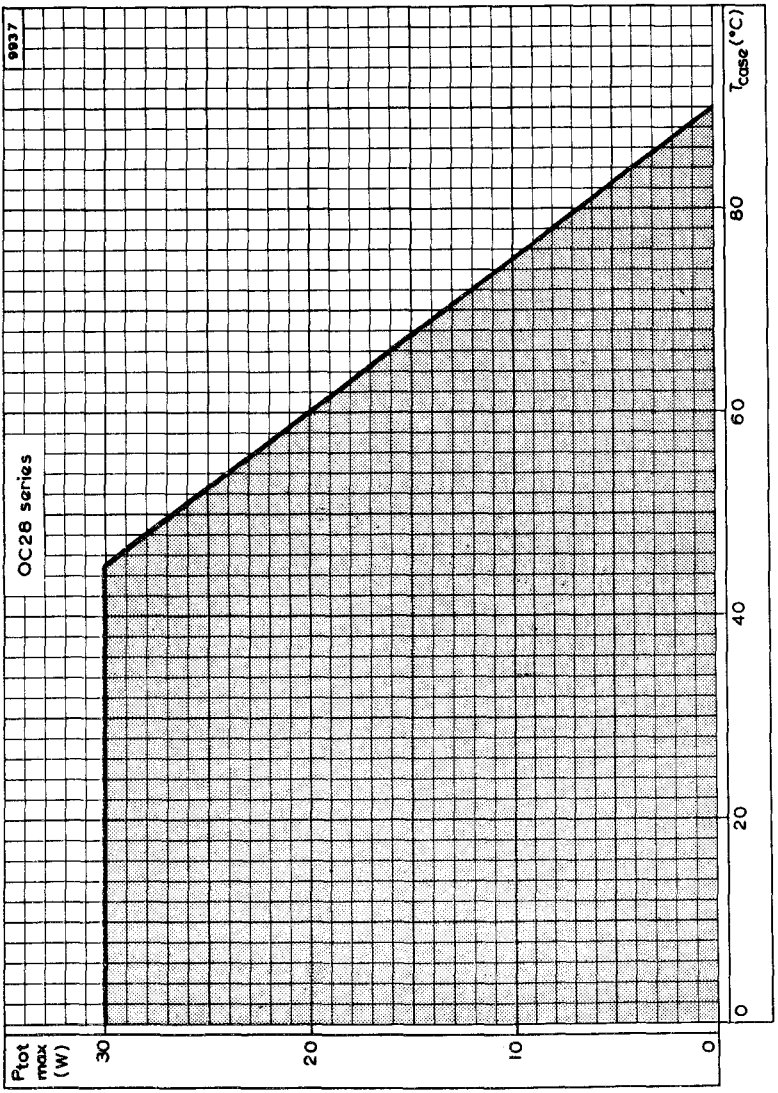
COLLECTOR CURRENT PLOTTED AGAINST ABSOLUTE MAXIMUM COLLECTOR-EMITTER VOLTAGE. OC28



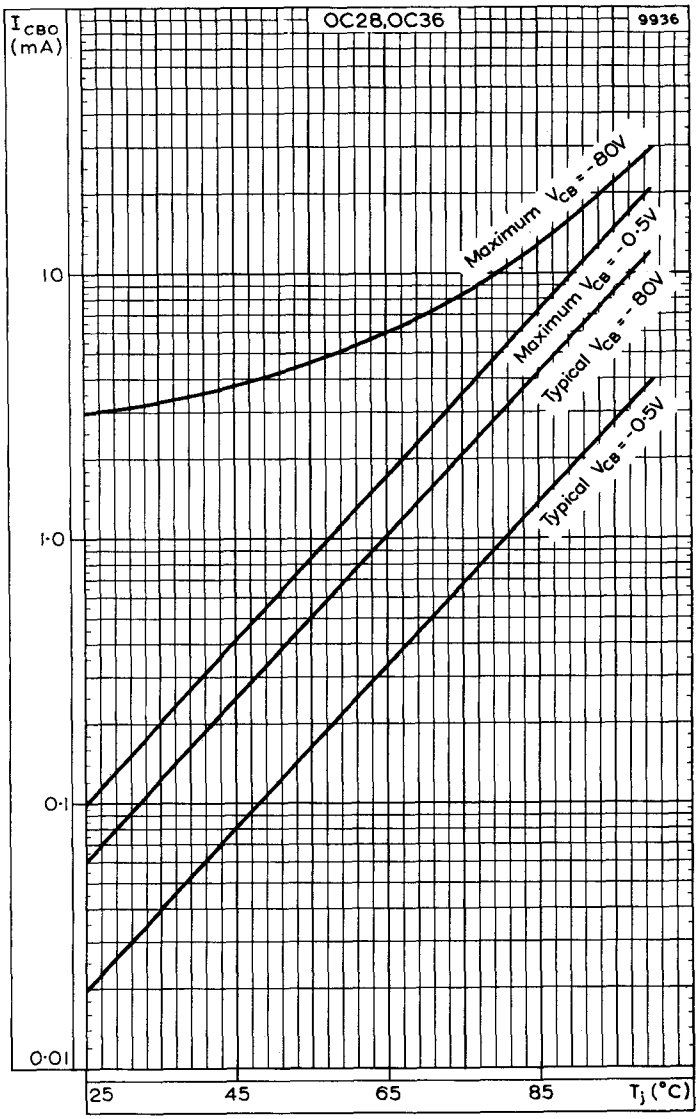
COLLECTOR CURRENT PLOTTED AGAINST ABSOLUTE MAXIMUM COLLECTOR-EMITTER VOLTAGE. OC29, OC35



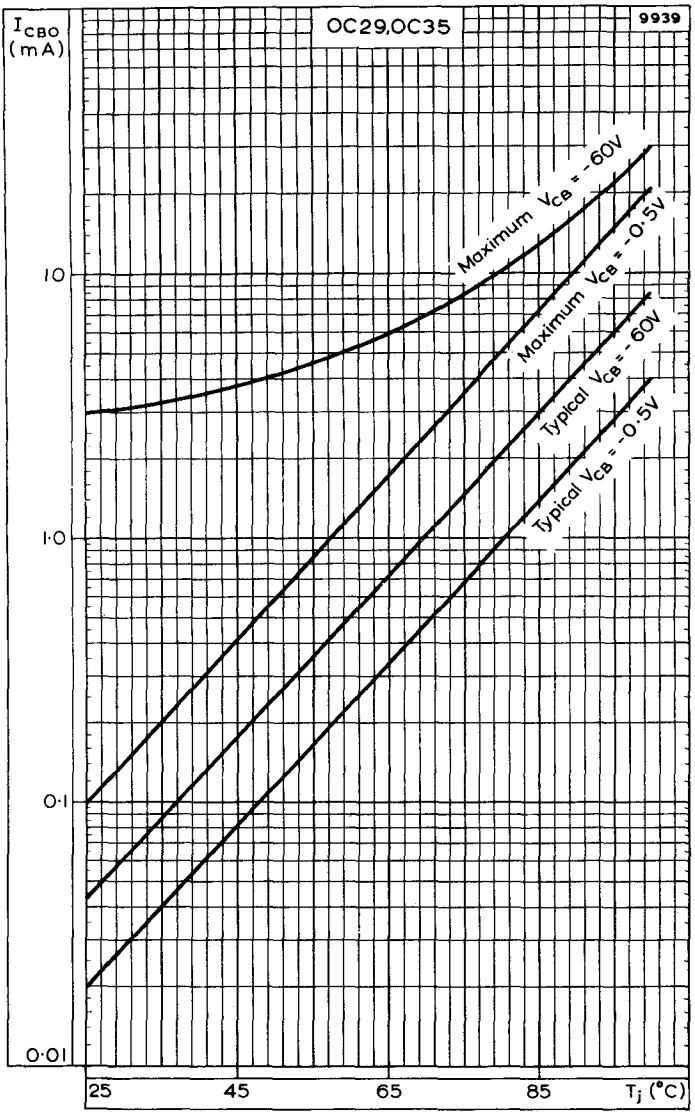
COLLECTOR CURRENT PLOTTED AGAINST ABSOLUTE MAXIMUM COLLECTOR-EMITTER VOLTAGE. OC36



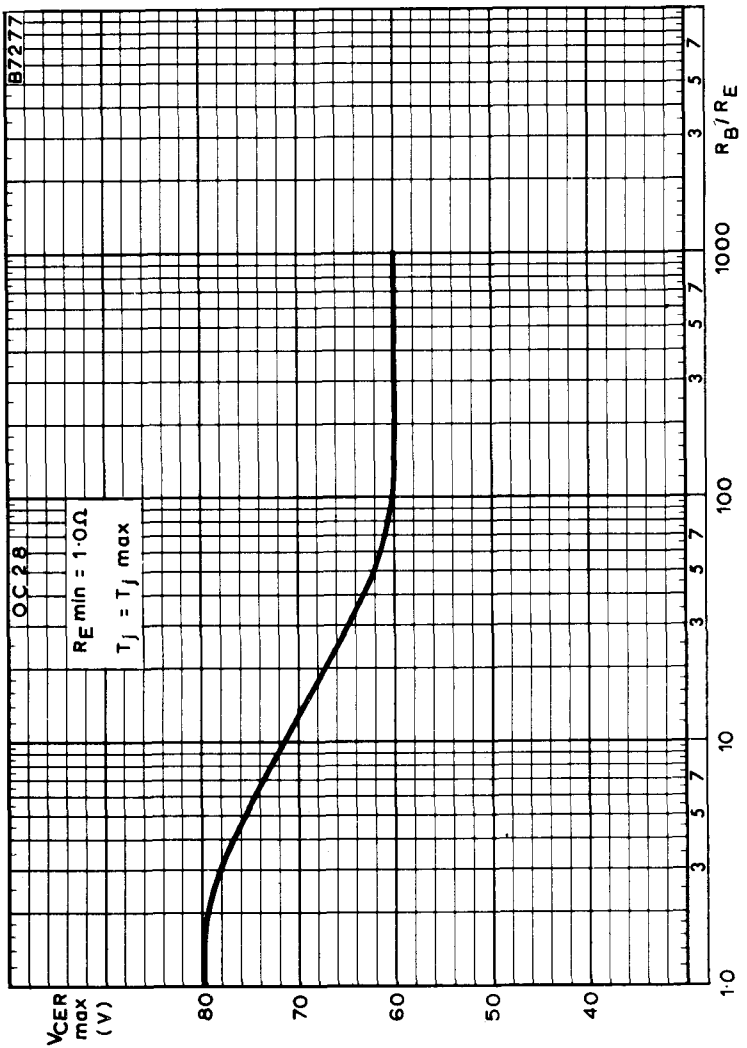
MAXIMUM TOTAL DISSIPATION PLOTTED AGAINST CASE TEMPERATURE



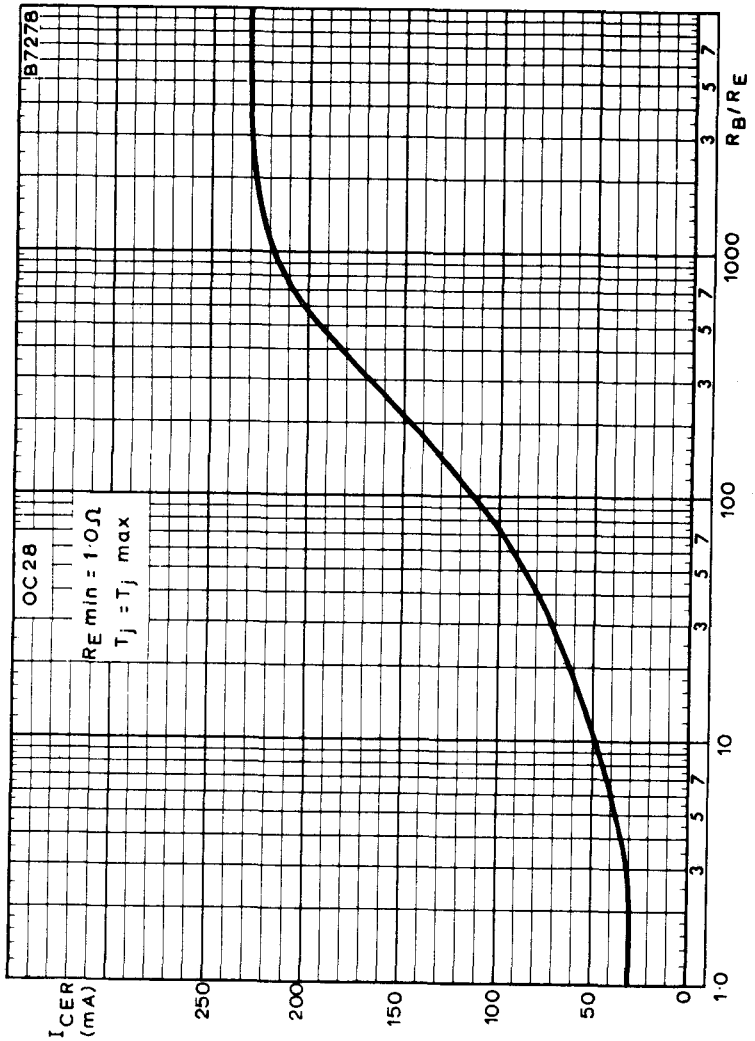
VARIATION OF I_{CBO} WITH JUNCTION TEMPERATURE. OC28, OC36



VARIATION OF I_{CBO} WITH JUNCTION TEMPERATURE. OC29, OC35



MAXIMUM PERMISSIBLE COLLECTOR-EMITTER VOLTAGE PLOTTED AGAINST RATIO OF R_B/R_E



TYPICAL VARIATION OF I_{CER} WITH RATIO OF R_B/R_E

SILICON N-P-N PLANAR TRANSISTOR

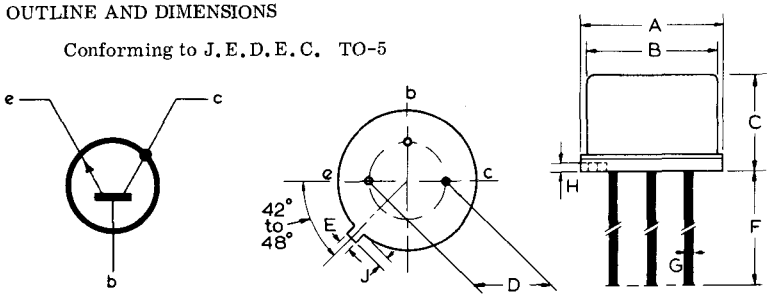
2N1613

Silicon n-p-n double diffused planar transistor designed for a wide variety of applications including d.c. amplifiers, high speed switching and high speed amplifiers.

QUICK REFERENCE DATA		
V_{CB} max. ($I_E = 0$)	+75	V
V_{CE} max.	+30	V
I_C max.	500	mA
P_{tot} max. ($T_{amb} = 25^oC$)	800	mW
h_{FE} ($I_{CM} = 150mA$, $V_{CE} = +10V$)	40 - 120	
f_T typ. ($I_C = 50mA$, $V_{CE} = +10V$, f = 20Mc/s)	60	Mc/s

OUTLINE AND DIMENSIONS

Conforming to J.E.D.E.C. TO-5



B2390

Collector connected to envelope

	Millimetres				Millimetres		
	Min.	Nom.	Max.		Min.	Nom.	Max.
A	8.64	8.9	9.4	F	38	-	-
B	7.75	8.15	8.50	G	-	0.45	-
C	6.10	6.35	6.60	*H	-	0.4	-
D	-	5.08	-	J	0.74	0.85	1.01
E	0.71	0.79	0.86	*Thickness of locating tab.			

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

†V_{CB} max.	+75	V
†V_{CER} max. ($R_{BE} \leq 10\Omega$)	+50	V
†V_{EB} max.	+7.0	V
†V_{CEO} max. ($I_B = 0$)	+30	V
I_{CM} max.	500	mA
†P_{tot} max. $T_{case} = 25^{o}C$	3.0	W
$T_{case} = 100^{o}C$	1.7	W
$T_{amb} = 25^{o}C$	0.8	W

Thermal

†T_{stg} min.	-65	^{o}C
T_{stg} max.	200*	^{o}C
†T_j (operating range)	-65 to +200	^{o}C

*See Soldering and Wiring Recommendation No. 4.

THERMAL CHARACTERISTIC

†$R_{th(j-case)}$	58.3	deg C/W

ELECTRICAL CHARACTERISTICS ($T_{amb}=25^{o}C$ unless otherwise stated)

		Min.	Max.	
†I_{CBO}	Collector cut-off current			
	$V_{CB}=60V$, $I_E=0$	-	10	nA
	$V_{CB}=60V$, $I_E=0$, $T_{amb}=150^{o}C$	-	10	μA
†I_{EBO}	Emitter cut-off current			
	$V_{EB}=+5.0V$, $I_C=0$	-	10	nA
†$V_{BR(CBO)}$	Collector-base breakdown voltage			
	$I_C=100\mu A$	+75	-	V
†$V_{BR(EBO)}$	Emitter-base breakdown voltage			
	$I_E=100\mu A$, $I_C=0$	+7.0	-	V
†$V_{CER(sat)}$	Collector-emitter voltage			
	$R_{BE}\leq 10\Omega$, $I_C=10mA$ (See note 1)	+50	-	V
†$V_{CE(sat)}$	Collector-emitter saturation voltage			
	$I_B=15mA$, $I_C=150mA$ (See note 1)	-	+1.5	V
†$V_{BE(sat)}$	Base-emitter saturation voltage			
	$I_B=15mA$, $I_C=150mA$ (see note 1)	-	+1.3	V
†h_{FE}	Large signal forward current transfer ratio			
	$I_C=150mA$, $V_{CE}=10V$ (See note 1)	40	120	
	$I_C=500mA$, $V_{CE}=10V$ (See note 1)	20	-	
	$I_C=10mA$, $V_{CE}=10V$ (See note 1)	35	-	
	$I_C=10mA$, $V_{CE}=10V$, $T_{amb}=-55^{o}C$, (See note 1)	20	-	

		Min.	Max.	
$t_d + t_r + t_f$	Switching time			
	I_C = 50mA, V_{BE}(on) = +1.0V,			
	V_{BE}(off) = +1.0V, (See Fig. 1)	-	30	ns
†h_{fe}	Small signal forward current transfer ratio			
	I_C = 1.0mA, V_{CE} = 5.0V	30	100	
	I_C = 5.0mA, V_{CE} = 10V	35	150	
†h_{ib}	Input impedance			
	I_C = 1.0mA, V_{CB} = 5.0V	24	35	Ω
	I_C = 5.0mA, V_{CB} = 10V	1.0	8.0	Ω
†h_{rb}	Voltage feedback ratio			
	I_C = 1.0mA, V_{CB} = 5.0V	-	3.0	$\times 10^{-4}$
	I_C = 5.0mA, V_{CB} = 10V	-	3.0	$\times 10^{-4}$
†h_{ob}	Output admittance			
	I_C = 1.0mA, V_{CB} = 5.0V	0.1	0.5	μmhos
	I_C = 5.0mA, V_{CB} = 10V	0.1	1.0	μmhos
†h_{fe}	High frequency current transfer ratio			
	I_C = 50mA, V_{CE} = 10V,			
	f = 20Mc/s	3.0	-	
†c_{ob}	Output capacitance			
	I_C = 0mA, V_{CB} = 10V	-	25	pF
†c_{ib}	Input capacitance			
	I_C = 0mA, V_{EB} = 0.5V	-	80	pF
†N.F.	Noise figure			
	I_C = 0.3mA, V_{CE} = 10V,			
	f = 1000c/s, R_S = 510Ω,			
	1 cycle bandwidth	-	12	dB

†J.E.D.E.C. Registered Data.

NOTE

1. Measured under pulsed conditions to prevent excessive dissipation P.W. = 300μs, duty cycle ≤ 1%.

SOLDERING AND WIRING RECOMMENDATIONS

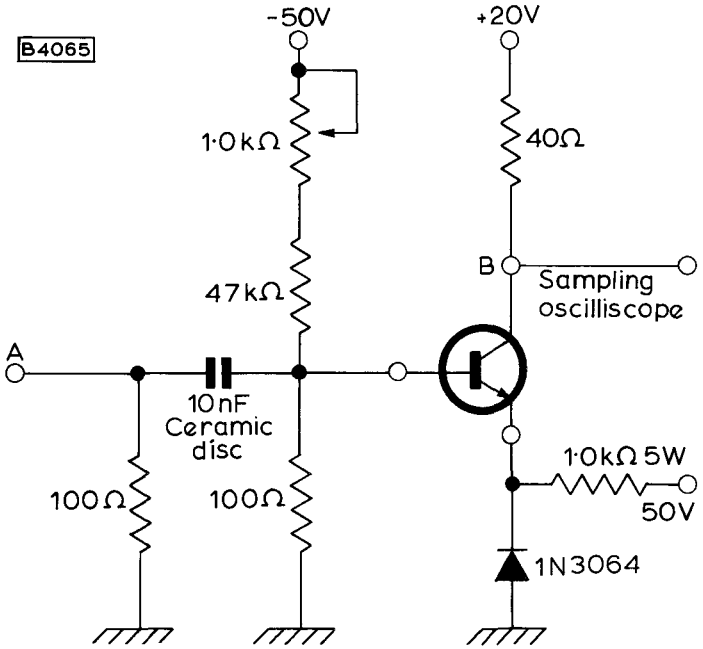
1. When using a soldering iron, transistors may be soldered directly into the circuit, but heat conducted to the junction should if possible be kept to a minimum by the use of a thermal shunt.

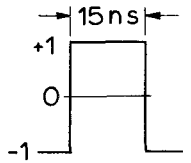
2. Transistors may be dip-soldered at a solder temperature of 245°C for a maximum soldering time of 5 seconds. The case temperature during soldering must not at any time exceed the maximum storage temperature. These recommendations apply to a transistor mounted flush on a board having punched-through holes, or spaced at least 1.5mm above a board having plated-through holes.

3. Care should be taken not to bend the leads nearer than 1.5mm from the seal.

4. After storage at temperatures greater than 125°C it may be necessary to take precautions in order to ensure adequate solderability of the leads.

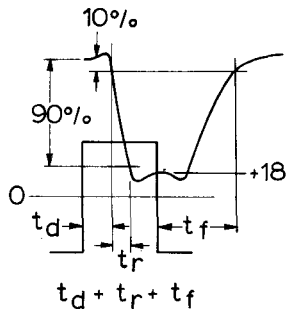
SWITCHING CHARACTERISTIC MEASUREMENT CIRCUIT

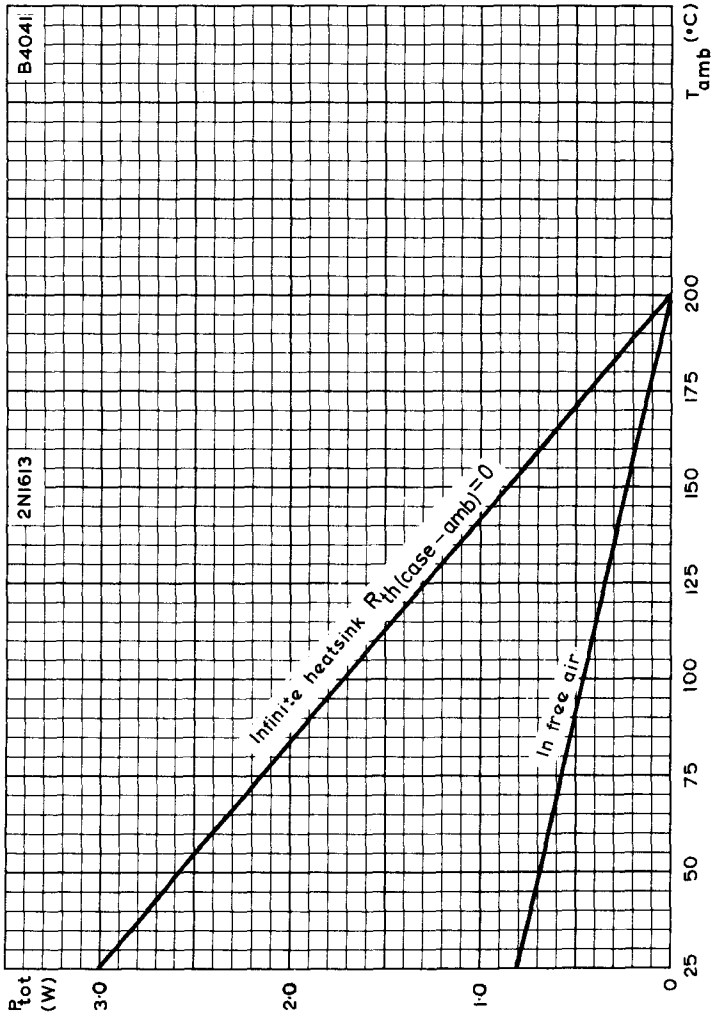




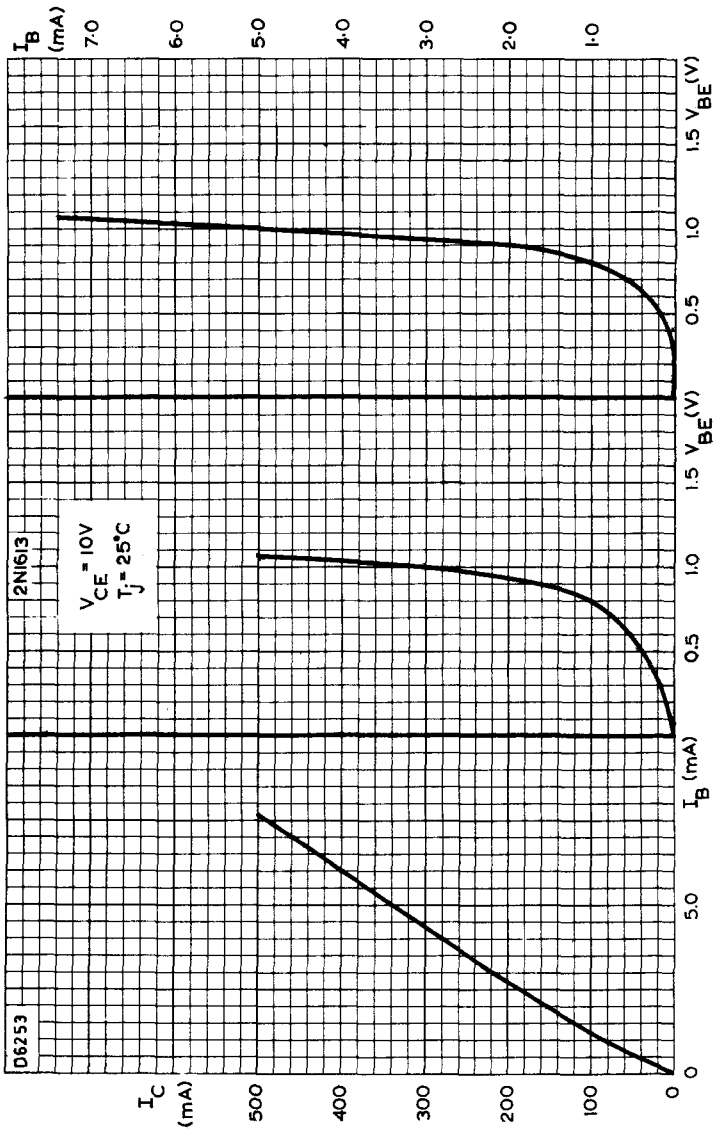
wave form at 'A'
from pulse generator
(<1ns rise time)
(<1ns fall time)

wave form at 'B'

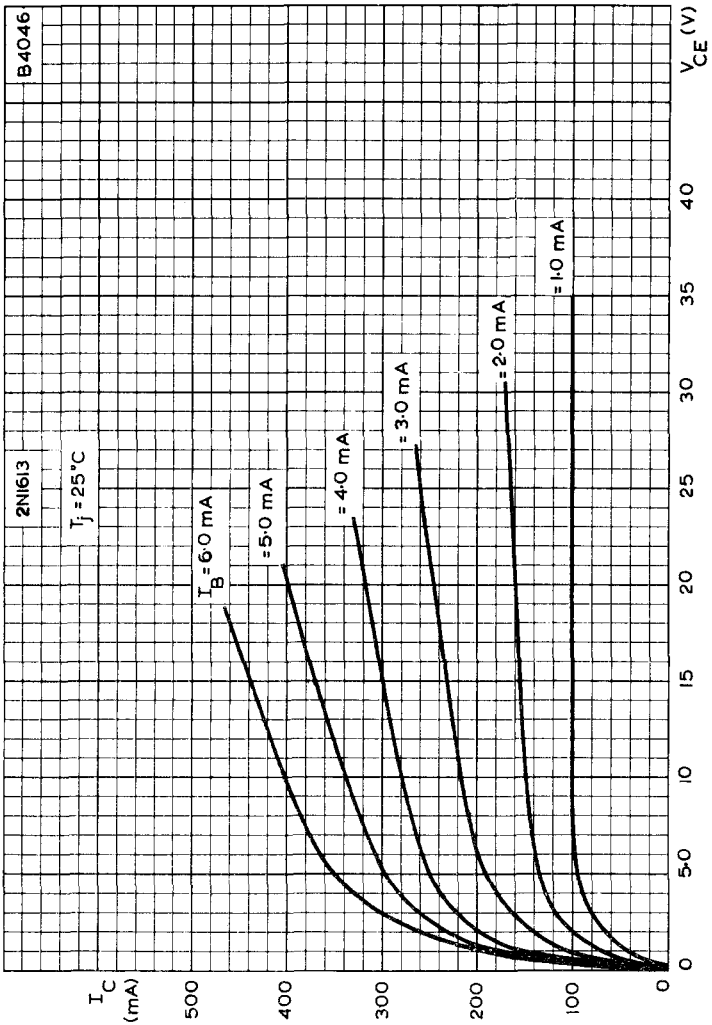




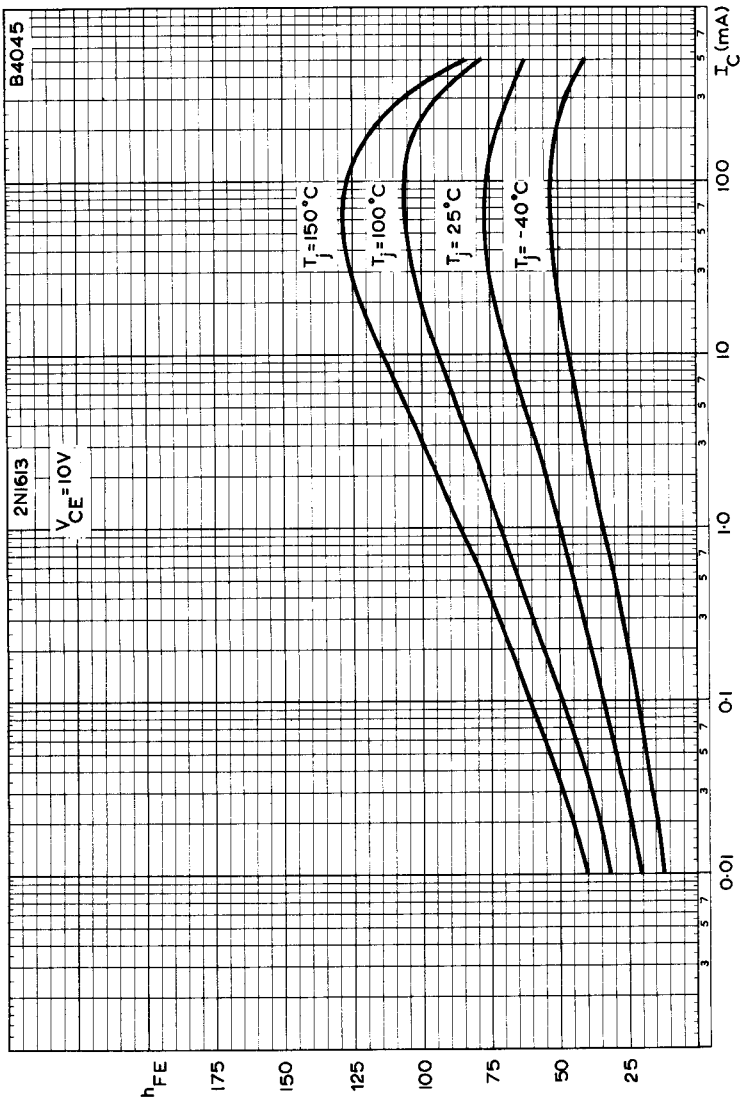
MAXIMUM TOTAL DISSIPATION PLOTTED AGAINST AMBIENT TEMPERATURE



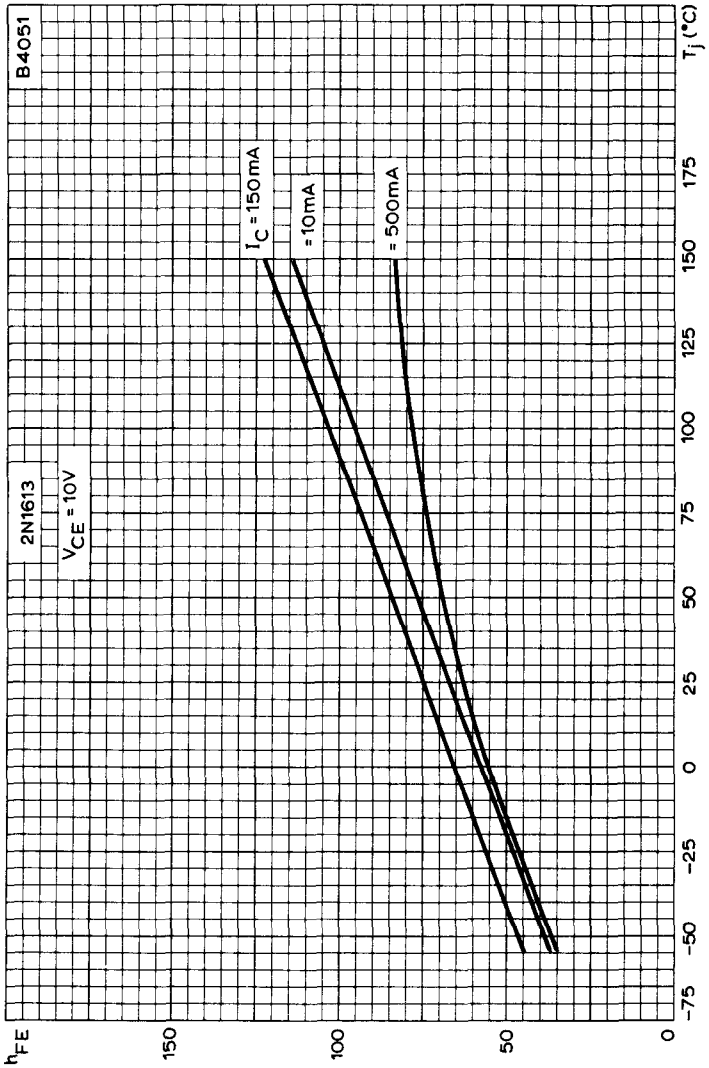
TYPICAL TRANSFER, MUTUAL AND INPUT CHARACTERISTICS



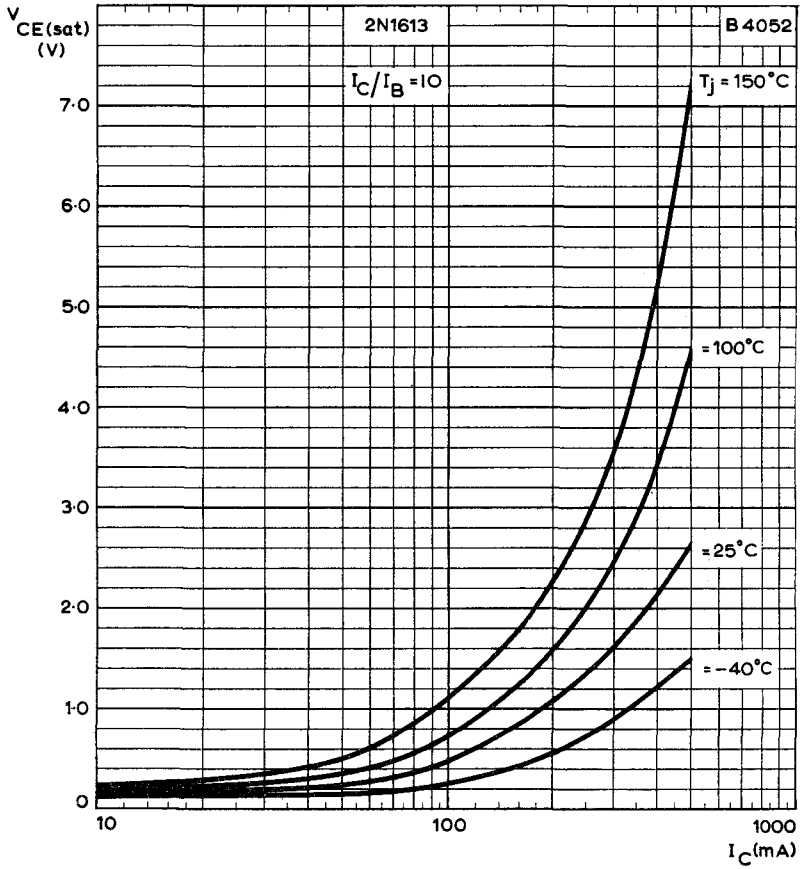
TYPICAL OUTPUT CHARACTERISTIC



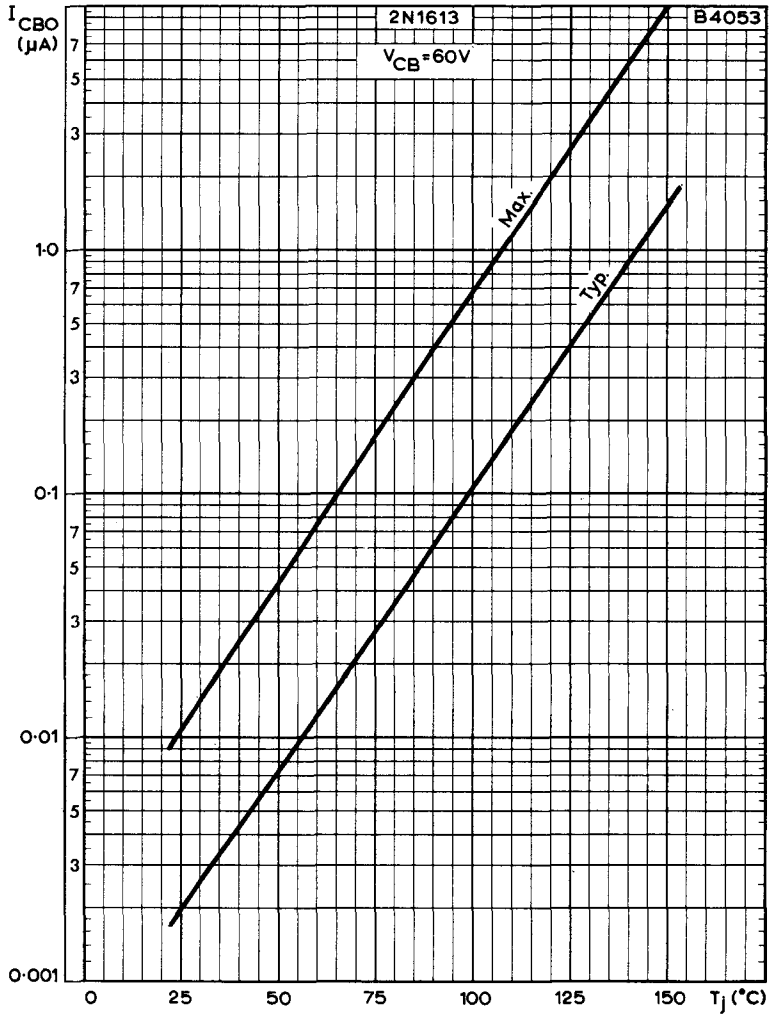
TYPICAL LARGE SIGNAL FORWARD CURRENT TRANSFER RATIO PLOTTED AGAINST COLLECTOR CURRENT WITH JUNCTION TEMPERATURE AS PARAMETER



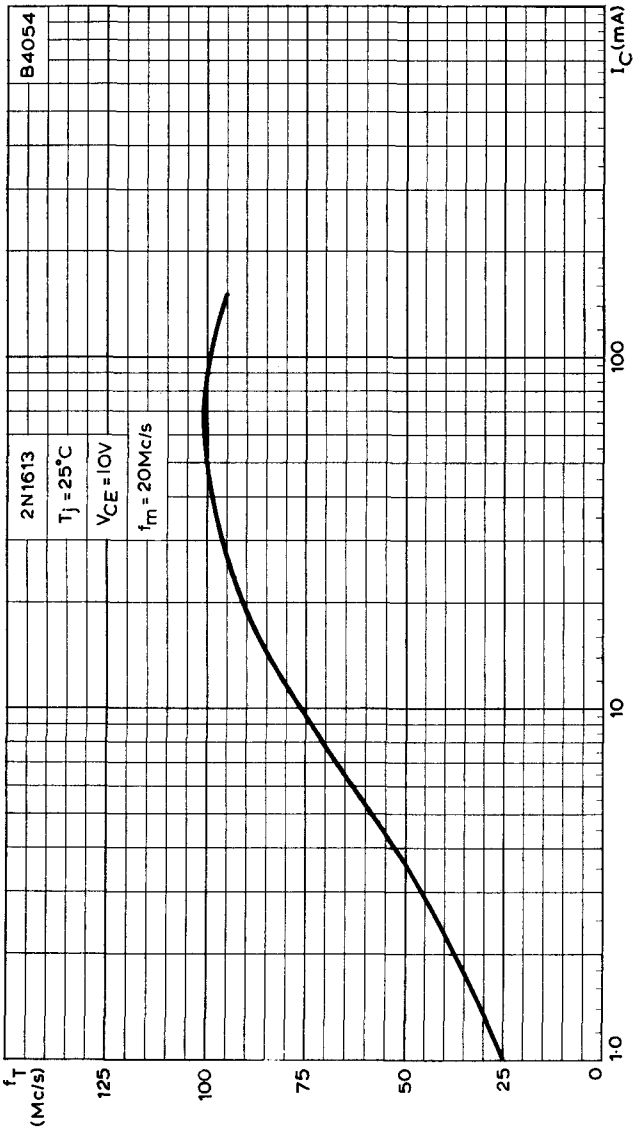
TYPICAL LARGE SIGNAL FORWARD CURRENT TRANSFER RATIO PLOTTED AGAINST JUNCTION TEMPERATURE WITH COLLECTOR CURRENT AS PARAMETER



TYPICAL COLLECTOR-EMITTER SATURATION VOLTAGE PLOTTED AGAINST COLLECTOR CURRENT WITH JUNCTION TEMPERATURE AS PARAMETER



SPREAD OF COLLECTOR CUT-OFF CURRENT PLOTTED AGAINST JUNCTION TEMPERATURE



TYPICAL TRANSITION FREQUENCY PLOTTED AGAINST COLLECTOR CURRENT

SILICON PLANAR N-P-N TRANSISTOR

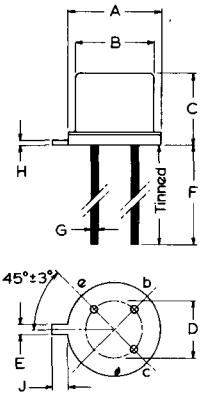
2N1711

Silicon n-p-n double diffused planar transistor designed for a wide variety of applications including d.c. and wideband amplifiers.

QUICK REFERENCE DATA		
V_{CBO} max. ($I_E = 0$)	+75	V
V_{CER} max. ($R_{BE} \leq 10\Omega$)	+50	V
I_{CM} max.	1.0	A
P_{tot} max. ($T_{amb} = 25^oC$)	800	mW
h_{FE} ($I_{CM} = 150mA$, $V_{CE} = +10V$)	100 - 300	

OUTLINE AND DIMENSIONS

Conforming to J.E.D.E.C. TO-5



	Millimetres		
	Min.	Nom.	Max.
A	8.64	8.9	9.4
B	7.75	8.15	8.5
C	6.1	6.35	6.6
D	-	5.08	-
E	0.71	0.79	0.86
F	38	-	-
G	-	0.45	-
H	-	0.4	-
J	0.74	0.85	1.01

Collector connected to envelope

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

†V_{CBO} max. (I_E=0)	+75	V
†V_{CER} max. (R_{BE} ≤10Ω)	+50	V
†V_{EBO} max. (I_C=0)	+7.0	V
V_{CEO} max. (I_B=0)	+30	V
†I_{CM} max.	1.0	A
†P_{tot} max. T_{case}=25°C	3.0	W
T_{case}=100°C	1.7	W
T_{amb}=25°C	800	mW

Temperature

†T_{stg} min.	-65	°C
T_{stg} max.	200*	°C
†T_j (operating range)	-65 to +200	°C

*See Soldering and Wiring Recommendation No.4.

THERMAL CHARACTERISTICS

†$\Theta_{j\text{-case}}$	58.3	degC/W
†$\Theta_{j\text{-amb}}$	219	degC/W

ELECTRICAL CHARACTERISTICS (T_{amb}=25°C unless otherwise stated)

		Min.	Max.	
†I_{CBO}	Collector cut-off current			
	V_{CB}=60V, I_E=0	-	10	nA
	V_{CB}=60V, I_E=0, T_{amb}=150°C	-	10	μA
†I_{EBO}	Emitter cut-off current			
	V_{EB}=5.0V, I_C=0	-	5.0	nA
†$V_{BR(CBO)}$	Collector-base breakdown voltage			
	I_C=100μA, I_E=0	+75	-	V
†$V_{BR(EBO)}$	Emitter-base breakdown voltage			
	I_E=100μA, I_C=0	+7.0	-	V
†$V_{CER(sust)}$	Collector-emitter sustaining voltage (See note 1)			
	R_{BE} ≤10Ω, I_C=100mA	+50	-	V

		Min.	Max.	
†$V_{CE(sat)}$	Collector-emitter saturation voltage (See note 1) I_B=15mA, I_C=150mA	-	+1.5	V
†$V_{BE(sat)}$	Base-emitter saturation voltage (See note 1) I_B=15mA, I_C=150mA	-	+1.3	V
†h_{FE}	Large signal forward current transfer ratio I_C=500mA, V_{CE}=10V	40	-	
	(See note 1) I_C=150mA, V_{CE}=10V	100	300	
	(See note 1) I_C=10mA, V_{CE}=10V	75	-	
	(See note 1) I_C=10mA, V_{CE}=10V, T_{amb}=-55°C	35	-	
	I_C=0.1mA, V_{CE}=10V	35	-	
	I_C=0.01mA, V_{CE}=10V	20		
Small Signal characteristics				
†h_{fe}	Small signal forward current transfer ratio I_C=1.0mA, V_{CE}=5.0V, f=1.0kc/s	50	200	
	I_C=5.0mA, V_{CE}=10V, f=1.0kc/s	70	300	
†h_{ib}	Input impedance I_C=1.0mA, V_{CB}=5.0V, f=1.0kc/s	24	34	Ω
	I_C=5.0mA, V_{CB}=10V, f=1.0kc/s	4.0	8.0	Ω
†h_{rb}	Voltage feedback ratio I_C=1.0mA, V_{CB}=5.0V, f=1.0kc/s	-	5.0	$\times 10^{-4}$
	I_C=5.0mA, V_{CB}=10V, f=1.0kc/s	-	5.0	$\times 10^{-4}$

		Min.	Max.	
†h_{ob}	Output admittance I_C=1.0mA, V_{CB}=5.0V, f=1.0kc/s	0.1	0.5	μmho
	I_C=5.0mA, V_{CB}=10V, f=1.0kc/s	0.1	1.0	μmho
†h_{fe}	Small signal forward current transfer ratio I_C=50mA, V_{CE}=10V, f=20Mc/s	3.5	-	
†c_{ob}	Output capacitance I_C=0, V_{CB}=10V	-	25	pF
†c_{ib}	Input capacitance I_C=0, V_{EB}=0.5V	-	80	pF
†NF	Noise figure I_C=0.3mA, V_{CE}=10V, f=1.0kc/s, R_S=510Ω, 1 cycle bandwidth	-	8.0	dB

†J.E.D.E.C. registered data

NOTE

1. Measured under pulsed conditions to prevent excessive dissipation pulse duration=300μs, duty cycle≤1%.

SOLDERING AND WIRING RECOMMENDATIONS

1. When using a soldering iron, transistors may be soldered directly into the circuit, but heat conducted to the junction should if possible be kept to a minimum by the use of a thermal shunt.
2. Transistors may be dip-soldered at a solder temperature of 245°C for a maximum soldering time of 5 seconds. The case temperature during dip-soldering must not at any time exceed tha maximum storage temperature. These recommendations apply to a transistor mounted flush on a board having punched-through holes, or spaced at least 1.5mm above a board having plated-through holes.
3. Care should be taken not to bend the leads nearer than 1.5mm from the seal.
4. If devices are stored above 100°C before incorporation into equipment, some deterioration of the external surface is likely to occur which may make soldering into the circuit difficult. Under these circumstances the leads should be retinned using a suitable activated flux.

SILICON N-P-N EPITAXIAL PLANAR TRANSISTOR

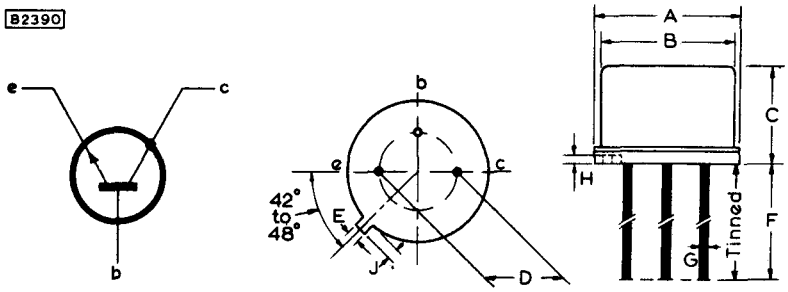
2N2297

Silicon n-p-n epitaxial planar transistor intended for large signal h.f. and v.h.f. amplifier applications.

QUICK REFERENCE DATA		
V_{CB} max. ($I_E = 0$)	+80	V
V_{CE} max.	+35	V
I_C max.	1.0	A
P_{tot} max. ($T_{amb} = 25^oC$)	800	mW
h_{FE} ($I_{CM} = 150mA$, $V_{CE} = +10V$)	40-120	
f_T min. ($I_C = 50mA$, $V_{CE} = +10V$, $f = 20Mc/s$)	60	Mc/s

OUTLINE AND DIMENSIONS

Conforming to J.E.D.E.C. TO-5



Collector connected to envelope

	Millimetres				Millimetres		
	Min.	Nom.	Max.		Min.	Nom.	Max.
A	8.64	8.9	9.4	F	38	-	-
B	7.75	8.15	8.50	G	-	0.45	-
C	6.10	6.35	6.60	*H	-	0.4	-
D	-	5.08	-	J	0.74	0.85	1.01
E	0.71	0.79	0.86	*Thickness of locating tab.			

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

†V_{CB} max. ($I_E = 0$)	+80	V
†V_{CE} max. ($I_B = 0$)	+35	V
†V_{EB} max. ($I_C = 0$)	+7.0	V
†I_C max.	1.0	A
†P_{tot} max. $T_{case} = 25^oC$	5.0	W
$T_{case} = 100^oC$	2.8	W
$T_{amb} = 25^oC$	0.8	W

Thermal

†T_{stg} min.	-65	^oC
T_{stg} max.	200*	^oC
†T_j max. (operating)	200	^oC

*See Soldering and Wiring Recommendation No. 4.

THERMAL CHARACTERISTICS

†Derating factor at $T_{case} = 25^oC$	28.6	mW/deg C
$T_{amb} = 25^oC$	4.6	mW/deg C

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise stated)

		Min.	Max.	
†I_{CBO}	Collector cut-off current			
	V_{CB} = +60V, I_E = 0	-	10	nA
	V_{CB} = +60V, I_E = 0, T_{amb} = 150	-	10	μA
†I_{EBO}	Emitter cut-off current			
	V_{EB} = 5.0V, I_C = 0	-	10	nA
†$V_{CEO(sust.)}$	Collector-emitter sustaining voltage			
	I_C = 30mA (See note 1)	35	-	V
†$V_{(BR)CBO}$	Collector-base breakdown voltage			
	I_C = 100μA, I_E = 0	80	-	V
†$V_{(BR)EBO}$	Emitter-base breakdown voltage			
	I_E = 100μA, I_C = 0	7.0	-	V
†$V_{CE(sat)}$	Collector-emitter saturation voltage			
	I_C = 150mA, I_B = 15mA	-	0.2	V
	I_C = 1.0A, I_B = 100mA (See notes 1 and 2)	-	1.0	V
†$V_{BE(sat)}$	Base-emitter saturation voltage			
	I_C = 1.0A, I_B = 100mA (See notes 1 and 2)	-	1.6	V
†h_{FE}	Large signal forward current transfer ratio			
	I_C = 150mA, V_{CE} = 10V (See note 1)	40	120	
	I_C = 10mA, V_{CE} = 10V (See note 1)	30	-	
	I_C = 1.0A, V_{CE} = 10V (See note 1)	15	-	

		Min.	Max.	
†f_T	Transition frequency I_C=50mA, V_{CE}=+10V, f=20Mc/s	60	-	Mc/s
†c_{ob}	Output capacitance V_{CB}=10V, I_E=0	-	12	pF
†c_{ib}	Open-circuit input capacitance I_C=0, V_{EB}=0.5V	-	80	pF
†r_b, c_c	Collector-base time constant I_C=10mA, V_{CB}=10V, f=4.0Mc/s	-	800	ps

†J.E.D.E.C. Registered Data.

NOTES

1. Measured under pulsed conditions to prevent excessive dissipation. P.W. ≐300μs, duty cycle ≤1%.

2. Measured at a point on the lead ≤12.7mm (0.5in) from the seating plane of the transistor

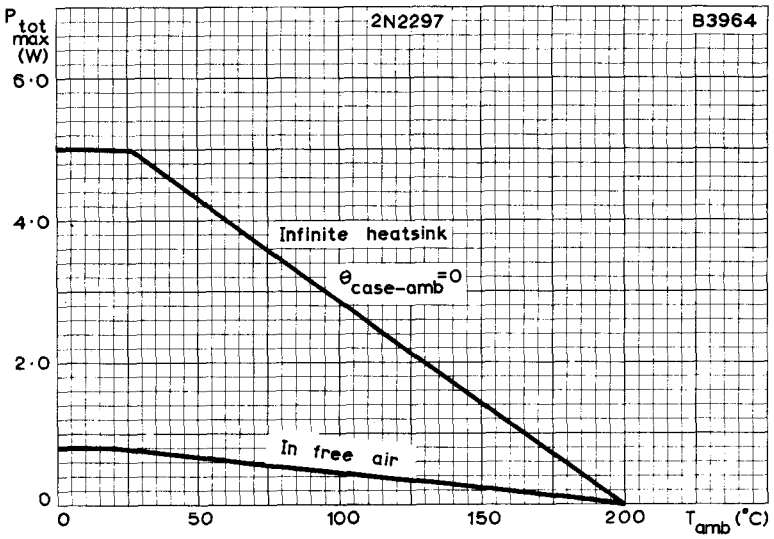
SOLDERING AND WIRING RECOMMENDATIONS

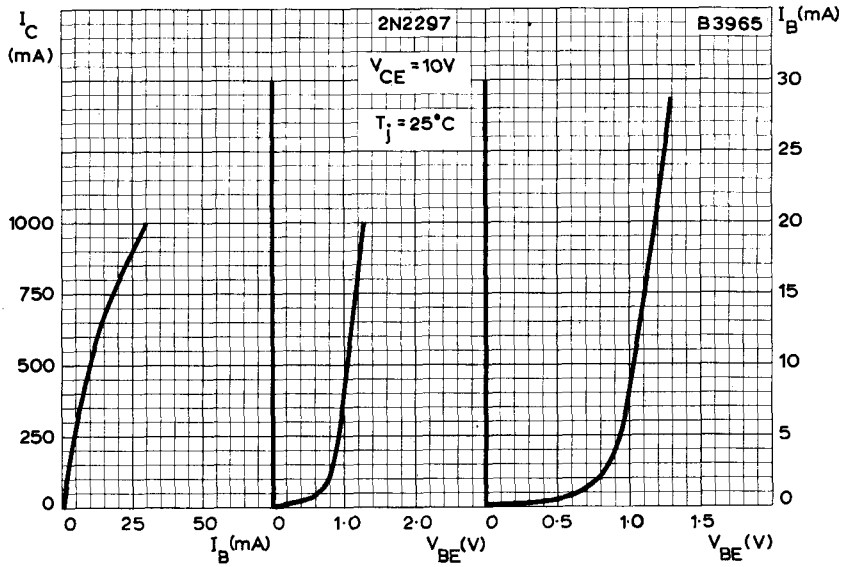
1. When using a soldering iron, transistors may be soldered directly into the circuit, but heat conducted to the junction should if possible be kept to a minimum by the use of a thermal shunt.

2. Transistors may be dip-soldered at a solder temperature of 245°C for a maximum soldering time of 5 seconds. The case temperature during soldering must not at any time exceed the maximum storage temperature . These recommendations apply to a transistor mounted flush on a board having punched-through holes, or spaced at least 1.5mm above a board having plated-through holes.

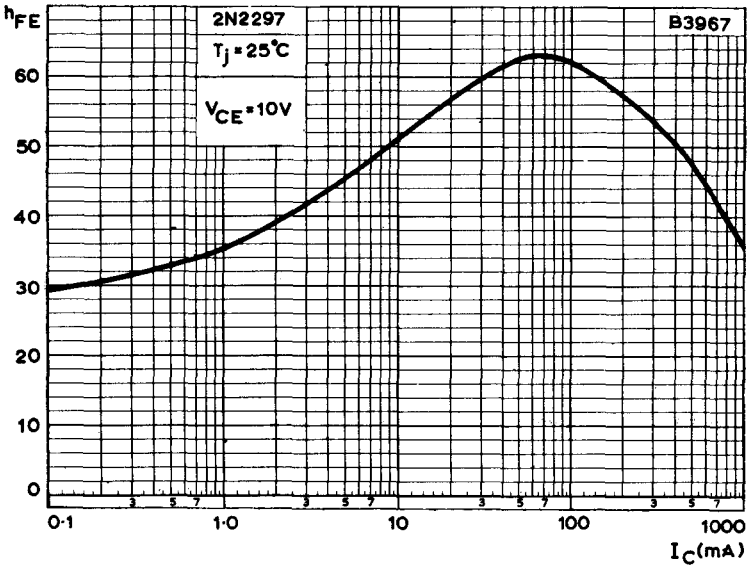
3. Care should be taken not to bend the leads nearer than 1.5mm from the seal.

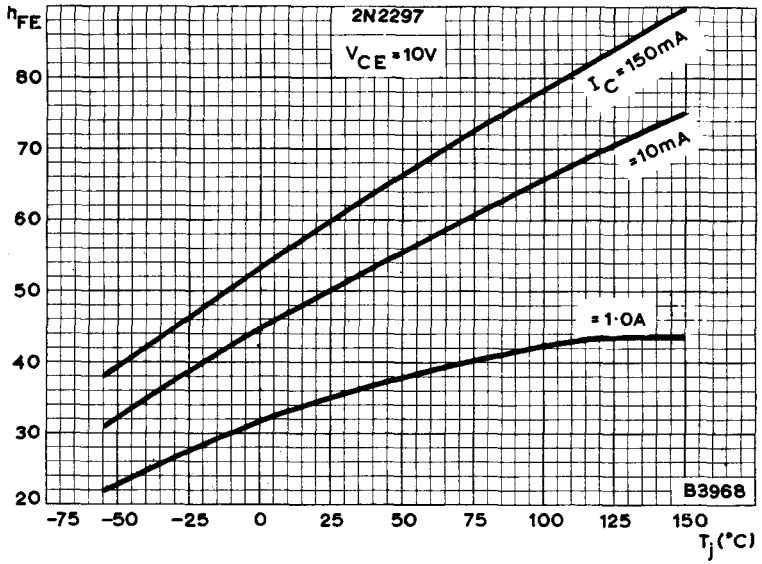
4. After storage at temperatures greater than 125°C it may be necessary to take precautions in order to ensure adequate solderability of the leads.



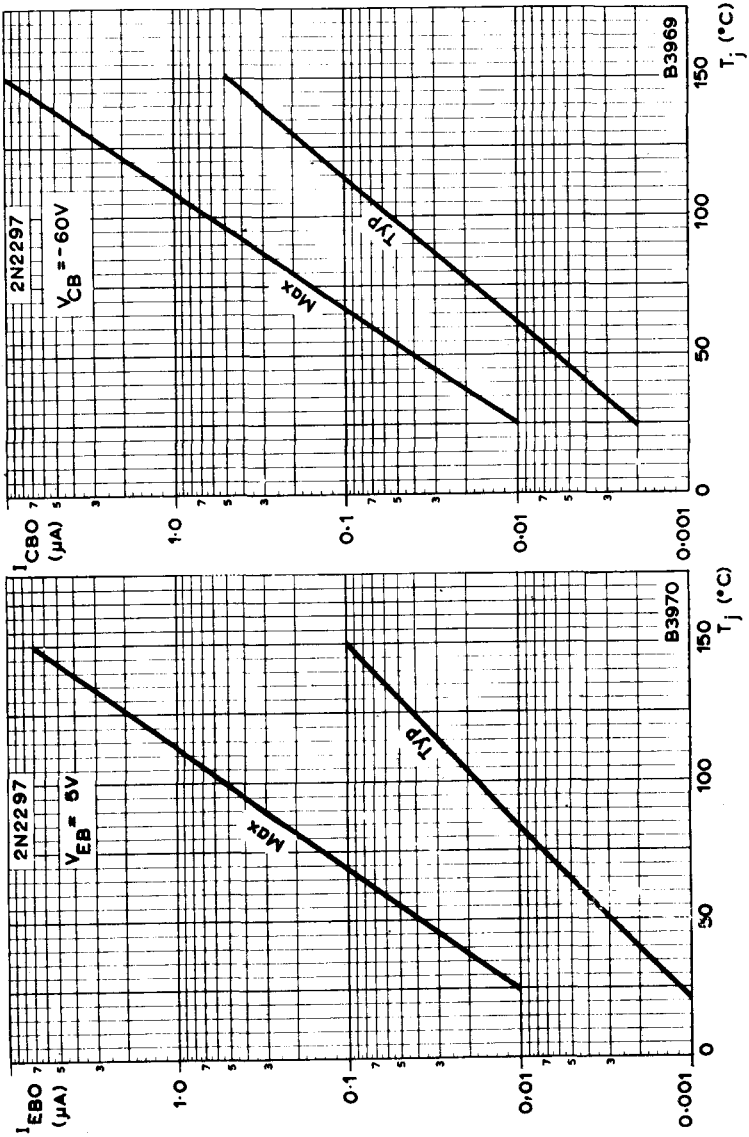


MAXIMUM TOTAL DISSIPATION PLOTTED AGAINST AMBIENT TEMPERATURE.
TYPICAL TRANSFER, MUTUAL AND INPUT CHARACTERISTICS



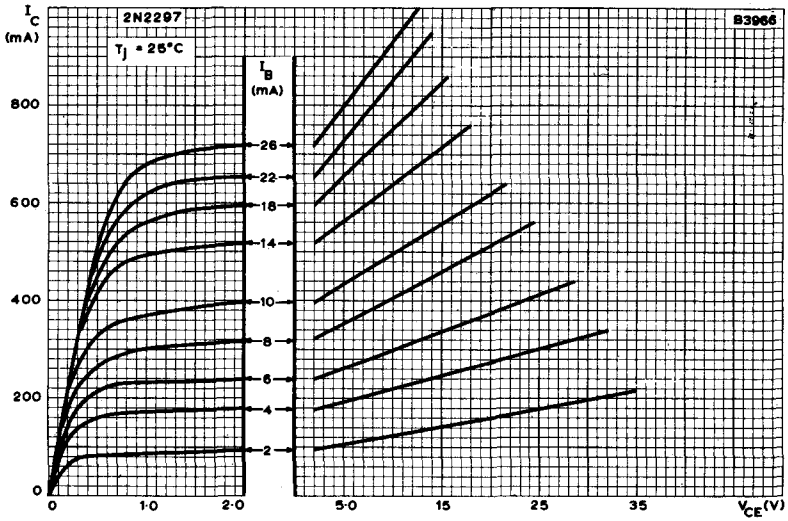


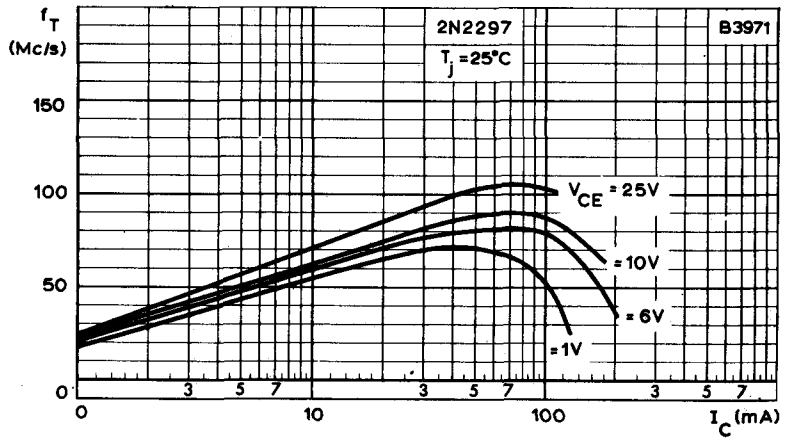
TYPICAL LARGE SIGNAL FORWARD CURRENT TRANSFER RATIO PLOTTED AGAINST COLLECTOR CURRENT
TYPICAL LARGE SIGNAL FORWARD CURRENT TRANSFER RATIO PLOTTED AGAINST JUNCTION TEMPERATURE



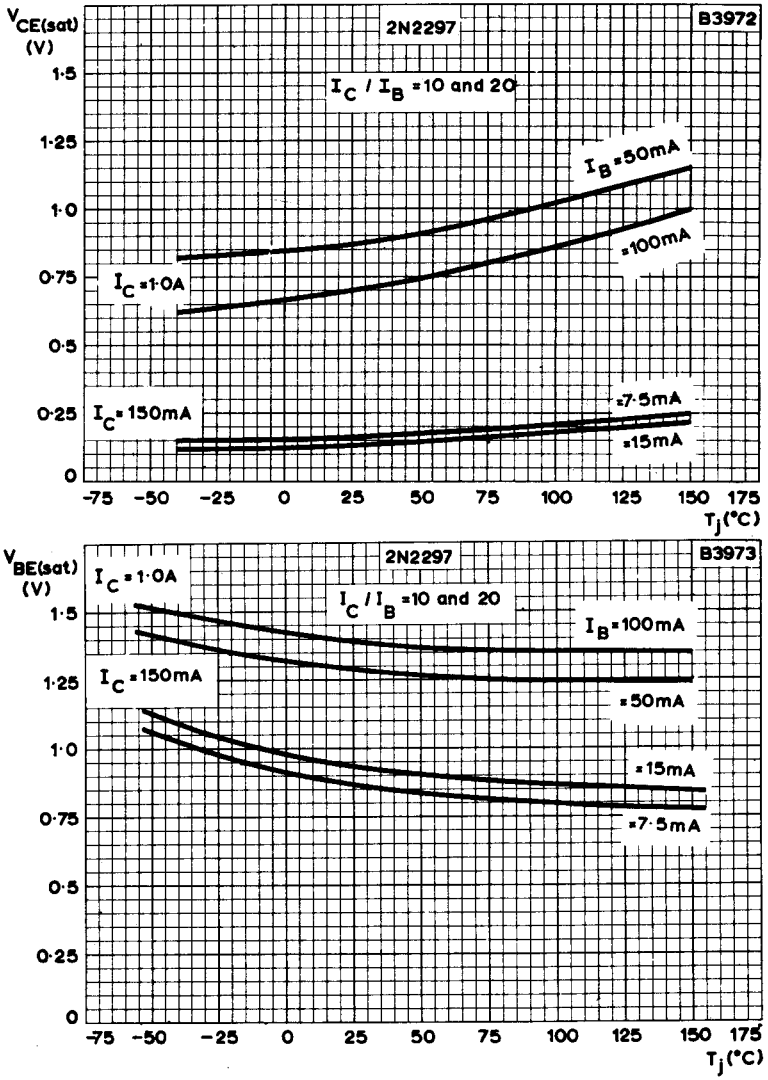
COLLECTOR CUT-OFF CURRENT PLOTTED AGAINST JUNCTION TEMPERATURE

EMITTER CUT-OFF CURRENT PLOTTED AGAINST JUNCTION TEMPERATURE



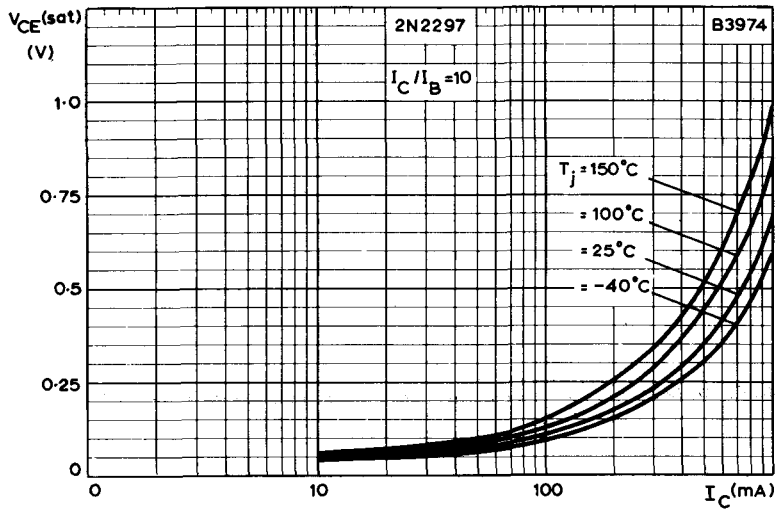


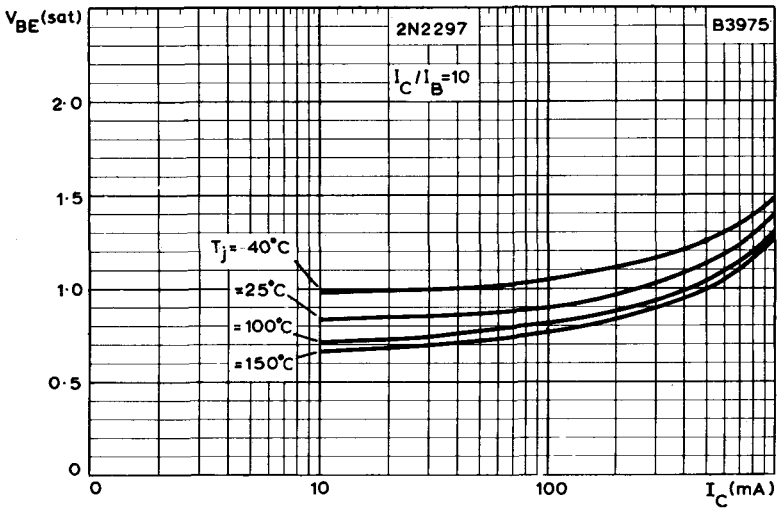
TYPICAL OUTPUT CHARACTERISTICS. $T_j = 25^oC$
TYPICAL TRANSITION FREQUENCY PLOTTED AGAINST COLLECTOR CURRENT.
COLLECTOR-EMITTER VOLTAGE AS PARAMETER



TYPICAL COLLECTOR-EMITTER SATURATION VOLTAGE PLOTTED AGAINST JUNCTION TEMPERATURE. COLLECTOR AND BASE CURRENTS AS PARAMETERS

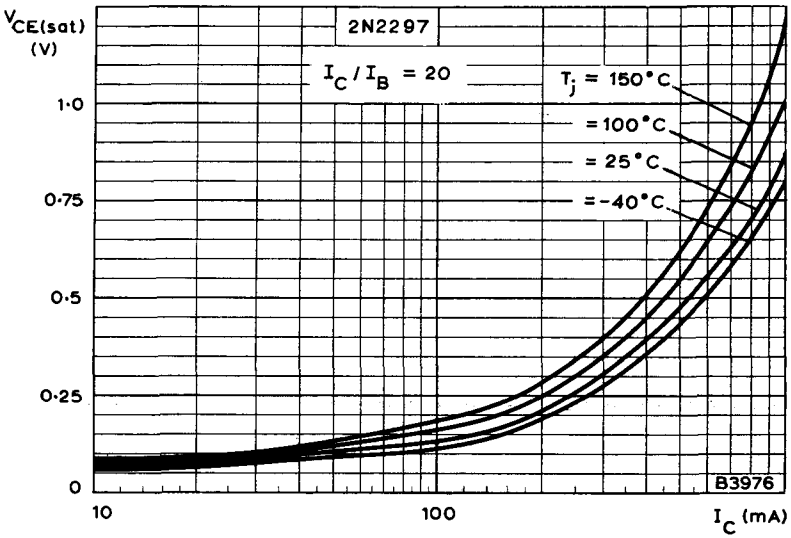
TYPICAL BASE-EMITTER SATURATION VOLTAGE PLOTTED AGAINST JUNCTION TEMPERATURE. COLLECTOR AND BASE CURRENTS AS PARAMETERS

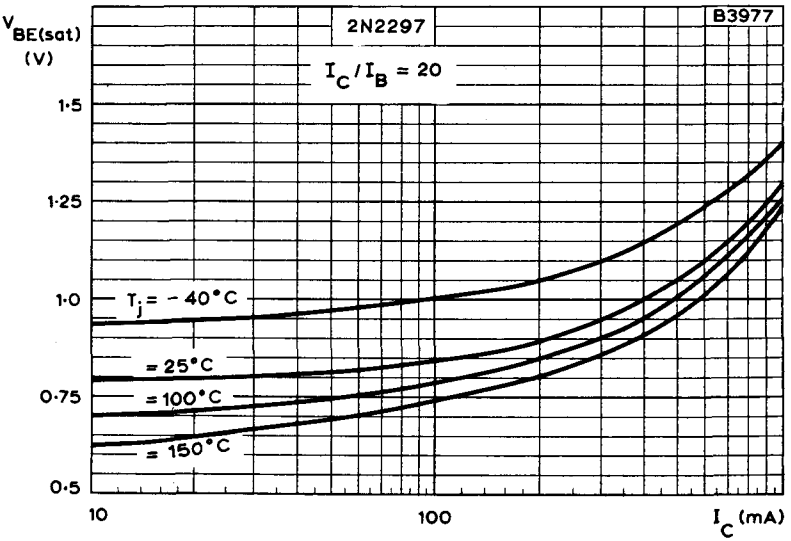




TYPICAL COLLECTOR-EMITTER SATURATION VOLTAGE PLOTTED AGAINST COLLECTOR CURRENT, WITH JUNCTION TEMPERATURE AS PARAMETER. $I_C/I_B=10$.

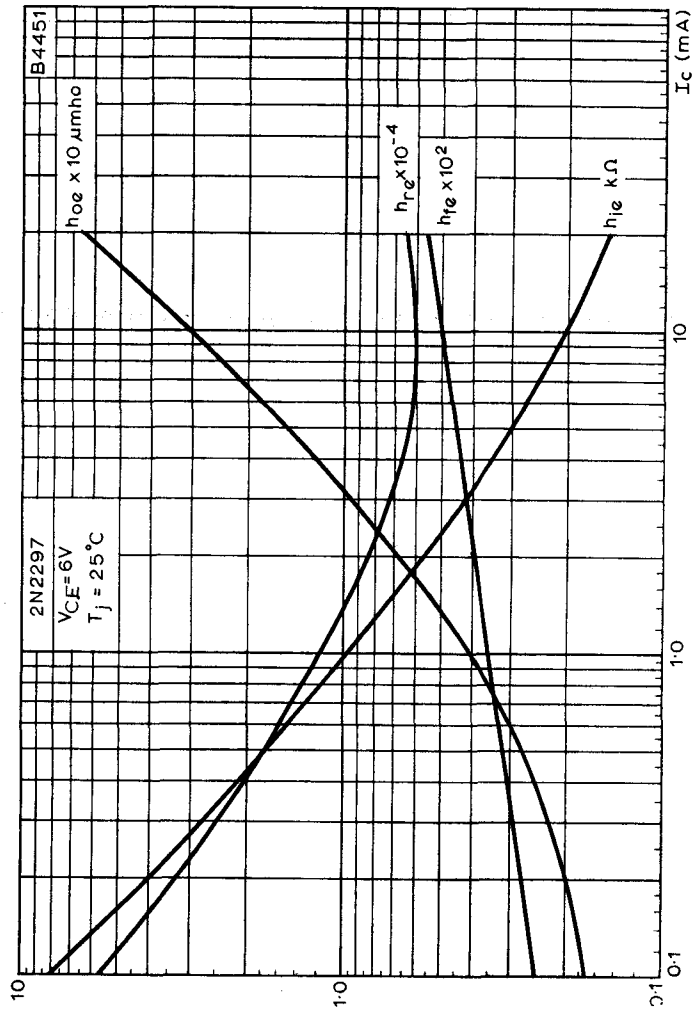
TYPICAL BASE-EMITTER SATURATION VOLTAGE PLOTTED AGAINST COLLECTOR CURRENT, WITH JUNCTION TEMPERATURE AS PARAMETER. $I_C/I_B=10$.



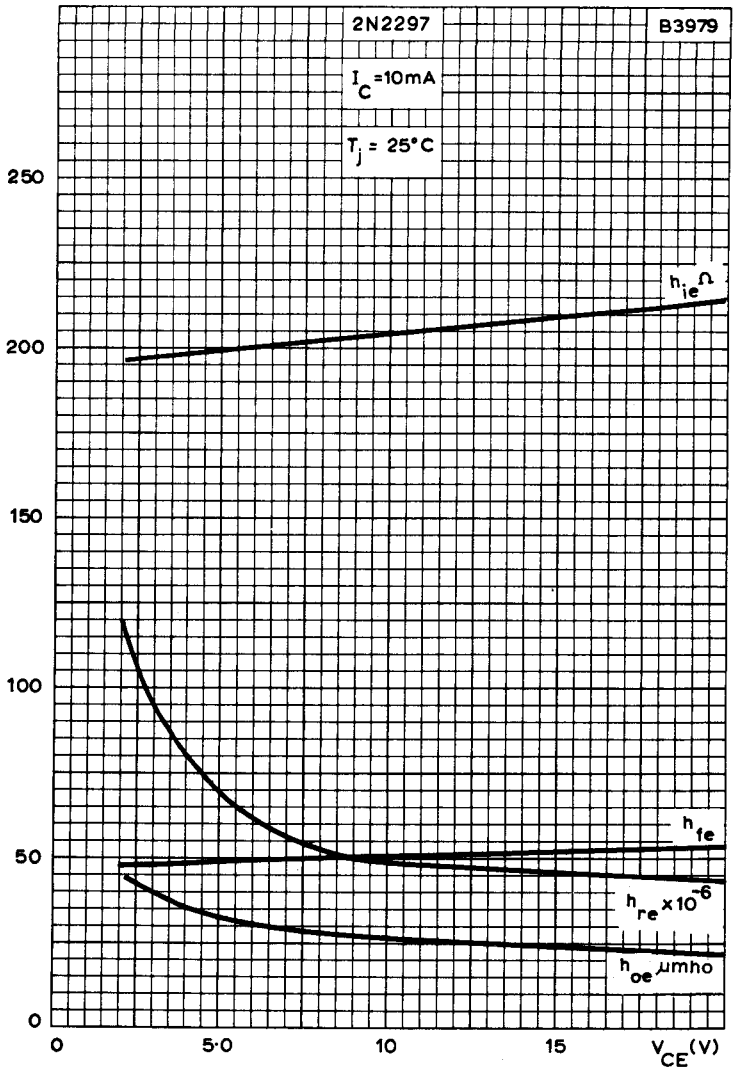


TYPICAL COLLECTOR-EMITTER SATURATION VOLTAGE PLOTTED AGAINST COLLECTOR CURRENT, WITH JUNCTION TEMPERATURE AS PARAMETER. $I_C/I_B = 20$.

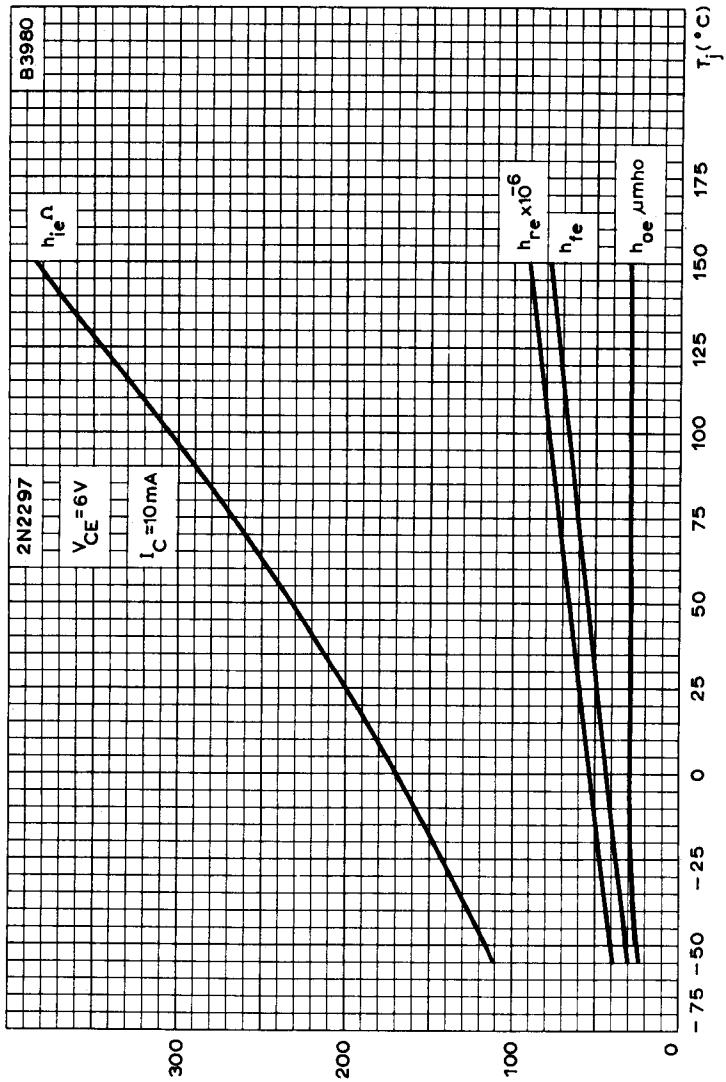
TYPICAL BASE-EMITTER SATURATION VOLTAGE PLOTTED AGAINST COLLECTOR CURRENT, WITH JUNCTION TEMPERATURE AS PARAMETER. $I_C/I_B = 20$.



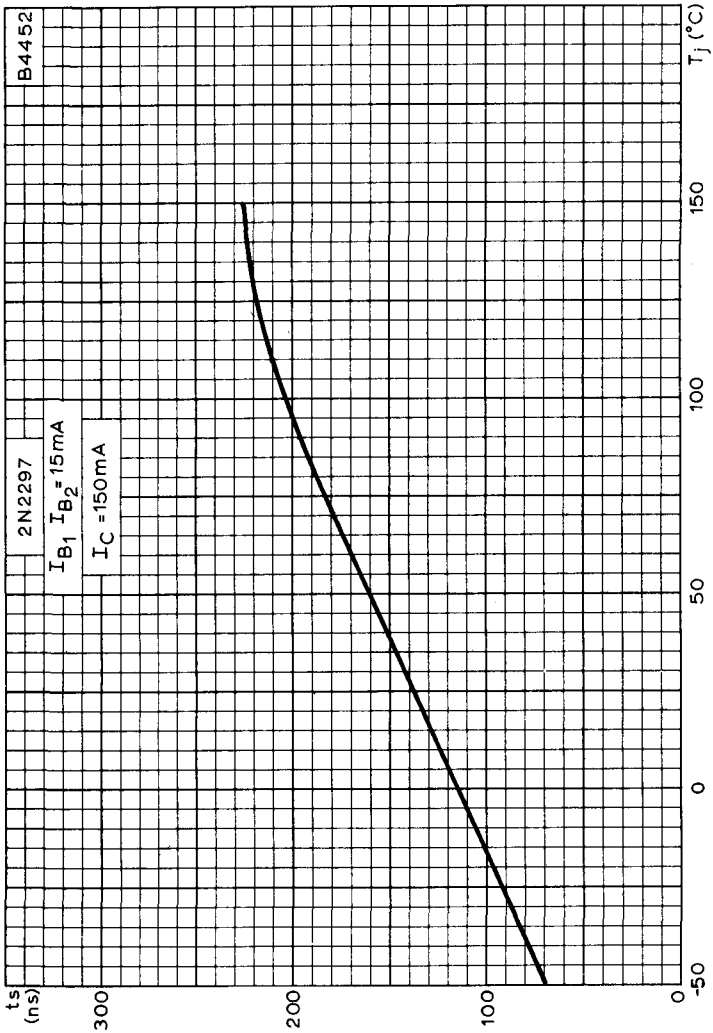
TYPICAL VARIATION OF h PARAMETERS WITH COLLECTOR CURRENT



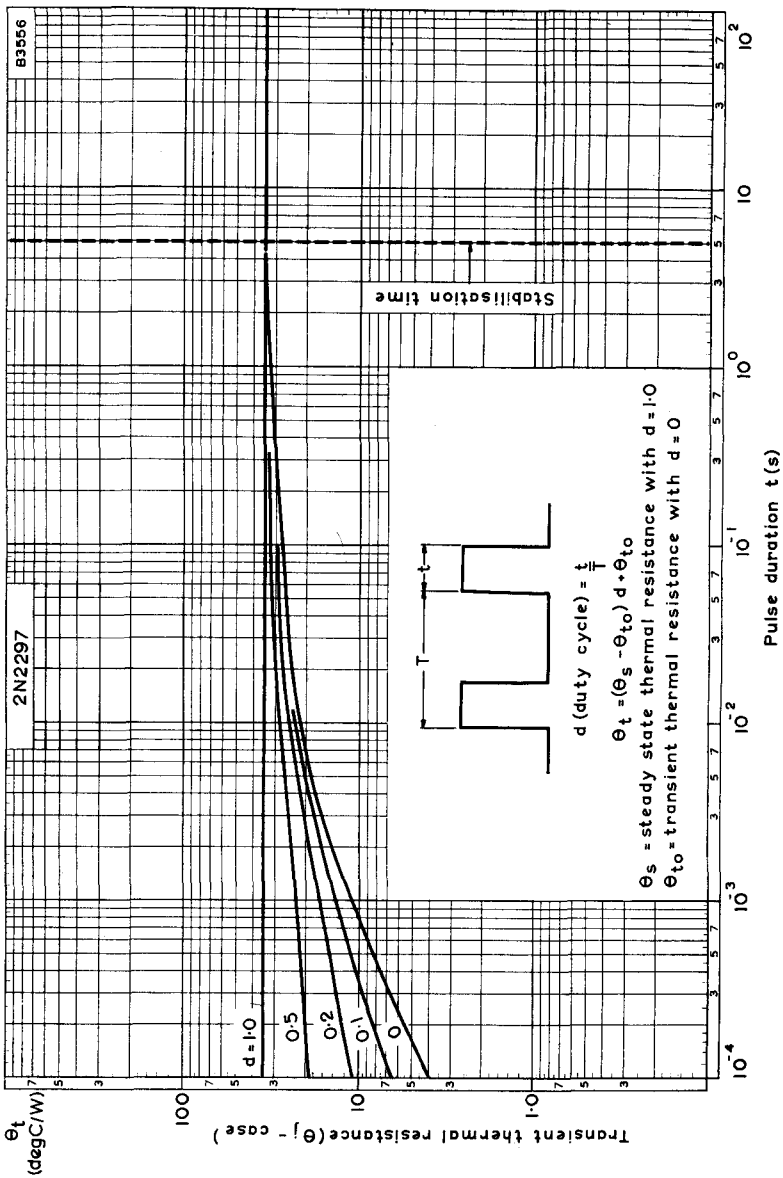
TYPICAL VARIATION OF h PARAMETERS WITH COLLECTOR-EMITTER VOLTAGE



TYPICAL VARIATION OF h PARAMETERS WITH JUNCTION TEMPERATURE



TYPICAL VARIATION OF STORAGE TIME WITH JUNCTION TEMPERATURE



TRANSIENT THERMAL RESISTANCE FOR VARIOUS DUTY FACTORS PLOTTED AGAINST PULSE DURATION

SILICON PLANAR EPITAXIAL N-P-N TRANSISTOR

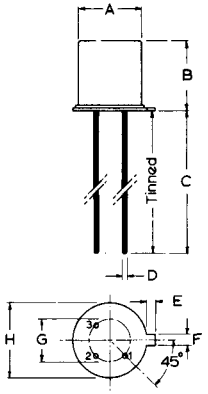
2N2369A

Silicon planar epitaxial n-p-n transistor primarily intended for high-speed saturated switching and high frequency amplifier applications. TO-18 construction with collector connected to envelope.

QUICK REFERENCE DATA		
V_{CBO} max.	40	V
V_{CEO} max.	15	V
I_{CM} max.	500	mA
P_{tot} max. ($T_{amb}=25^{o}C$)	360	mW
T_j max.	200	^{o}C
h_{FE} min. ($I_C=10mA$, $V_{CE}=1.0V$)	40-120	
f_T min. ($I_C=10mA$, $f=100MHz$)	500	MHz
t_s max. ($I_C=I_B=-I_{BM}=10mA$)	13	ns

OUTLINE AND DIMENSIONS

Conforming to J.E.D.E.C. TO-18



	Millimetres		
	Min.	Nom.	Max.
A	-	-	4.8
B	-	-	5.33
C	12.7	-	-
D	-	0.43	-
E	-	1.0	-
F	-	1.05	-
G	-	2.54	-
H	5.3	5.55	5.8

Connections 1. Emitter

2. Base

3. Collector connected to envelope

†RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{CBO} max.	40	V
V_{CES} max.	40	V
V_{CEO} max. (I_C=0.01 to 10mA)	15	V
V_{EBO} max.	4.5	V
I_{CM} max. (10μs pulse)	500	mA
I_C max.	200	mA
P_{tot} max. T_{amb}=25°C	360	mW
T_{case}=25°C	1200	mW
T_{case}=100°C	680	mW

Temperature

T_{stg} min.	-65	°C
T_{stg} max.	200	°C
T_j max.	200	°C

†THERMAL CHARACTERISTICS

Derating factors T_{amb} ≥25°C	2.06	mW/degC
T_{case} ≥25°C	6.85	mW/degC

†ELECTRICAL CHARACTERISTICS (T_{amb}=25°C unless otherwise stated)

		Min.	Max.	
I_{CBO}	Collector cut-off current V_{CB}=20V, I_E=0, T_{amb}=150°C	-	30	μA
I_{CES}	Collector-emitter cut-off current V_{CE}=20V, V_{BE}=0	-	0.4	μA
$-I_{BEX}$	Base current V_{CE}=20V, V_{BE}=0	-	0.4	μA
$V_{(BR)CBO}$	Collector-base breakdown voltage I_C=10μA, I_E=0	40	-	V
$V_{(BR)CES}$	Collector-emitter breakdown voltage I_C=10μA, V_{BE}=0	40	-	V

† J.E.D.E.C. registered data.

		Min.	Max.	
$V_{(BR)EBO}$	Emitter-base breakdown voltage $I_E = 10\mu A$, $I_C = 0$	4.5	-	V
$V_{CEO(sust)}$	*Collector-emitter sustaining voltage $I_C = 10mA$, $I_B = 0$	15	-	V
h_{FE}	*Large signal forward current transfer ratio $I_C = 10mA$, $V_{CE} = 1.0V$	40	120	
	$I_C = 10mA$, $V_{CE} = 0.35V$, $T_{amb} = -55^oC$	20	-	
	$I_C = 30mA$, $V_{CE} = 0.4V$	30	-	
	$I_C = 100mA$, $V_{CE} = 1.0V$	20	-	
$V_{CE(sat)}$	Collector-emitter saturation voltage $I_C = 10mA$, $I_B = 1.0mA$	-	0.20	V
	$I_C = 10mA$, $I_B = 1.0mA$, $T_{amb} = 125^oC$	-	0.30	V
	$I_C = 30mA$, $I_B = 3.0mA$	-	0.25	V
	$I_C = 100mA$, $I_B = 10mA$	-	0.50	V
$V_{BE(sat)}$	Base-emitter saturation voltage $I_C = 10mA$, $I_B = 1.0mA$	0.70	0.85	V
	$I_C = 10mA$, $I_B = 1.0mA$, $T_{amb} = 125^oC$	0.59	-	V
	$I_C = 10mA$, $I_B = 1.0mA$ $T_{amb} = -55^oC$	-	1.02	V
	$I_C = 30mA$, $I_B = 3.0mA$	-	1.15	V
	$I_C = 100mA$, $I_B = 10mA$	-	1.60	V
f_T	Transition frequency $V_{CE} = 10V$, $I_C = 10mA$, $f = 100MHz$	500	-	MHz

*Measured under pulsed conditions to avoid excessive dissipation, pulse width = 300μs duty cycle ≤2%.

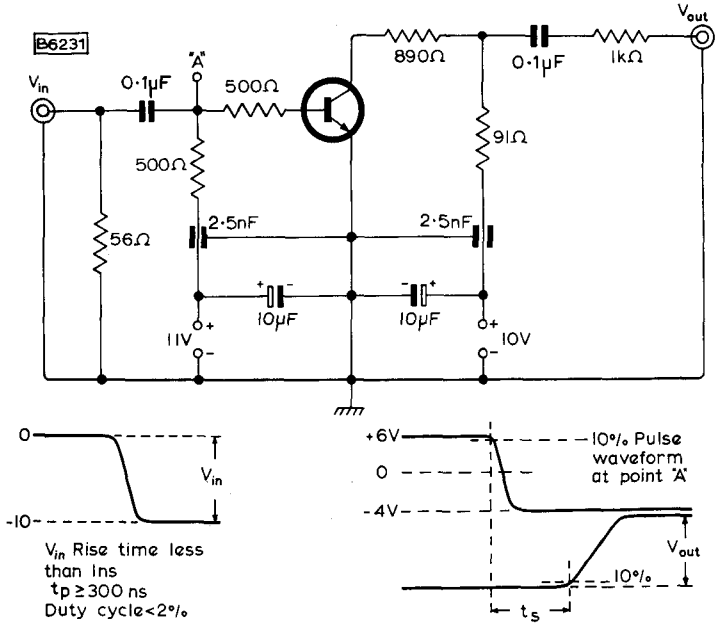
		Min.	Max.	
c_{tc}	Collector capacitance V_{CB}=5.0V, I_E=I_e=0, f=140kHz	-	4.0	pF
t_s	Storage time (see fig.1.) I_C=I_B=-I_{BM}=10mA	-	13	ns
t_{on}	Turn-on time (see fig.2.) I_C=10mA, I_B=3.0mA	-	12	ns
t_{off}	Turn-off time (see fig.2.) I_C=10mA, I_B=3.0mA, -I_{BM}=1.5mA	-	18	ns

SOLDERING RECOMMENDATION

†Max. T_{lead} 1/16" from case for 60 seconds is 300°C.

†J.E.D.E.C. registered data

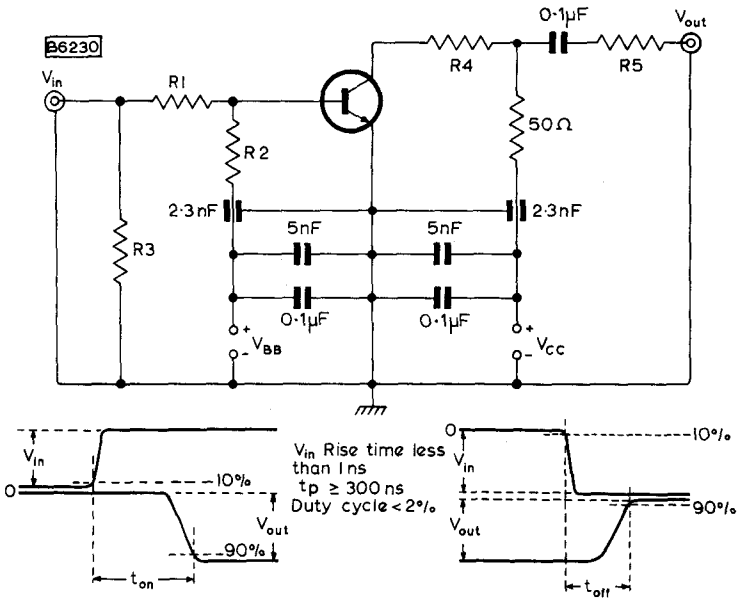
STORAGE TIME TEST CIRCUIT



Input and output waveforms

Fig. 1

t_{on} AND t_{off} TEST CIRCUIT



Input and output waveforms

Fig. 2

Circuit conditions:

V_{CC} (V)	$R_1 = R_2$ (kΩ)	R_3 (Ω)	R_4 (Ω)	R_5 (Ω)	t_{on} V_{BB} (V)	t_{on} V_{in} (V)	t_{off} V_{BB} (V)	t_{off} V_{in} (V)
3.0	3.3	50	220	0	-3.0	15	12	-15

P-N-P SILICON PLANAR EPITAXIAL TRANSISTORS

2N2904
2N2904A

P-N-P silicon planar epitaxial medium power transistors designed primarily for high-speed saturated switching and driver applications for industrial service.

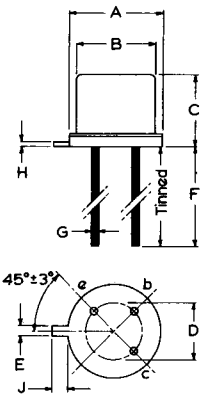
QUICK REFERENCE DATA

	2N2904	2N2904A	
$-V_{CBO}$ max.	60		V
$-V_{CEO}$ max. ($-I_C$ < 100mA)	40	60	V
$-I_C$ max.	600		mA
P_{tot} max. (T_{amb} = 25°C)	600		mW
T_j max.	200		°C
h_{FE} ($-I_C$ = 150mA, $-V_{CE}$ = 10V)	40-120		
f_T min. ($-I_C$ = 50mA, f = 100MHz)	200		MHz
t_s max. ($-I_{CS}$ = 150mA, $-I_B = +I_{BM}$ = 15mA)	80		ns

Unless otherwise stated data is applicable to both types

OUTLINE AND DIMENSIONS

Conforming to B.S. 3934 SO-3/SB3-3A
J.E.D.E.C. TO-5



	Millimetres		
	Min.	Nom.	Max.
A	8.64	8.90	9.40
B	7.75	8.15	8.50
C	6.10	6.35	6.60
D	-	5.08	-
E	0.71	0.79	0.86
F	38	-	-
G	-	0.45	-
H	-	0.4	-
J	0.74	0.85	1.0

Collector connected to envelope

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

†$-V_{CBO}$ max.		60	V
†$-V_{CEO}$ max. ($-I_C$=0 to 100mA)	2N2904	40	V
	2N2904A	60	V
†$-V_{EBO}$ max.		5.0	V
†$-I_C$ max.		600	mA
P_{tot} max. (T_{amb}=25°C)		600	mW

†Temperature

T_{stg} min.	-65	°C
T_{stg} max.	200	°C
T_j max.	200	°C

THERMAL CHARACTERISTIC

$\Theta_{j\text{-amb}}$	292	degC/W

†ELECTRICAL CHARACTERISTICS (T_{amb}=25°C unless otherwise stated)

			Min.	Max.	
$-I_{CBO}$	Collector cut-off current				
	$-V_{CB}$=50V, I_E=0	2N2904	-	20	nA
		2N2904A	-	10	nA
	$-V_{CB}$=50V, I_E=0,				
	T_{amb}=150°C	2N2904	-	20	μA
		2N2904A	-	10	μA
$-I_{CEX}$	Collector-emitter cut-off current				
	$-V_{CE}$=30V, $+V_{BE}$=0.5V		-	50	nA
I_{BEX}	Base current				
	$-V_{CE}$=30V, $+V_{BE}$=0.5V		-	50	nA
$-V_{(BR)CBO}$	Collector-base breakdown voltage				
	$-I_C$=10μA, I_E=0		60	-	V
$-V_{(BR)CEO}$	*Collector-emitter breakdown voltage				
	$-I_C$=10mA, I_B=0	2N2904	40	-	V
		2N2904A	60	-	V

*Pulse condition, pulse width ≤300μs, duty cycle ≤2%.

†J.E.D.E.C. registered data.

			Min.	Max.	
$-V_{(BR)EBO}$	Emitter-base breakdown voltage $-I_E = 10\mu A$, $I_C = 0$		5.0	-	V
$-V_{CE(sat)}$	*Collector-emitter saturation voltage				
	$-I_C = 150mA$, $-I_B = 15mA$		-	0.4	V
	$-I_C = 500mA$, $-I_B = 50mA$		-	1.6	V
$-V_{BE(sat)}$	*Base-emitter saturation voltage				
	$-I_C = 150mA$, $-I_B = 15mA$		-	1.3	V
	$-I_C = 500mA$, $-I_B = 50mA$		-	2.6	V
h_{FE}	Static forward current transfer ratio				
	$-I_C = 0.1mA$, $-V_{CE} = 10V$	2N2904	20	-	
		2N2904A	40	-	
	$-I_C = 1.0mA$, $-V_{CE} = 10V$	2N2904	25	-	
		2N2904A	40	-	
	$-I_C = 10mA$, $-V_{CE} = 10V$	2N2904	35	-	
		2N2904A	40	-	
	*$-I_C = 150mA$, $-V_{CE} = 10V$		40	120	
	*$-I_C = 500mA$, $-V_{CE} = 10V$	2N2904	20	-	
		2N2904A	40	-	
c_{ob}	Common base, open circuit output capacitance $-V_{CB} = 10V$, $I_E = 0$, $f = 100kHz$		-	8.0	pF
c_{ib}	Common base, open circuit input capacitance $V_{BE} = 2.0V$, $I_C = 0$, $f = 100kHz$		-	30	pF
f_T	Transition frequency $-V_{CE} = 20V$, $-I_C = 50mA$, $f = 100MHz$		200	-	MHz

*Pulse condition, pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.

Switching characteristics

		Max.	
Turn-on (see Fig.1)			
$-V_{CC}=30V$, $-I_{CS}=150mA$, $-I_B=15mA$			
t_d	Turn-on delay time	10	ns
t_r	Rise time	40	ns
t_{on}	Turn-on time ($t_d + t_r$)	45	ns
Turn-off (see Fig.2)			
$-V_{CC}=6V$, $-I_{CS}=150mA$, $-I_B=+I_{BM}=15mA$			
t_s	Storage time	80	ns
t_t	Fall time	30	ns
t_{off}	Turn-off time ($t_s + t_f$)	100	ns

TEST CIRCUITS

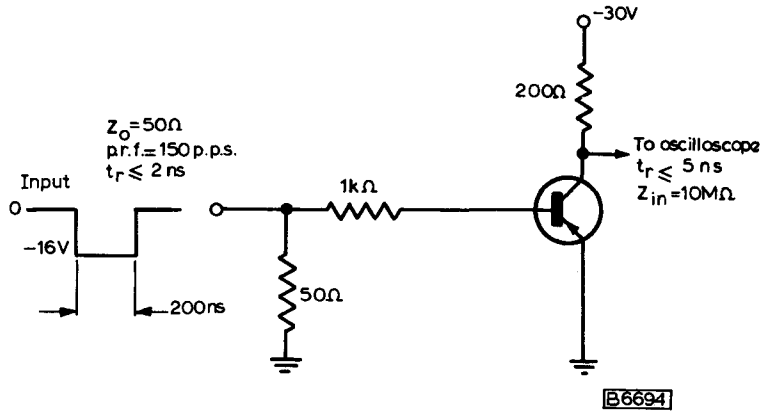


Fig.1

Test circuit for determining delay, rise and turn-on time

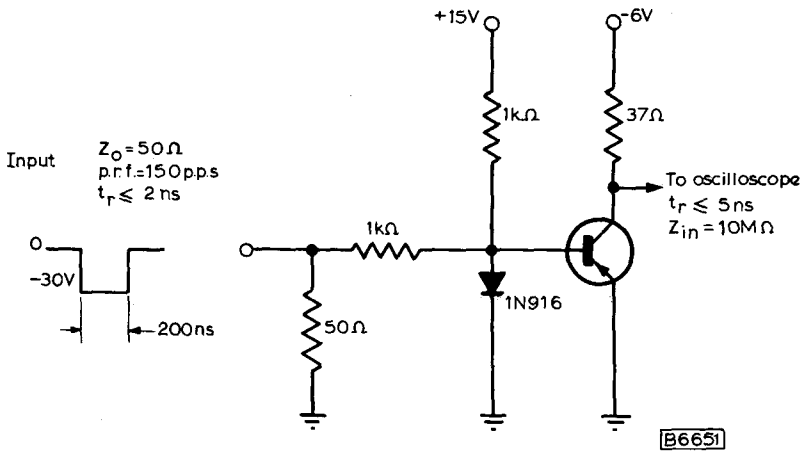


Fig.2

Test circuit for determining storage, fall and turn-off time

WAVEFORMS

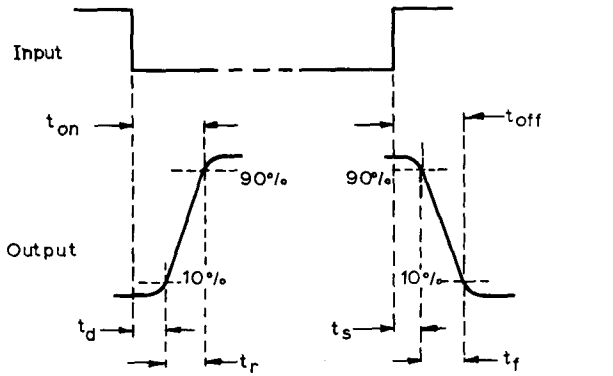
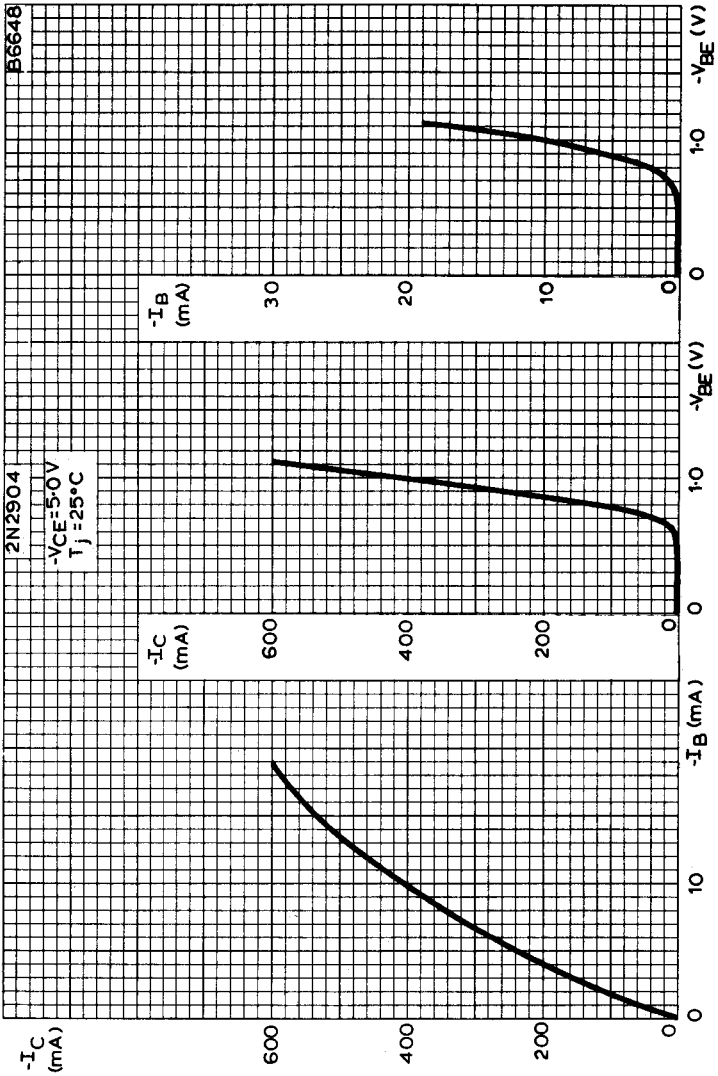
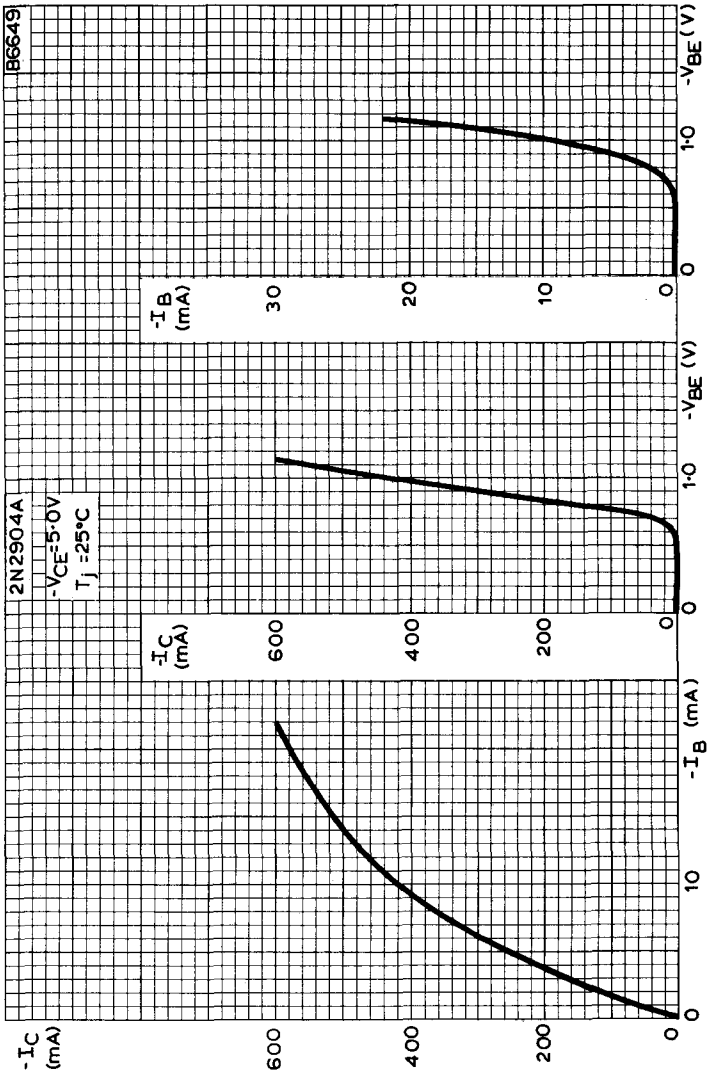


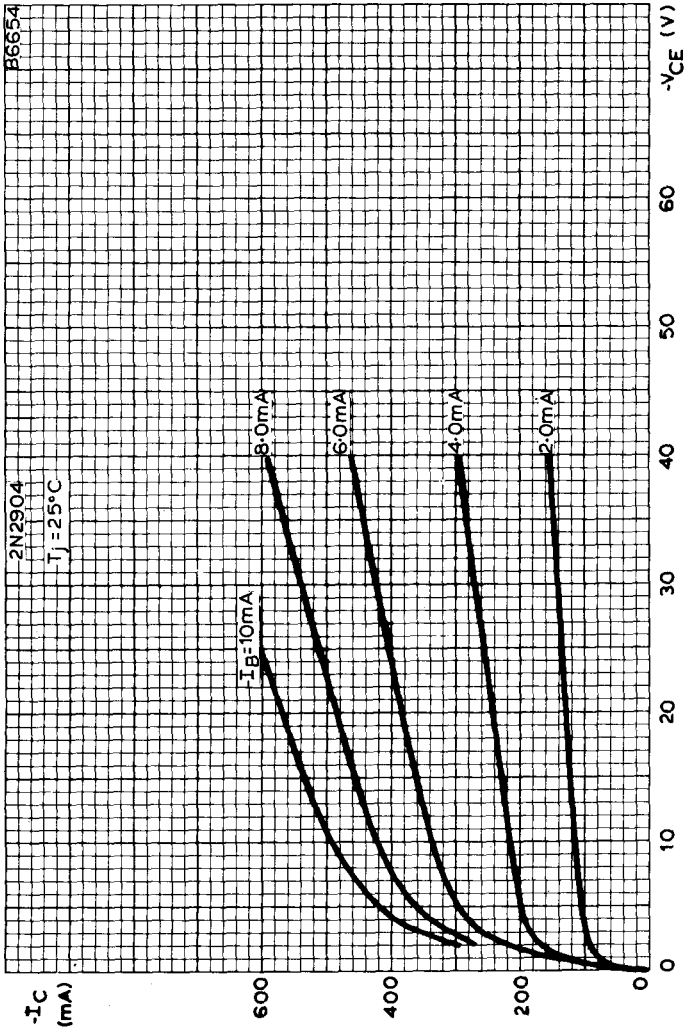
Fig. 3



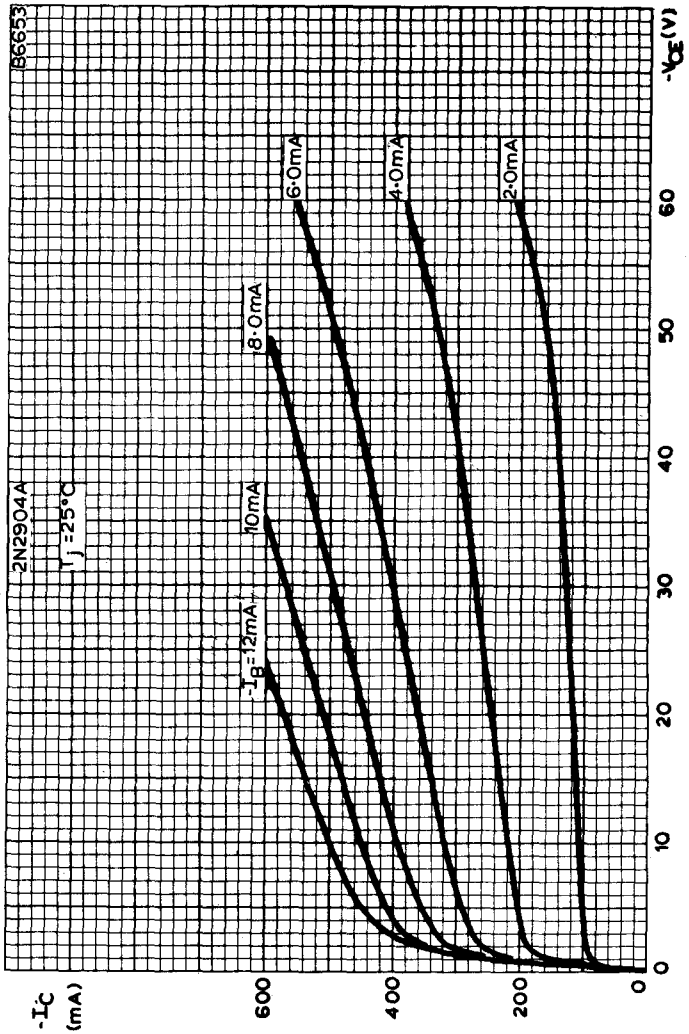
TYPICAL TRANSFER, MUTUAL AND INPUT CHARACTERISTICS



TYPICAL TRANSFER, MUTUAL AND INPUT CHARACTERISTICS



TYPICAL OUTPUT CHARACTERISTICS



TYPICAL OUTPUT CHARACTERISTICS

P-N-P SILICON PLANAR EPITAXIAL TRANSISTORS

2N2905
2N2905A

P-N-P silicon planar epitaxial medium power transistors designed primarily for high-speed saturated switching and driver applications for industrial service.

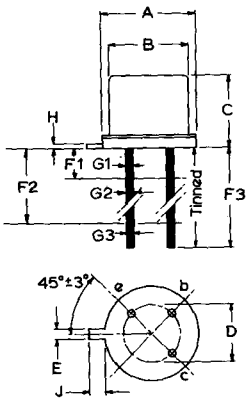
QUICK REFERENCE DATA

	2N2905	2N2905A	
$-V_{CBO}$ max.	60		V
$-V_{CEO}$ max.	40	60	V
$-I_C$ max.	600		mA
P_{tot} max. ($T_{amb}=25^oC$)	600		mW
T_j max.	200		^oC
h_{FE} ($-I_C=150mA$, $-V_{CE}=10V$)	100-300		
f_T min. ($-I_C=50mA$, $f=100MHz$)	200		MHz
t_s max. ($-I_{CS}=150mA$, $-I_B=+I_{BM}=15mA$)	80		ns

Unless otherwise stated data is applicable to both types

OUTLINE AND DIMENSIONS

Conforming to B.S. 3934 SO-3/SB3-3A
J.E.D.E.C. TO-5



	Millimetres		
	Min.	Typ.	Max.
A	9.10	-	9.39
B	8.2	-	8.50
C	6.15	-	6.60
D	-	5.08	-
E	0.71	-	0.86
F1	-	-	0.51
F2	12.7	-	-
F3	38.1	-	41.3
G1	-	-	1.01
G2	0.41	-	0.48
G3	-	-	0.53
H	-	0.4	-
J	0.74	-	1.01

Collector connected to envelope

†RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

$-V_{CBO}$ max.		60	V
$-V_{CEO}$ max. ($-I_C$=0 to 100mA)	2N2905	40	V
	2N2905A	60	V
$-V_{EBO}$ max.		5.0	V
$-I_C$ max.		600	mA
P_{tot} max. (T_{amb}=25°C)		600	mW

Temperature

T_{stg} min.	-65	°C
T_{stg} max.	200	°C
T_j max.	200	°C

†THERMAL CHARACTERISTIC

$\Theta_{j\text{-amb}}$	290	degC/W

†ELECTRICAL CHARACTERISTICS (T_{amb}=25°C unless otherwise stated)

			Min.	Max.	
$-I_{CBO}$	Collector cut-off current				
	$-V_{CB}$=50V, I_E=0	2N2905	-	20	nA
		2N2905A	-	10	nA
	$-V_{CB}$=50V, I_E=0, T_{amb}=150°C	2N2905	-	20	μA
		2N2905A	-	10	μA
$-I_{CEX}$	Collector-emitter cut-off current				
	$-V_{CE}$=30V, $+V_{BE}$=0.5V		-	50	nA
I_{BEX}	Base current				
	$-V_{CE}$=30V, $+V_{BE}$=0.5V		-	50	nA
$-V_{(BR)CBO}$	Collector-base breakdown voltage				
	$-I_C$=10μA, I_E=0		60	-	V
$-V_{(BR)CEO}$	*Collector-emitter breakdown voltage				
	$-I_C$=10mA, I_B=0	2N2905	40	-	V
		2N2905A	60	-	V

†J.E.D.E.C. registered data

*Pulse condition, pulse width ≤300μs, duty cycle ≤2%.

			Min.	Max.	
$-V_{(BR)EBO}$	Emitter-base breakdown voltage $-I_E=10\mu A$, $I_C=0$		5.0	-	V
$-V_{CE(sat)}$	*Collector-emitter saturation voltage $-I_C=150mA$, $-I_B=15mA$		-	0.4	V
	$-I_C=500mA$, $-I_B=50mA$		-	1.6	V
$-V_{BE(sat)}$	*Base-emitter saturation voltage $-I_C=150mA$, $-I_B=15mA$		-	1.3	V
	$-I_C=500mA$, $-I_B=50mA$		-	2.6	V
h_{FE}	Static forward current transfer ratio $-I_C=0.1mA$, $-V_{CE}=10V$	2N2905	35	-	
		2N2905A	75	-	
	$-I_C=1.0mA$, $-V_{CE}=10V$	2N2905	50	-	
		2N2905A	100	-	
	$-I_C=10mA$, $-V_{CE}=10V$	2N2905	75	-	
		2N2905A	100	-	
	*$-I_C=150mA$, $-V_{CE}=10V$		100	300	
	*$-I_C=500mA$, $-V_{CE}=10V$	2N2905	30	-	
		2N2905A	50	-	
C_{ob}	Common base, open circuit output capacitance $-V_{CB}=10V$, $I_E=0$, $f=100kHz$		-	8.0	pF
C_{ib}	Common base, open circuit input capacitance $+V_{BE}=2.0V$, $I_C=0$, $f=100kHz$		-	30	pF
f_T	Transition frequency $-V_{CE}=20V$, $-I_C=50mA$, $f=100MHz$		200	-	MHz

*Pulse conditions, pulse width = 300μA, duty cycle $\leq$2%.

Switching characteristics

		Max.	
Turn-on (see fig.1)			
$-V_{CC}=30V$, $-I_{CS}=150mA$, $-I_B=15mA$			
t_d	Turn-on delay time	10	ns
t_r	Rise time	40	ns
t_{on}	Turn-on time (t_d+t_r)	45	ns
Turn-off (see fig.2)			
$-V_{CC}=6.0V$, $-I_{CS}=150mA$, $-I_B=+I_{BM}=15mA$			
t_s	Storage time	80	ns
t_f	Fall time	30	ns
t_{off}	Turn-off time (t_s+t_f)	100	ns

TEST CIRCUITS

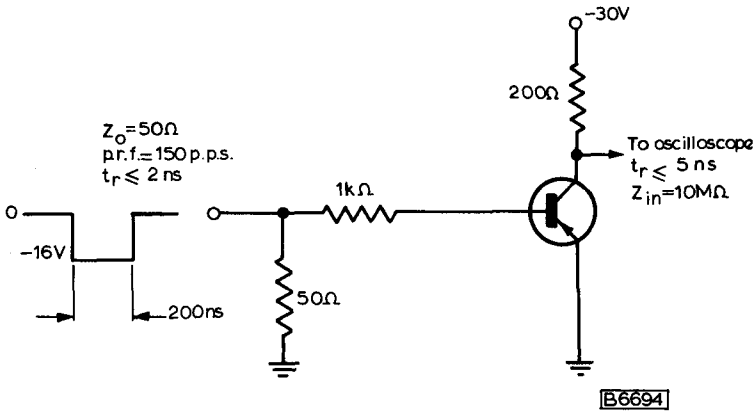


Fig.1

Test circuit for determining delay, rise and turn-on time

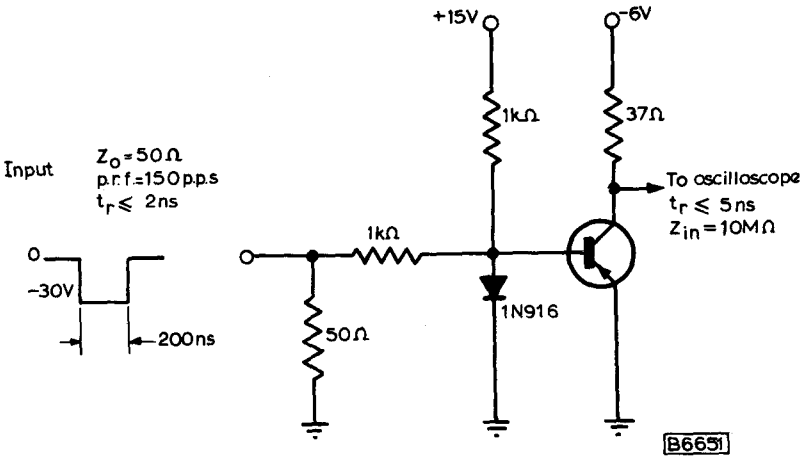


Fig. 2

Test circuit for determining storage, fall and turn-off time

WAVEFORMS

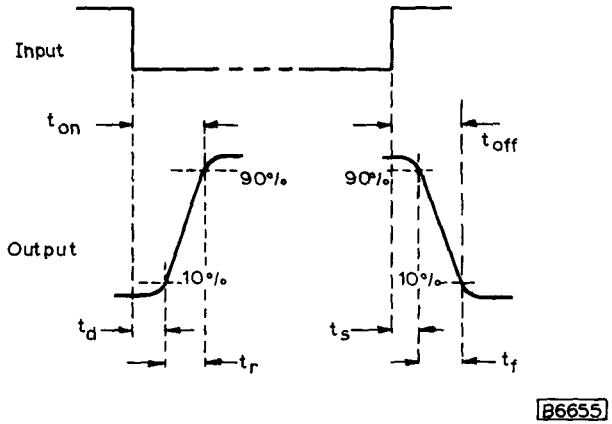


Fig. 3

P-N-P SILICON PLANAR EPITAXIAL TRANSISTORS

2N2906
2N2906A

P-N-P silicon planar epitaxial medium power transistors designed primarily for high-speed saturated switching and driver applications for industrial service.

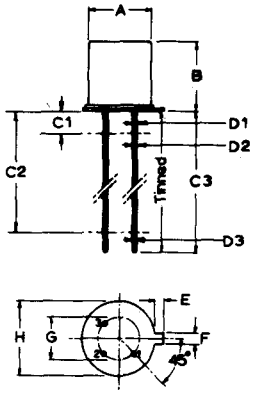
QUICK REFERENCE DATA

	2N2906	2N2906A	
$-V_{CBO}$ max.	60		V
$-V_{CEO}$ max. ($-I_C$ < 100mA)	40	60	V
$-I_C$ max.	600		mA
P_{tot} max. ($T_{amb} = 25^oC$)	400		mW
T_j max.	200		^oC
h_{FE} ($-I_C$ = 150mA, $-V_{CE}$ = 10V)	40-120		
f_T min. ($-I_C$ = 50mA, f = 100MHz)	200		MHz
t_s max. ($-I_{CS}$ = 150mA, $-I_B = +I_{BM}$ = 15mA)	80		ns

Unless otherwise stated data is applicable to both types

OUTLINE AND DIMENSIONS

Conforms to J.E.D.E.C. TO-18
B.S. 3934 SO-12A/SB3-6A



Viewed from underside

	Millimetres		
	Min.	Typ.	Max.
A	4.53	-	4.8
B	4.66	-	5.33
C1	-	-	0.51
C2	12.7	-	-
C3	12.7	-	15
D1	-	-	1.01
D2	0.41	-	0.48
D3	-	-	0.53
E	0.84	-	1.17
F	0.92	-	1.16
G	-	2.54	-
H	5.31	-	5.84

Connections 1. Emitter 3. Collector connected to envelope
2. Base

†RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

$-V_{CBO}$ max.		60	V
$-V_{CEO}$ max. ($-I_C$ = 0 to 100mA)	2N2906	40	V
	2N2906A	60	V
$-V_{EBO}$ max.		5.0	V
$-I_C$ max.		600	mA
P_{tot} max. (T_{amb} = 25°C)		400	mW

Temperature

T_{stg} min.	-65	°C
T_{stg} max.	200	°C
T_j max.	200	°C

†THERMAL CHARACTERISTIC

$\Theta_{j\text{-amb}}$	0.44	degC/mW

†ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise stated)

			Min.	Max.	
$-I_{CBO}$	Collector cut-off current				
	$-V_{CB}$ = 50V, I_E = 0	2N2906	-	20	nA
		2N2906A	-	10	nA
	$-V_{CB}$ = 50V, I_E = 0,				
	T_{amb} = 150°C	2N2906	-	20	μA
		2N2906A	-	10	μA
$-I_{CEX}$	Collector-emitter cut-off current				
	$-V_{CE}$ = 30V, $+V_{BE}$ = 0.5V		-	50	nA
I_{BEX}	Base current				
	$-V_{CE}$ = 30V, $+V_{BE}$ = 0.5V		-	50	nA
$-V_{(BR)CBO}$	Collector-base breakdown voltage				
	$-I_C$ = 10μA, I_E = 0		60	-	V
$-V_{(BR)CEO}$	*Collector-emitter breakdown voltage				
	$-I_C$ = 10mA, I_B = 0	2N2906	40	-	V
		2N2906A	60	-	V

*Pulse condition, pulse width≤300μs, duty cycle≤2%.

†J.E.D.E.C. registered data.

			Min.	Max.	
$-V_{(BR)EBO}$	Emitter-base breakdown voltage $-I_E = 10\mu A$, $I_C = 0$		5.0	-	V
$-V_{CE(sat)}$	*Collector-emitter saturation voltage $-I_C = 150mA$, $-I_B = 15mA$		-	0.4	V
	$-I_C = 500mA$, $-I_B = 50mA$		-	1.6	V
$-V_{BE(sat)}$	*Base-emitter saturation voltage $-I_C = 150mA$, $-I_B = 15mA$		-	1.3	V
	$-I_C = 500mA$, $-I_B = 50mA$		-	2.6	V
h_{FE}	Static forward current transfer ratio				
	$-I_C = 0.1mA$, $-V_{CE} = 10V$	2N2906	20	-	
		2N2906A	40	-	
	$-I_C = 1.0mA$, $-V_{CE} = 10V$	2N2906	25	-	
		2N2906A	40	-	
	$-I_C = 10mA$, $-V_{CE} = 10V$	2N2906	35	-	
		2N2906A	40	-	
	*$-I_C = 150mA$, $-V_{CE} = 10V$		40	120	
	*$-I_C = 500mA$, $-V_{CE} = 10V$	2N2906	20	-	
		2N2906A	40	-	
C_{ob}	Common base, open circuit output capacitance $-V_{CB} = 10V$, $I_E = 0$, $f = 100kHz$		-	8.0	pF
C_{ib}	Common base, open circuit input capacitance $V_{BE} = 2.0V$, $I_C = 0$, $f = 100kHz$		-	30	pF
f_T	Transition frequency $-V_{CE} = 20V$, $-I_C = 50mA$, $f = 100MHz$		200	-	MHz

*Pulse condition, pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.

Switching characteristics

		Max.	
Turn-on (see Fig.1)			
$-V_{CC}=30V$, $-I_{CS}=150mA$, $-I_B=15mA$			
t_d	Turn-on delay time	10	ns
t_r	Rise time	40	ns
t_{on}	Turn-on time ($t_d + t_r$)	45	ns
Turn-off (see Fig.2)			
$-V_{CC}=6V$, $-I_{CS}=150mA$, $-I_B=+I_{BM}=15mA$			
t_s	Storage time	80	ns
t_f	Fall time	30	ns
t_{off}	Turn-off time ($t_s + t_f$)	100	ns

TEST CIRCUITS

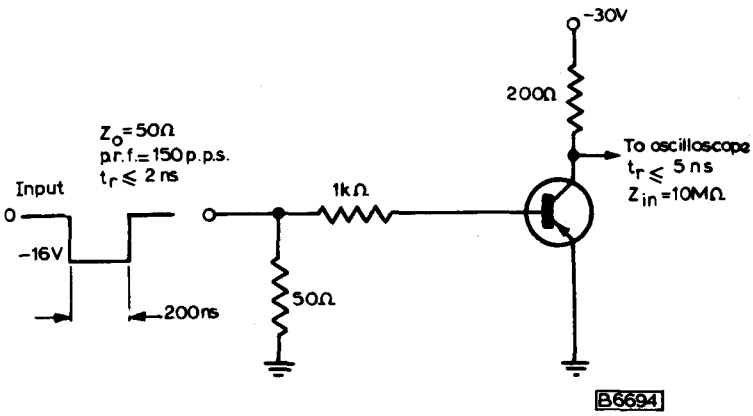


Fig.1

Test circuit for determining delay, rise and turn-on time

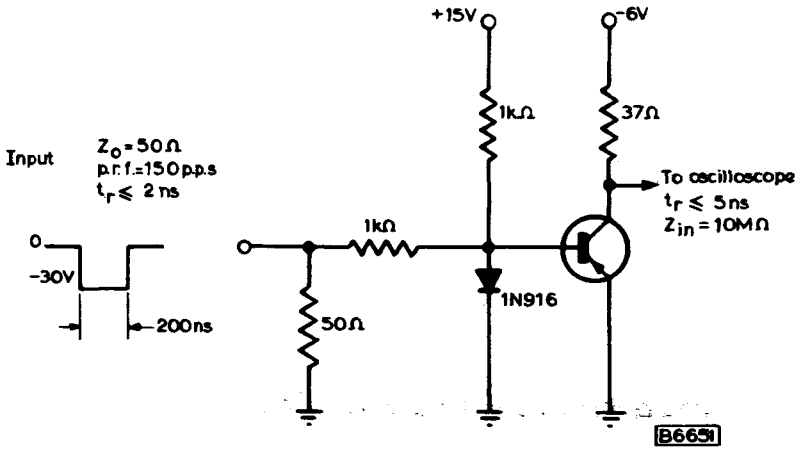


Fig. 2

Test circuit for determining storage, fall and turn-off time

WAVEFORMS

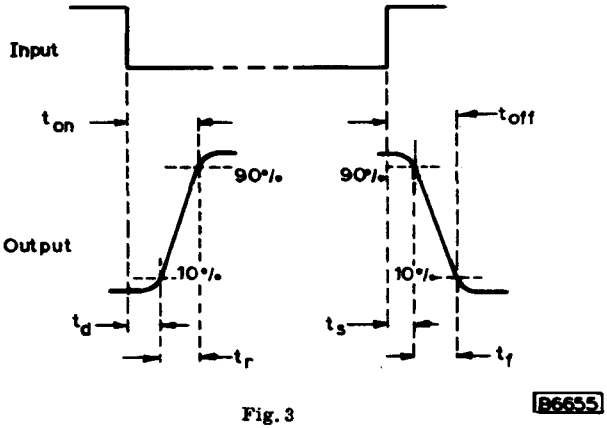


Fig. 3

P-N-P SILICON PLANAR EPITAXIAL TRANSISTORS

2N2907
2N2907A

P-N-P silicon planar epitaxial medium power transistors designed primarily for high-speed saturated switching and driver applications for industrial service.

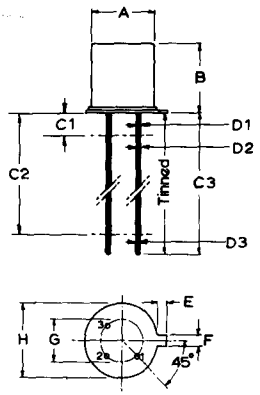
QUICK REFERENCE DATA

	2N2907	2N2907A	
$-V_{CBO}$ max.	60		V
$-V_{CEO}$ max. ($-I_C$ < 100mA)	40	60	V
$-I_C$ max.	600		mA
P_{tot} max. ($T_{amb} = 25^oC$)	400		mW
T_j max.	200		^oC
h_{FE} ($-I_C = 150mA$, $-V_{CE} = 10V$)	100-300		
f_T min. ($-I_C = 50mA$, f = 100MHz)	200		MHz
t_s max. ($-I_{CS} = 150mA$, $-I_B = +I_{BM} = 15mA$)	80		ns

Unless otherwise stated data is applicable to both types

OUTLINE AND DIMENSIONS

Conforms to J.E.D.E.C. TO-18
B.S. 3934 SO-12A/SB3-6A



Viewed from underside

	Millimetres		
	Min.	Typ.	Max.
A	4.53	-	4.8
B	4.66	-	5.33
C1	-	-	0.51
C2	12.7	-	-
C3	12.7	-	15
D1	-	-	1.01
D2	0.41	-	0.48
D3	-	-	0.53
E	0.84	-	1.17
F	0.92	-	1.16
G	-	2.54	-
H	5.31	-	5.84

Connections 1. Emitter 3. Collector connected to envelope
2. Base

†RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

$-V_{CBO}$ max.		60	V
$-V_{CEO}$ max. ($-I_C$ = 0 to 100mA)	2N2907	40	V
	2N2907A	60	V
$-V_{EBO}$ max.		5.0	V
$-I_C$ max.		600	mA
P_{tot} max. (T_{amb} = 25°C		400	mW

Temperature

T_{stg} min.	-65	°C
T_{stg} max.	200	°C
T_j max.	200	°C

†THERMAL CHARACTERISTIC

$\Theta_{j\text{-amb}}$	0.44	degC/mW

†ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless otherwise stated)

			Min.	Max.	
$-I_{CBO}$	Collector cut-off current				
	$-V_{CB}$ = 50V, I_E = 0	2N2907	-	20	nA
		2N2907A	-	10	nA
	$-V_{CB}$ = 50V, I_E = 0,				
	T_{amb} = 150°C	2N2907	-	20	μA
		2N2907A	-	10	μA
$-I_{CEX}$	Collector-emitter cut-off current				
	$-V_{CE}$ = 30V, $+V_{BE}$ = 0.5V		-	50	nA
I_{BEX}	Base current				
	$-V_{CE}$ = 30V, $+V_{BE}$ = 0.5V		-	50	nA
$-V_{(BR)CBO}$	Collector-base breakdown voltage				
	$-I_C$ = 10μA, I_E = 0		60	-	V
$-V_{(BR)CEO}$	*Collector-emitter breakdown voltage				
	$-I_C$ = 10mA, I_B = 0	2N2907	40	-	V
		2N2907A	60	-	V

*Pulse condition, pulse width≤300μs, duty cycle≤2%.

†J.E.D.E.C. registered data

			Min.	Max.	
$-V_{(BR)EBO}$	Emitter-base breakdown voltage $-I_E = 10\mu A$, $I_C = 0$		5.0	-	V
$-V_{CE(sat)}$	*Collector-emitter saturation voltage				
	$-I_C = 150mA$, $-I_B = 15mA$		-	0.4	V
	$-I_C = 500mA$, $-I_B = 50mA$		-	1.6	V
$-V_{BE(sat)}$	*Base-emitter saturation voltage				
	$-I_C = 150mA$, $-I_B = 15mA$		-	1.3	V
	$-I_C = 500mA$, $-I_B = 50mA$		-	2.6	V
h_{FE}	Static forward current transfer ratio				
	$-I_C = 0.1mA$, $-V_{CE} = 10V$	2N2907	35	-	
		2N2907A	75	-	
	$-I_C = 1.0mA$, $-V_{CE} = 10V$	2N2907	50	-	
		2N2907A	100	-	
	$-I_C = 10mA$, $-V_{CE} = 10V$	2N2907	75	-	
		2N2907A	100	-	
	$*-I_C = 150mA$, $-V_{CE} = 10V$		100	300	
	$*-I_C = 500mA$, $-V_{CE} = 10V$	2N2907	30	-	
		2N2907A	50	-	
C_{ob}	Common base, open circuit output capacitance $-V_{CB} = 10V$, $I_E = 0$, $f = 100kHz$		-	8.0	pF
C_{ib}	Common base, open circuit input capacitance $+V_{BE} = 2.0V$, $I_C = 0$, $f = 100kHz$		-	30	pF
f_T	Transition frequency $-V_{CE} = 20V$, $-I_C = 50mA$, $f = 100MHz$		200	-	MHz

*Pulse conditions, pulse width = 300μA, duty cycle ≤2%.

Switching characteristics

		Max.	
Turn-on (see fig.1)			
$-V_{CC}=30V$, $-I_{CS}=150mA$, $-I_B=15mA$			
t_d	Turn-on delay time	10	ns
t_r	Rise time	40	ns
t_{on}	Turn-on time (t_d+t_r)	45	ns
Turn-off (see fig.2)			
$-V_{CC}=6.0V$, $-I_{CS}=150mA$, $-I_B=+I_{BM}=15mA$			
t_s	Storage time	80	ns
t_f	Fall time	30	ns
t_{off}	Turn-off time (t_s+t_f)	100	ns

TEST CIRCUITS

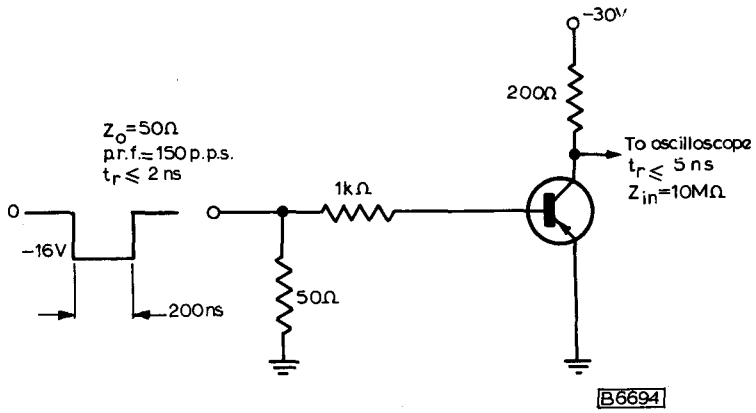


Fig.1

Test circuit for determining delay, rise and turn-on time

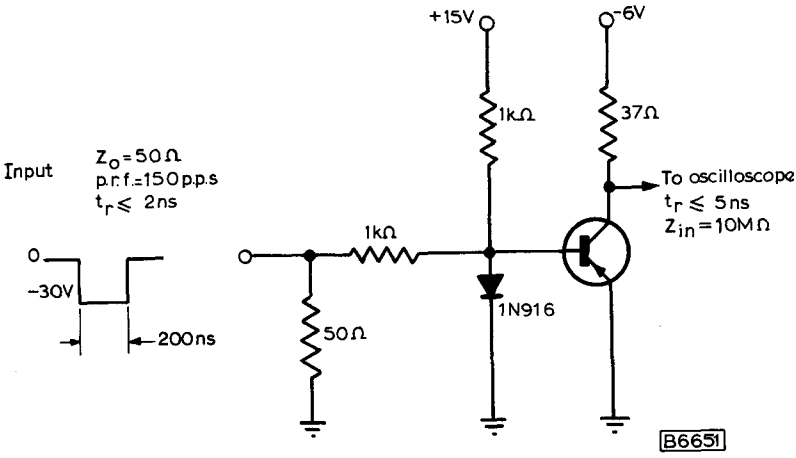


Fig. 2

Test circuit for determining storage, fall and turn-off time

WAVEFORMS

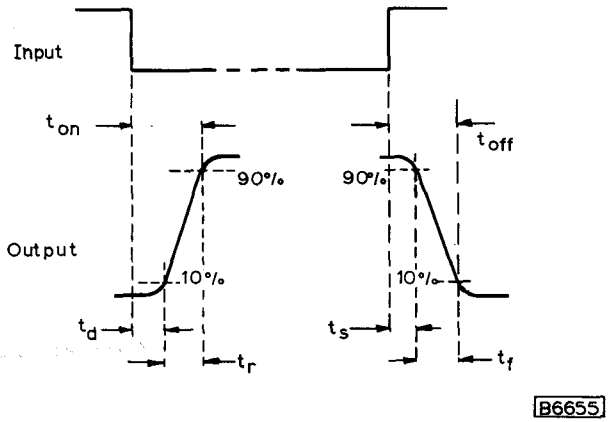


Fig. 3

N-P-N SILICON PLANAR TRANSISTOR

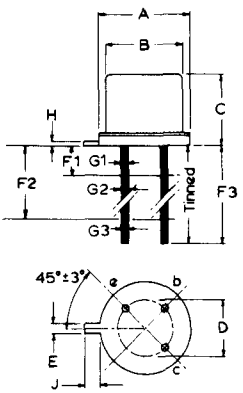
2N3053

N-P-N silicon planar transistor designed for medium speed, saturated and nonsaturated switching applications for industrial service.

QUICK REFERENCE DATA		
V_{CBO} max.	60	V
V_{CEO} max.	40	V
I_C max.	700	mA
P_{tot} max. ($T_{case} = 25^oC$)	5.0	W
T_j max.	200	^oC
h_{FE} ($I_C = 150mA$, $V_{CE} = 10V$)	50-250	
f_T min. ($I_C = 50mA$, $V_{CE} = 10V$, $f = 20MHz$)	100	MHz

OUTLINE AND DIMENSIONS

Conforming to B.S. 3934 SO-3/SB3-3A
J.E.D.E.C. TO-5



	Millimetres		
	Min.	Nom.	Max.
A	9. 10	-	9.39
B	8.20	-	8.50
C	6.15	-	6.60
D	-	5.08	-
E	0.71	-	0.86
F1	-	-	0.51
F2	12.7	-	-
F3	38.1	-	41.3
G1	-	-	1.01
G2	0.41	-	0.48
G3	-	-	0.53
H	-	0.4	-
J	0.74	-	1.01

Collector connected to case

†RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{CBO} max.	60	V
*V_{CEO} max.	40	V
V_{EBO} max.	5.0	V
I_C max.	700	mA
P_{tot} max. ($T_{case}=25^oC$)	5.0	W

Temperature

T_{stg} min.	-65	^oC
T_{stg} max.	200	^oC
T_j max.	200	^oC

*For $I_C=0$ to 100mA (pulsed), pulse duration=300μs, duty factor = 1.8%; 0 to 700mA for shorter pulses.

†THERMAL CHARACTERISTIC

$\Theta_{j\text{-case}}$ (above 25^oC)	35	degC/W

†ELECTRICAL CHARACTERISTICS ($T_{amb}=25^oC$)

		Min.	Max.	
I_{CEX}	Collector-emitter cut-off current $V_{CE}=60V$, $-V_{BE}=1.5V$	-	0.25	μA
$-I_{BEX}$	Base current $V_{CE}=60V$, $-V_{BE}=1.5V$	-	0.25	μA
$V_{(BR)CBO}$	Collector-base breakdown voltage $I_C=100\mu A$, $I_E=0$	60	-	V
$V_{(BR)EBO}$	Emitter-base breakdown voltage $I_E=100\mu A$, $I_C=0$	5.0	-	V
	**Collector-emitter breakdown voltage			
$V_{(BR)CEO}$	$I_C=100\mu A$, $I_B=0$	40	-	V
$V_{(BR)CER}$	$I_C=100mA$, $R_{BE}=10\Omega$	50	-	V

**Pulse test, pulse width=300μs, duty factor=1.8%.

†J.E.D.E.C. registered data.

ELECTRICAL CHARACTERISTICS (cont'd)

		Min.	Max.	
$V_{CE(sat)}$	Collector-emitter saturation voltage $I_C = 150mA$, $I_B = 15mA$	-	1.4	V
$V_{BE(sat)}$	Base-emitter saturation voltage $I_C = 150mA$, $I_B = 15mA$	-	1.7	V
V_{BE}	Base-emitter voltage $I_C = 150mA$, $V_{CE} = 2.5V$	-	1.7	V
h_{FE}	Static forward current transfer ratio $I_C = 150mA$, $V_{CE} = 2.5V$	25	-	
	**$I_C = 150mA$, $V_{CE} = 10V$	50	250	
f_T	Transition frequency $I_C = 50mA$, $V_{CE} = 10V$, $f = 20MHz$	100	-	MHz
C_{ob}	Output capacitance $V_{CB} = 10V$, $I_C = 0$, $f = 140kHz$	-	15	pF
C_{ib}	Input capacitance $V_{EB} = 0.5V$, $I_E = 0$, $f = 140kHz$	-	80	pF

**Pulse test, pulse width = 300μs, duty factor = 1.8%.

N-P-N SILICON DIFFUSED POWER TRANSISTOR

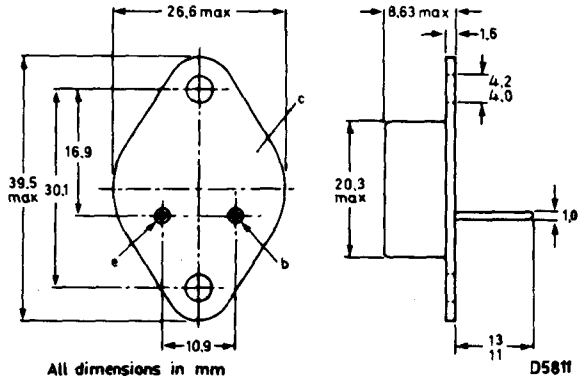
2N3055

N-P-N silicon diffused power transistor, intended for high quality amplifiers, power supplies, inverters and similar industrial applications.

QUICK REFERENCE DATA		
V_{CBO} max.	100	V
V_{CER} max. (R_{BE}=100Ω)	70	V
I_C max.	15	A
P_{tot} max. (T_{mb}≤25°C)	115	W
T_j max.	200	°C
h_{FE} (I_C=4.0A, V_{CE}=4.0V)	20-70	
f_T min. (I_C=1.0A, V_{CE}=4.0V, f=1.0MHz)	0.8	MHz

OUTLINE AND DIMENSIONS

Conforming to B.S. 3934 SO-5B/SB2-2
J.E.D.E.C. TO-3



Collector connected to envelope

Accessories available: 56239A (insulating bush), 56201B (mica washer), 56214 (lead washer)

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{CBO} max.	100	V
V_{CER} max. (R_{BE} = 100Ω)	70	V
V_{EBO} max.	7.0	V
I_C max.	15	A
I_B max.	7.0	A
P_{tot} max. ($T_{mb} \leq 25^oC$)	115	W

Temperature

T_{stg} range	-65 to +200	^oC
T_j max.	200	^oC

THERMAL CHARACTERISTIC

$R_{th(j-mb)}$	1.5	degC/W

ELECTRICAL CHARACTERISTICS ($T_j = 25^oC$ unless otherwise stated)

		Min.	Max.	
	Collector cut-off current			
I_{CEO}	V_{CE} = 30V, I_B = 0	-	0.7	mA
I_{CEX}	V_{CE} = 100V, $-V_{BE}$ = 1.5V	-	5.0	mA
I_{CEX}	V_{CE} = 100V, $-V_{BE}$ = 1.5V, T_j = 150°C	-	10	mA
I_{EBO}	Emitter cut-off current V_{EB} = 7.0V, I_C = 0	-	5.0	mA
	Collector-emitter sustaining voltage			
$V_{CEO(sust)}$	I_C = 0.2A, I_B = 0	60	-	V
$V_{CER(sust)}$	I_C = 0.2A, R_{BE} = 100Ω	70	-	V
V_{BE}	Base-emitter voltage I_C = 4.0A, V_{CE} = 4.0V	-	1.8	V
$V_{CE(sat)}$	Collector-emitter saturation voltage			
	I_C = 4.0A, I_B = 0.4A	-	1.1	V
	I_C = 10A, I_B = 3.3A	-	4.0	V

ELECTRICAL CHARACTERISTICS (cont'd)

		Min.	Max.	
h_{FE}	Static forward current transfer ratio I_C=4.0A, V_{CE}=4.0V	20	70	
f_T	Transition frequency I_C=1.0A, V_{CE}=4.0V, f=1.0MHz	0.8	-	MHz
h_{fe}	Small signal forward current transfer ratio I_C=1.0A, V_{CE}=4.0V, f=1.0kHz	15	-	

SILICON V.H.F. N-P-N POWER TRANSISTORS

2N3375
2N3553
2N3632

The 2N3553, 2N3375, and 2N3632 are silicon power transistors. The 2N3553 and 2N3375 are designed for v.h.f./u.h.f. application and the 2N3632 for v.h.f. application in industrial and military transmitting equipment.

QUICK REFERENCE DATA

	2N3553	2N3375	2N3632	
V_{CBO} max.	65	65	65	V
V_{CEO} max.	40	40	40	V
I_{CM} max.	1.0	1.5	3.0	A
P_{tot} max. ($T_{mb} \leqslant 25°C$)	7.0	11.6	23	W
T_j max. (operating)	200	200	200	°C
f_T typ.	500	500	400	MHz
Output power				
at V_{CE} = 28V, common emitter				
P_{out} min. (P_{in} = 0.25W, f = 175MHz)	2.5	—	—	W
P_{out} min. (P_{in} = 1.0W, f = 100MHz)	—	7.5	—	W
P_{out} min. (P_{in} = 1.0W, f = 400MHz)	—	3.0	—	W
P_{out} min. (P_{in} = 3.5W, f = 175MHz)	—	—	13.5	W

OUTLINE AND DIMENSIONS

For details see page D4.

2N3553 Conforms to J.E.D.E.C. TO-39, B.S. 3934 SO-3/SB3-3B
2N3375 and 2N3632 Conform to J.E.D.E.C. TO-60

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

	2N3553	2N3375	2N3632	
V_{CBO} max.	65	65	65	V
V_{CEO} max.	40	40	40	V
V_{EBO} max.	4.0	4.0	4.0	V
I_C max.	0.35	0.5	1.0	A
I_{CM} max.	1.0	1.5	3.0	A
*P_{tot} max.($T_{mb} \leqslant 25°C$)	7.0	11.6	23	W

Temperature

T_{stg} min.		−65	°C
T_{stg} max.		+200	°C
T_j max. (operating)		+200	°C

*See safe operation area curves on pages C1 and C2

THERMAL CHARACTERISTICS

θ_{j-mb}	25	15	7.5	degC/W
θ_{mb-h}	—	0.6	0.6	degC/W
θ_{mb-h} (mounted with top clamping washer of accessory 56218)	1.0	—	—	degC/W
θ_{mb-h} (mounted with top clamping washer of accessory 56218 and a Boron nitride washer for electrical insulation)	1.2	—	—	degC/W

ELECTRICAL CHARACTERISTICS (T_j = 25°C)

$V_{(BR)CBO}$ min.	Collector-base breakdown voltage I_C = 250μA, I_E = 0	65	65	65	V
$V_{(BR)CEX}$ min.**	Collector-emitter breakdown voltage I_C = 0 to 200mA, V_{EB} = 1.5V, R_B = 33Ω	65	65	65	V
$V_{(BR)CEO}$ min.**	I_C = 0 to 200mA, I_B = 0	40	40	40	V
$V_{(BR)EBO}$ min.	Emitter-base breakdown voltage I_E = 250μA, I_C = 0	4.0	4.0	4.0	V
I_{CEO} max.	Collector cut-off current V_{CE} = 30V, I_B = 0	100	100	250	μA
h_{FE}	Large signal forward current transfer ratio				
	I_C = 125mA, V_{CE} = 5.0V min.	15	15	—	
	max.	200	200	—	
	I_C = 250mA, V_{CE} = 5.0V min.	10	10	10	
	max.	100	100	150	
	I_C = 1000mA, V_{CE} = 5.0V min.	—	—	5	
	max.	—	—	110	

**Pulsed through an inductor (25mH); δ = 0.5; f = 50Hz.

SILICON V.H.F. N-P-N POWER TRANSISTORS

2N3375
2N3553
2N3632

ELECTRICAL CHARACTERISTICS ($T_j = 25°C$)

			2N3553	2N3375	2N3632	
V_{BE}	Base-Emitter Voltage (max.)					
	$I_C = 250mA$, $V_{CE} = 5V$		1.5	—	—	V
	$I_C = 500mA$, $V_{CE} = 5V$		—	1.5	—	V
	$I_C = 1000mA$, $V_{CE} = 5V$		—	—	1.5	V
$V_{CE(Sat)}$	Collector-emitter saturation voltage (max.)					
	$I_C = 250mA$, $I_B = 50mA$		1.0	—	—	V
	$I_C = 500mA$, $I_B = 100mA$		—	1.0	—	V
	$I_C = 1000mA$, $I_B = 200mA$		—	—	1.0	V
f_T typ.	Transition frequency					
	$V_{CE} = 28V$, $I_C = 125mA$		500	500	—	MHz
	$= 500mA$		—	—	400	MHz
C_{te}	Collector capacitance					
	$V_{CB} = 28V$, $I_E = I_e = 0$, $f = 1MHz$	(max.)	10	10	20	pF
C_C	Collector-case capacitance	(max.)	—	6.0	6.0	pF
$R_{e(hie)}$	Real part of input impedance					
	$f = 200MHz$, $I_C = 125mA$, $V_{CE} = 28V$	(max.)	20	20	—	Ω
	$f = 200MHz$, $I_C = 250mA$, $V_{CE} = 28V$	(max.)	—	—	20	Ω

R.F. Performance

in un-neutralised common emitter amplifier

$V_{CE} = 28V$

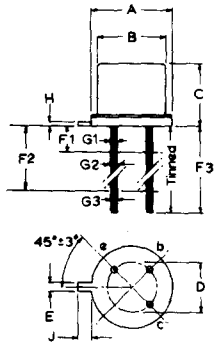
Type	Freq.	Power out	Power in	I_C	η	Circuit No,
2N3553	175MHz	2.5W	<0.25W	<180mA	>50%	fig 2
2N3375	100MHz	7.5W	<1.0W	<410mA	>65%	fig 1
2N3375	400MHz	>3.0W	1.0W	270mA	>40%	fig 3
2N3632	175MHz	>13.5W	3.5W	690mA	>70%	fig 2

The transistors can withstand an output V.S.W.R. of 3 : 1 varied through all phases for the conditions mentioned in the above table.

OUTLINE AND DIMENSIONS FOR 2N3553

Conforms to J.E.D.E.C. TO-39

B.S.3934 SO-3/SB3-3B

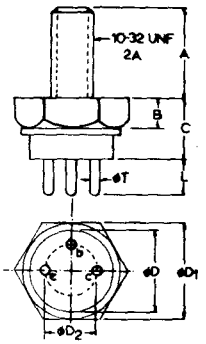


	Millimetres		
	Min.	Nom.	Max.
A	8.64	8.9	9.4
B	7.75	8.15	8.5
C	6.1	6.36	6.6
D	–	5.08	–
E	0.71	0.79	0.86
F	13	–	–
H	–	0.4	–
J	0.74	0.85	1.0

Collector connected to case

OUTLINE AND DIMENSIONS FOR 2N3375, 2N3632

Conforms to TO-60



	Millimetres
	Nom.
A	11.10
B	3.18
C	6.86
ϕD	8.38
ϕD_1	10.92
ϕD_2	5.08
L	3.81
ϕT	0.97

SILICON V.H.F. N-P-N POWER TRANSISTORS

2N3375
2N3553
2N3632

SOLDERING AND WIRING RECOMMENDATIONS (2N3553)

1. When using a soldering iron, transistors may be soldered directly into the circuit, but heat conducted to the junction should if possible be kept to a minimum by the use of a thermal shunt.
2. Transistors may be dip-soldered at a solder temperature of 245°C for a maximum soldering time of 5 seconds. The case temperature during soldering must not at any time exceed the maximum storage temperature. These recommendations apply to a transistor mounted flush on a board having punched-through holes, or spaced at least 1.5mm above a board having plated-through holes.
3. Care should be taken not to bend the leads nearer than 1.5mm from the seal.
4. If devices are stored at temperatures above 100°C before incorporation into equipment, some deterioration of the external surface is likely to occur which may make soldering into the circuit difficult. Under these circumstances the leads should be retinned using a suitable activated, flux.

NOTES (2N3375, 2N3632)

1. A heatsink thermal resistance of 3degC/W is recommended for operation in ambient temperature up to 65°C.

CAUTION

This device incorporates Beryllium Oxide, the dust of which is toxic. The device is entirely safe provided that it is not dismantled.
Care should be taken to ensure that all those who may handle, use or dispose of this device are aware of its nature and of the necessary safety precautions. In particular, it should never be thrown out with general industrial or domestic waste.

DISPOSAL SERVICE

Devices requiring disposal may be returned to Mullard Service Department. They must be separately and securely packed and clearly identified. If any are damaged or broken they MUST NOT be sent through the post. In this case advice is available from the Service Department.

Service Department,
Mullard Limited,
New Road,
Mitcham,
Surrey.

COMMON EMITTER TEST CIRCUIT 100MHz 2N3375

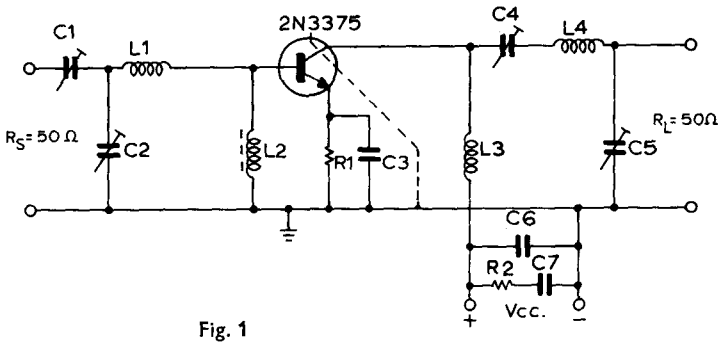


Fig. 1

C_1	= 3,5–61,5pF	air trimmer.
C_2	= 3,5–61,5pF	air trimmer.
C_3	= 10nF	polyester.
C_4	= 4–29pF	air trimmer.
C_5	= 4–29pF	air trimmer.
C_6	= 330pF	ceramic.
C_7	= 10ηF	polyester.

L_1 = 2 turns of 1.5mm closely wound enamelled Cu wire, int. diam. 10mm, leads: 2 × 10mm.

L_2 = Ferroxcube choke coil, Z (at 100MHz) = 700Ω ± 20%.

L_3 = 23 turns of 0.7mm closely wound enamelled Cu wire, int. diam. 6mm.

L_4 = 5 turns of 1.5mm closely wound enamelled Cu wire, int. diam. 12mm, leads: 2 × 10mm.

R_1 = 1.35Ω carbon.

R_2 = 10Ω carbon.

COMMON EMITTER TEST CIRCUIT 175MHz 2N3553, 2N3632

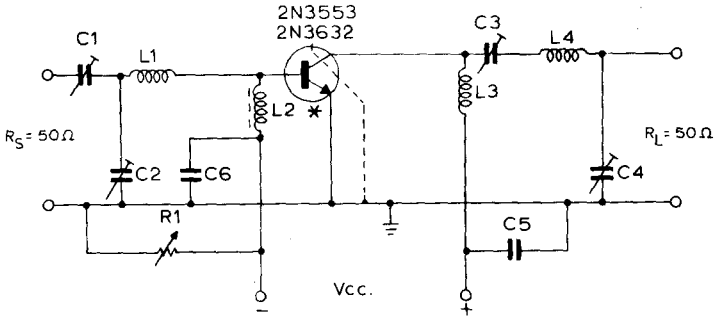


Fig. 2

C_1, C_2, C_3, C_4 = 4–29pF air trimmer.

C_5 = 10nF polyester.

C_6 = 100pF ceramic.

L_1 = 1 turn of 1mm Cu wire, int. diam. 10mm; Leads: 2 × 10mm.

L_2 = Ferroxcube choke coil. Z (at 175MHz) = 550Ω ± 20%.

L_3 = 15 turns of 0.7mm closely wound enamelled Cu wire, int. diam 4mm.

L_4 = 3 turns of 1.5mm closely wound enamelled Cu wire, int. diam 12mm, Leads: 2 × 20mm.

R = 0–2Ω for 2N3632 and R = 0Ω for 2N3553.

*Emitter of the 2N3632 is connected to case as short as possible. The length of the external emitter wire of the 2N3553 is 1.6mm.

COMMON EMITTER TEST CIRCUIT 400MHz 2N3375

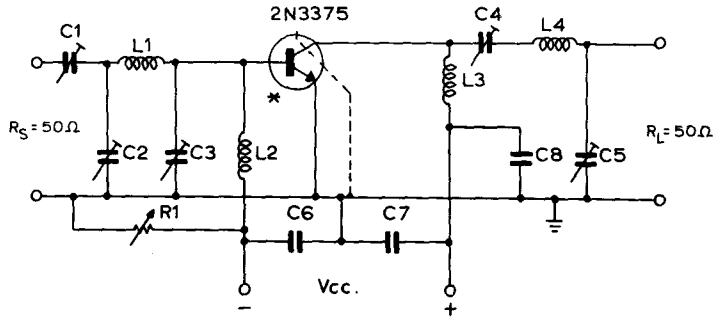


Fig. 3

C_1	= 0.7–6.7pF	ceramic trimmer.
C_2	= 0.7–6.7pF	ceramic trimmer.
C_3	= 0.5–3.5pF	ceramic trimmer.
C_4	= 3–19pF	air trimmer.
C_5	= 3–19pF	air trimmer.
C_6	= 15pF	ceramic.
C_7	= 15pF	ceramic.
C_8	= 4700pF	ceramic.

L_1 = 20mm straight Cu wire diam. 1.5mm, spaced 8mm from chassis.
L_2 = 17 turns of 0.5mm closely wound enamelled Cu wire, int. diam. 3mm.
L_3 = 7 turns of 0.5mm closely wound enamelled Cu wire, int. diam. 3mm.
L_4 = 1 turn of 1.5mm Cu wire, int. diam. 10mm, leads: 2 × 5mm.

R = 0–5Ω.

*Emitter connected to case as short as possible.

FREQUENCY DOUBLER TEST CIRCUIT 87.5MHz–175MHz 2N3553

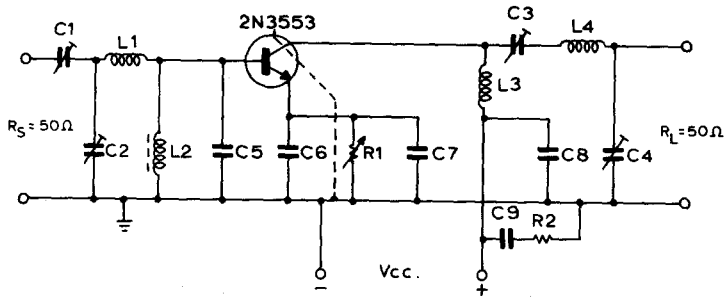


Fig. 4

C_1, C_2, C_3 = 4–29pF air trimmer.

C_4 = 3.5–61.5pF air trimmer.

C_5 = 56pF ceramic.

C_6 = 680pF ceramic.

C_7 = 150pF ceramic.

C_8 = 100pF ceramic.

C_9 = 10nF polyester.

L_1 = 5 turns of 1mm Cu wire, winding pitch 1.5mm, int. diam. 6mm, Leads: 2×12mm.

L_2 = Ferroxcube choke coil, Z (at 87.5MHz) = 750Ω±20%.

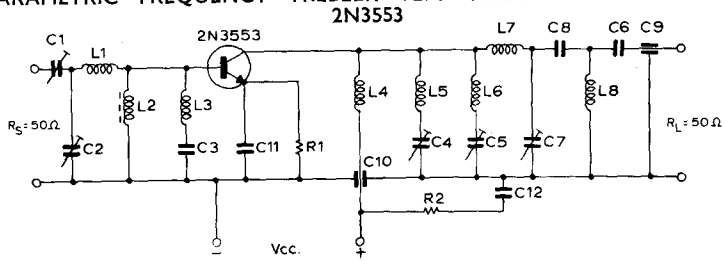
L_3 = 15 turns of 0.7mm closely wound enamelled Cu wire, int. diam. 4mm.

L_4 = 6 turns of 1mm Cu wire, winding pitch 1.5mm, int. diam. 6mm, leads: 2×12mm.

R_1 = 0–50Ω.

R_2 = 10Ω carbon.

PARAMETRIC FREQUENCY TREBLER TEST CIRCUIT 156.7MHz–470MH



*Tuned to second harmonic frequency.

Fig. 5

C_1, C_2, C_3, C_4 } 4–29pF air trimmer.

C_5, C_6, C_7 } 4–10.4pF air trimmer.

C_8 = 1pF ceramic.
C_9 = 12pF ceramic
C_{10} = 100pF ceramic. } feed through.
C_{11} = 1000pF ceramic.
C_{12} = 15nF polyester.
R_1 = 2.2Ω carbon.
R_2 = 10Ω carbon.

L_1 = 35mm straight Cu wire, diam. 1mm, spaced 5.5mm from chassis.

L_2 = Ferroxcube choke coil, Z (at 156,7MHz) = 600Ω ± 20%.

L_3 = 18mm straight Cu wire, diam. 1mm, spaced 5.5mm from chassis.

L_4 = 7 turns of 0.5mm closely wound enamelled Cu wire, int. diam. 3.5mm.

L_5 = 3 turns of 1mm Cu wire, winding pitch 1.7mm, int. diam. 8.5mm, leads: 2 × 10mm.

L_6 = 2 turns of 1mm Cu wire, winding pitch 1.7mm, int. diam. 7mm, leads: 2 × 10mm.

L_7 = 40mm straight Cu wire, diam. 1.5mm spaced 5.5mm from chassis.

L_8 = 1 turn of 1mm Cu wire, int. diam. 7mm, leads: 2 × 5mm.

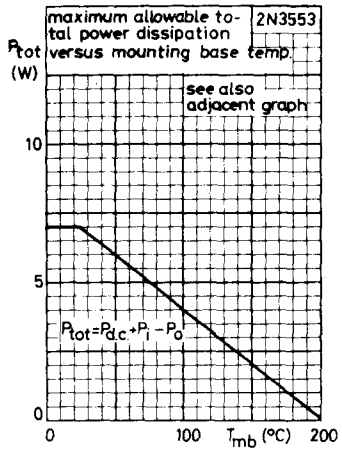
Performance

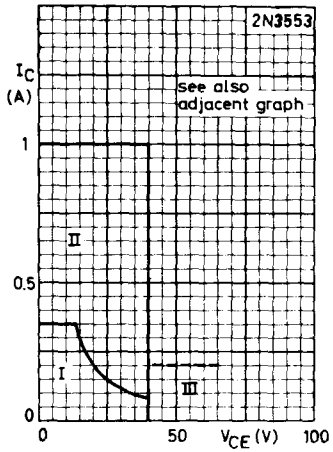
Typical performance at a supply voltage of 28V.

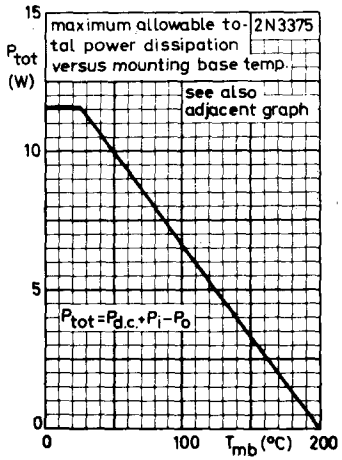
P_o	P_i	G	I_C	η
(W)	(W)	(dB)	(mA)	(%)
1.5	0.27	7.5	125	43
2.0	0.39	7.1	156	46

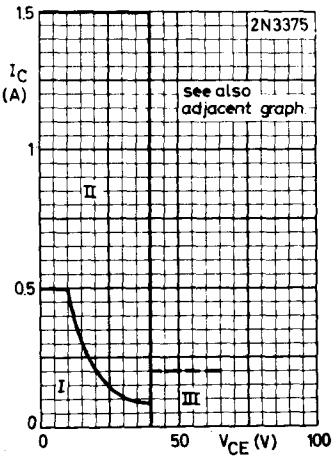
SILICON V.H.F. N-P-N POWER TRANSISTORS

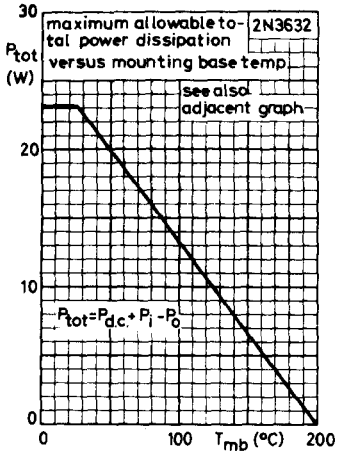
2N3375
2N3553
2N3632

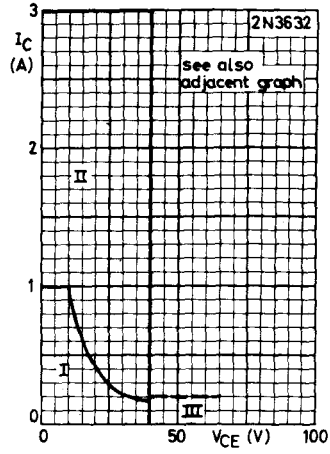










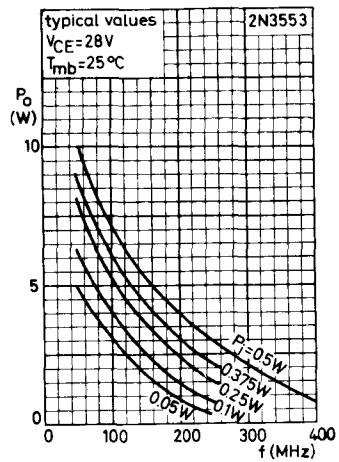


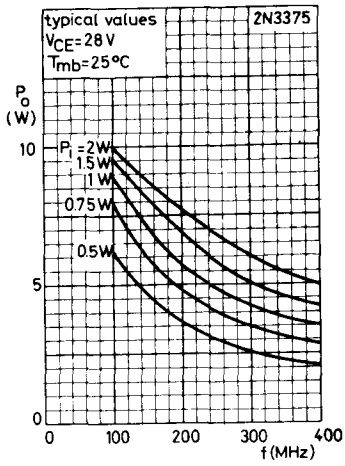
EXPLANATION OF AREAS OF SAFE OPERATION

Region I Operation is allowed under all base-emitter conditions, provided no limiting values are exceeded (d.c. and a.c. operation).

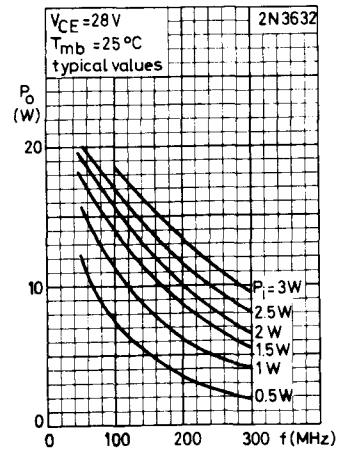
Region II Operating is allowed under all base-emitter conditions with frequencies $\geqslant$ 1MHz, provided no limiting values are exceeded.
Care must be taken to reduce the d.c. adjustment to region I before removing the a.c. signal.
This may be achieved by an appropriate bias in class A, B or C.

Region III Operating during switching-off in this region is allowed, provided the transistor is cut-off with $-V_{BE} \leqslant 1.5V$ and $R_{BE} \geqslant 33\Omega$, $I_C \leqslant 400mA$ and the transient energy does not exceed 2mWs.

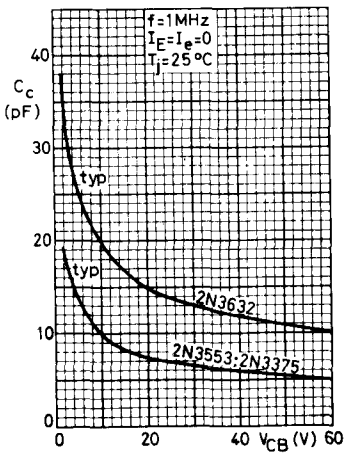




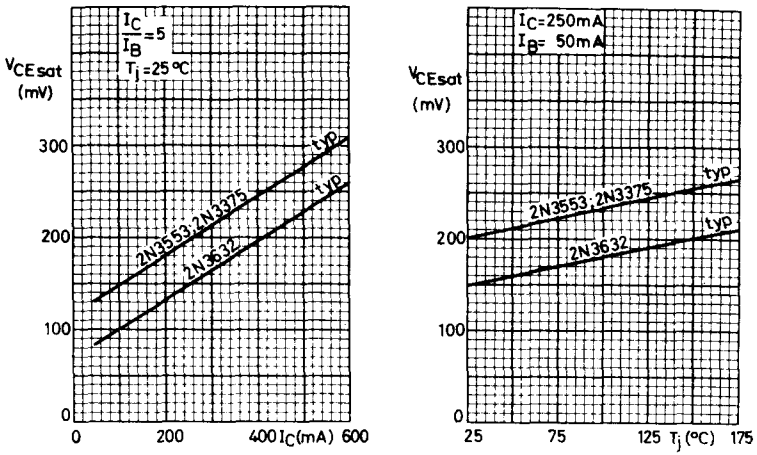
TYPICAL OUTPUT POWER PLOTTED AGAINST FREQUENCY



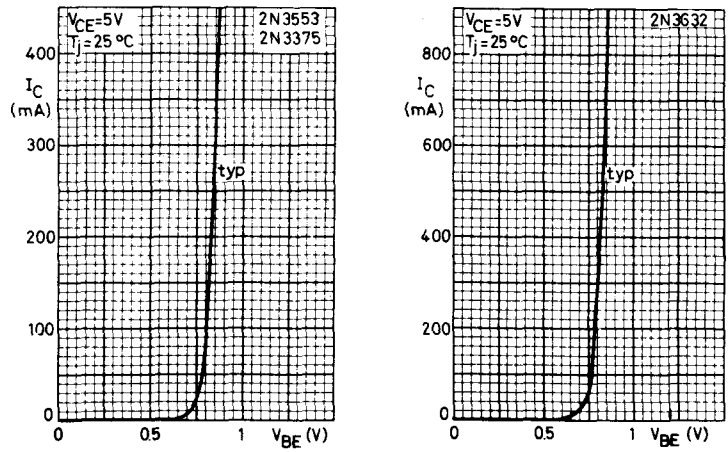
TYPICAL OUTPUT POWER PLOTTED AGAINST FREQUENCY



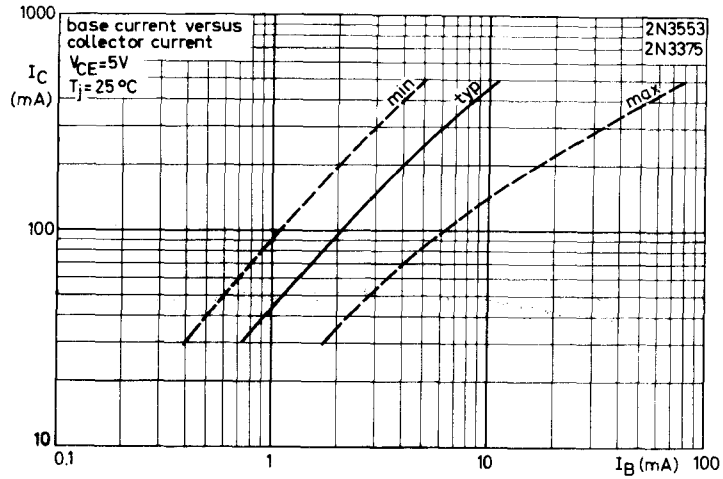
TYPICAL COLLECTOR CAPACITANCE PLOTTED AGAINST COLLECTOR-BASE VOLTAGE

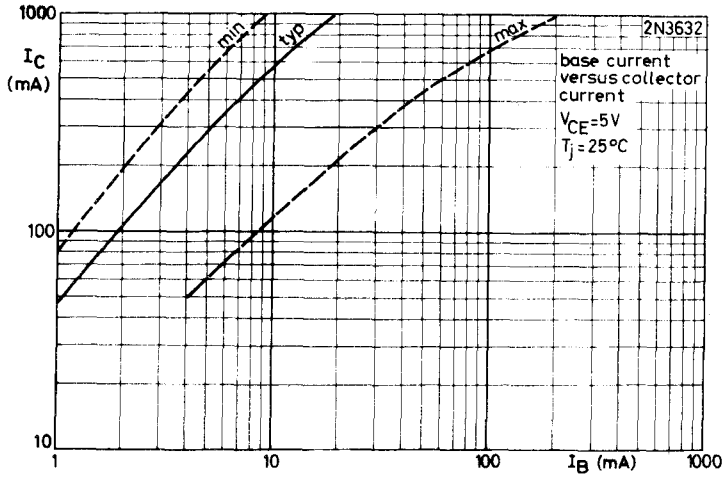


TYPICAL COLLECTOR-EMITTER SATURATION VOLTAGE PLOTTED AGAINST JUNCTION TEMPERATURE

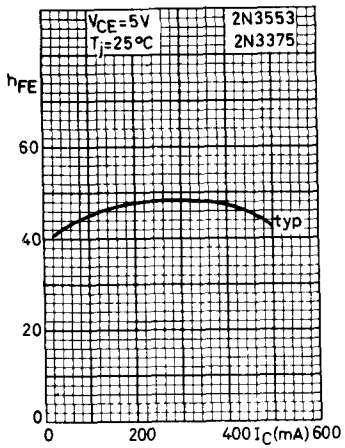


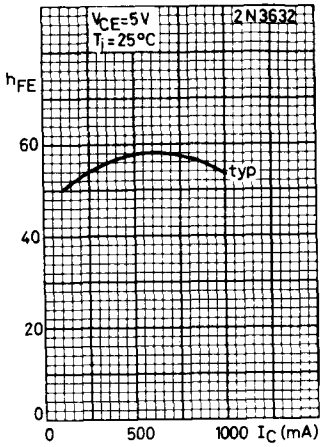
TYPICAL COLLECTOR CURRENT PLOTTED AGAINST BASE-EMITTER VOLTAGE



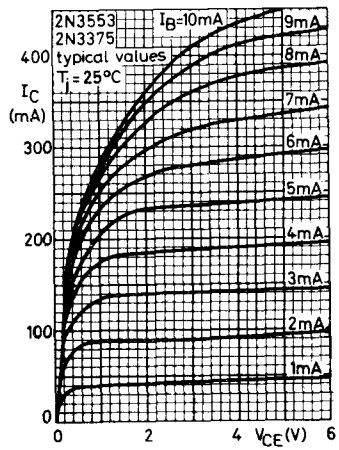


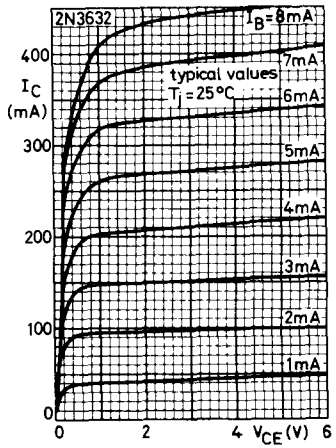
COLLECTOR CURRENT PLOTTED AGAINST BASE CURRENT



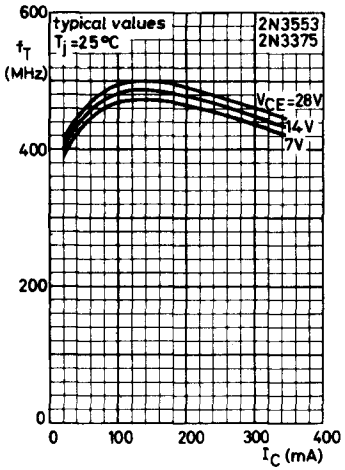


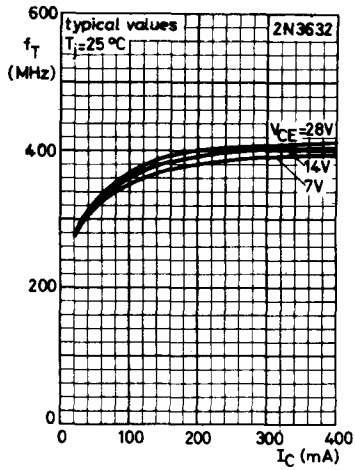
TYPICAL LARGE SIGNAL FORWARD CURRENT TRANSFER RATIO PLOTTED AGAINST COLLECTOR CURRENT



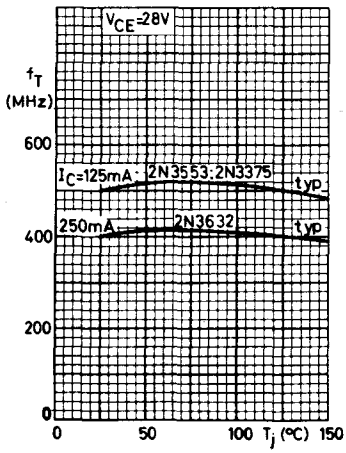


COLLECTOR CURRENT PLOTTED AGAINST COLLECTOR-EMITTER VOLTAGE WITH BASE CURRENT AS A PARAMETER

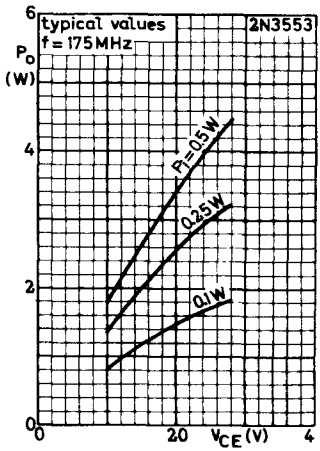




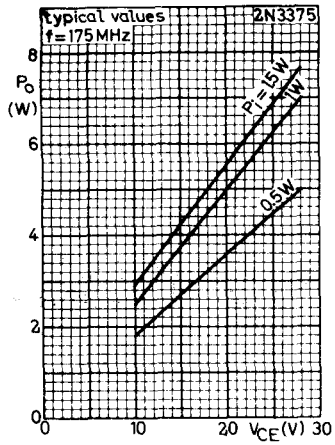
TYPICAL TRANSITION FREQUENCY PLOTTED AGAINST COLLECTOR CURRENT WITH COLLECTOR-EMITTER VOLTAGE AS A PARAMETER

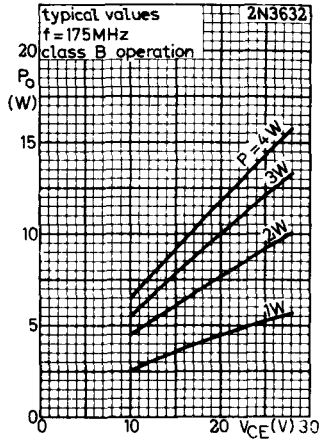


TYPICAL TRANSITION FREQUENCY PLOTTED AGAINST JUNCTION TEMPERATURE

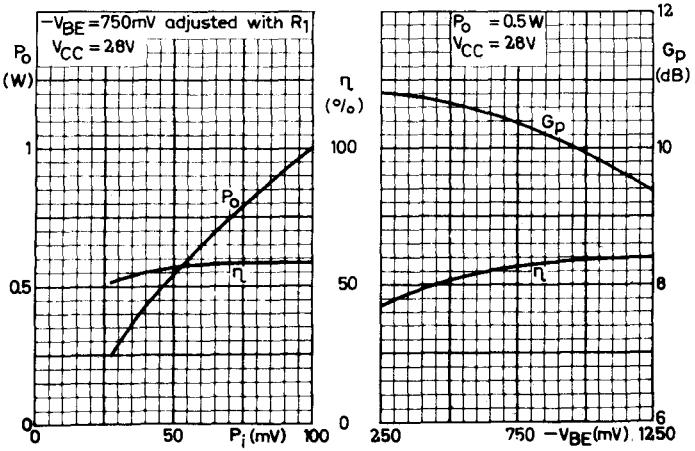


OUTPUT POWER PLOTTED AGAINST COLLECTOR-EMITTER VOLTAGE WITH INPUT POWER AS A PARAMETER





OUTPUT POWER PLOTTED AGAINST COLLECTOR-EMITTER VOLTAGE WITH INPUT POWER AS A PARAMETER



POWER GAIN, POWER OUTPUT, AND EFFICIENCY CURVES PLOTTED AGAINST INPUT POWER AND BASE-EMITTER VOLTAGE FOR DOUBLER CIRCUIT ON PAGE D9

N-P-N SILICON DIFFUSED POWER TRANSISTORS

2N3442
2N4347

N-P-N silicon diffused power transistors intended for use in a wide variety of linear power applications in audio amplifiers, converters, voltage regulators, power supplies, etc.

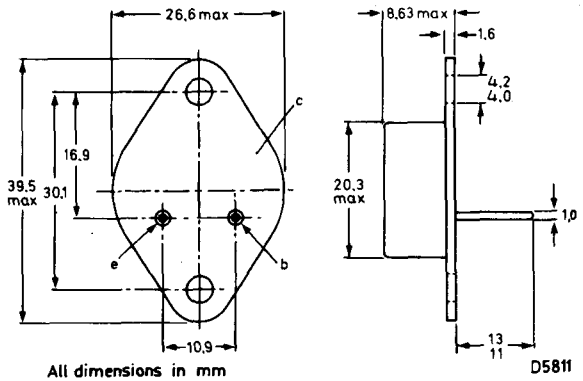
QUICK REFERENCE DATA

	2N3442	2N4347	
V_{CBO} max.	160	140	V
V_{CEO} max.	140	120	V
I_C max.	10	5	A
P_{tot} max. ($T_{mb} \leq 25^oC$)	117	100	W
T_j max.	200	200	^oC
h_{FE} min., I_C=3A, V_{CE}=4V	20-70	-	
I_C=2A, V_{CE}=4V	-	20-70	

Unless otherwise stated data are applicable to both types

OUTLINE AND DIMENSIONS

Conforms to B.S. 3934 SO-5B/SB2-2
J.E.D.E.C. TO-3



Collector connected to envelope

Accessories available: 56239A (insulating bush), 56201B (mica washer), 56214 (lead washer)

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical	2N3442	2N4347	
V_{CBO} max.	160	140	V
V_{CEO} max.	140	120	V
V_{CER} max. (R_{BE} = 100Ω)	150	130	V
V_{EBO} max.	7.0	7.0	V
I_C max.	10	5.0	A
I_{CM} max.	15	10	A
I_B max.	7.0	3.0	A
P_{tot} max. ($T_{mb} \leq 25^oC$)	117	100	W

Temperature		
T_{stg}	-65 to +200	^oC
T_j max.	200	^oC

THERMAL CHARACTERISTICS

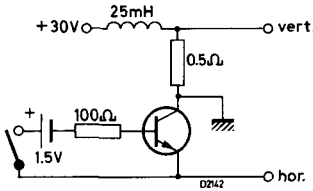
$R_{th(j-mb)}$	Thermal resistance, junction to mounting-base	1.5		1.75	degC/W
$R_{th(mb-h)}$	Thermal resistance, mounting-base to heatsink		0.5		degC/W
$R_{th(mb-h)}$	Thermal resistance, mounting-base to heatsink with accessories 56201, 56214		0.75		degC/W

ELECTRICAL CHARACTERISTICS ($T_j = 25^oC$ unless otherwise stated)

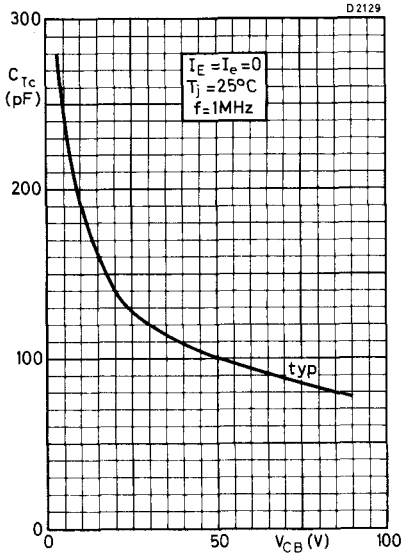
			Min.	Typ.	Max.	
I_{CBO}	Collector-base cut-off current $I_E = 0$, $V_{CB} = 140V$		-	50	1000	μA
I_{CEX}	Collector-emitter cut-off current $-V_{BE} = 1.5V$, $V_{CE} = 140V$	2N3442	-	5.0	1000	μA
	$-V_{BE} = 1.5V$, $V_{CE} = 140V$, $T_{mb} = 150^oC$	2N3442	-	0.1	10	mA
	$-V_{BE} = 1.5V$, $V_{CE} = 120V$	2N3442	-	1.0	-	μA
		2N4347	-	5.0	2000	μA
	$-V_{BE} = 1.5V$, $V_{CE} = 120V$, $T_{mb} = 150^oC$	2N4347	-	0.1	10	mA
I_{EBO}	Emitter cut-off current $I_C = 0$, $V_{EB} = 7V$		-	1.0	5000	μA

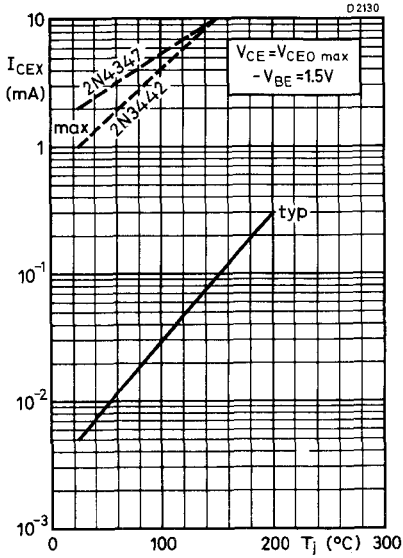
ELECTRICAL CHARACTERISTICS (contd.)

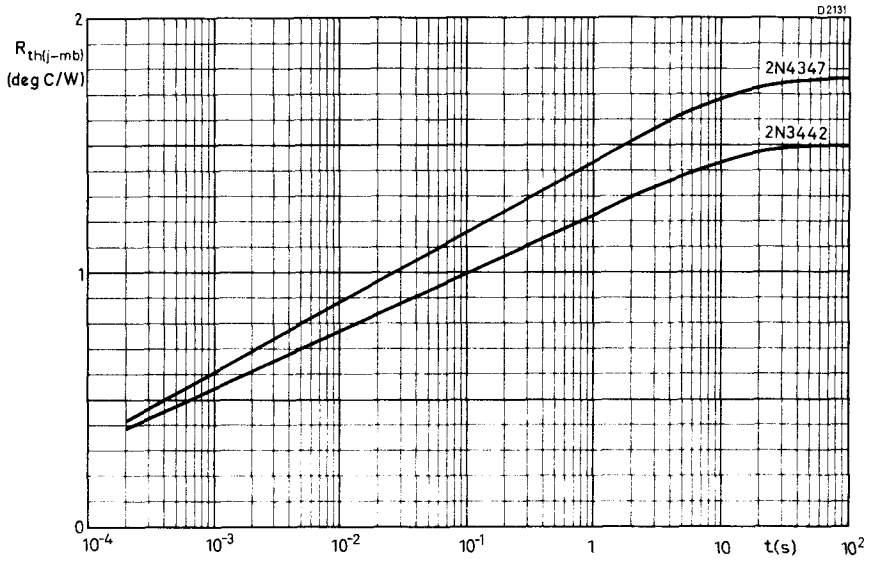
			Min.	Typ.	Max.	
$V_{(BR)CER}$	Collector-emitter breakdown voltage					
	I_C=0.1A, R_{BE}=100Ω	2N3442	150	-	-	V
		2N4347	130	-	-	V
	Collector-emitter sustaining voltage					
$V_{CEO(sust)}$	I_B=0, I_C=0.2 to 3.0A	2N3442	140	-	-	V
		2N4347	120	-	-	V
$V_{CEX(sust)}$	$-V_{BE}$=1.5V, I_C=0.1 to 1.5A	2N3442	160	-	-	V
		2N4347	140	-	-	V

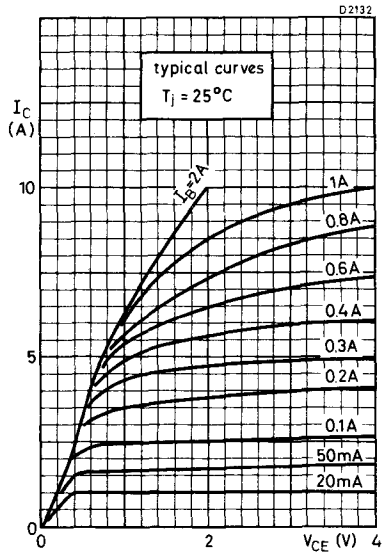


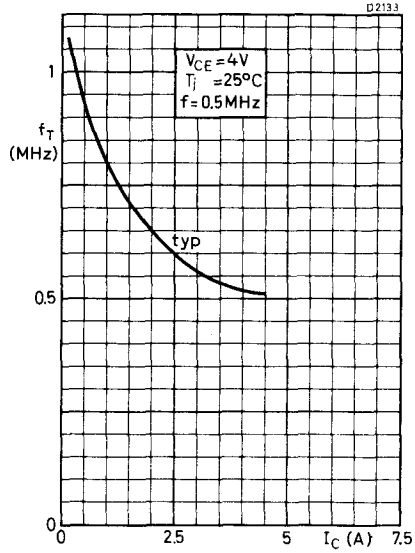
V_{BE}	Base-emitter voltage (t_p=10ms)					
	I_C=2.0A, V_{CE}=4.0V	2N4347	-	0.95	2.0	V
	I_C=3.0A, V_{CE}=4.0V	2N3442	-	1.15	1.7	V
	I_C=5.0A, V_{CE}=4.0V	2N4347	-	1.55	4.0	V
	I_C=10A, V_{CE}=4.0V	2N3442	-	2.8	5.7	V
$V_{CE(sat)}$	Collector-emitter saturation voltage (t_p=10ms)					
	I_C=2.0A, I_B=0.2A	2N4347	-	-	1.0	V
	I_C=3.0A, I_B=0.3A	2N3442	-	-	1.0	V
	I_C=5.0A, I_B=1.0A	2N4347	-	-	5.0	V
	I_C=10A, I_B=2.0A	2N3442	-	-	5.0	V
h_{FE}	Static forward current transfer ratio (t_p=10ms)					
	I_C=2.0A, V_{CE}=4.0V	2N4347	20	35	70	
	I_C=3.0A, V_{CE}=4.0V	2N3442	20	25	70	
	I_C=5.0A, V_{CE}=4.0V	2N4347	7.5	15	-	
	I_C=10A, V_{CE}=4.0V	2N3442	7.5	10	-	
h_{fe}	Small signal current gain					
	I_C=2.0A, V_{CE}=4.0V					
	f=40kHz	2N3442	2.0	9.5	-	
	f=1.0kHz	2N3442	12	18	72	

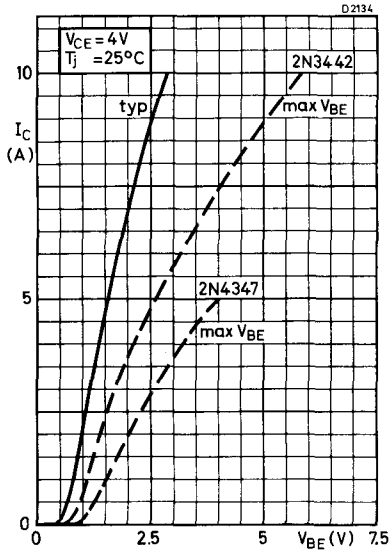

D2129
300
200
100
0
C_{Tc} (pF)
$I_E = I_e = 0$
$T_j = 25°C$
f = 1MHz
typ
0
50
V_{CB} (V)
100

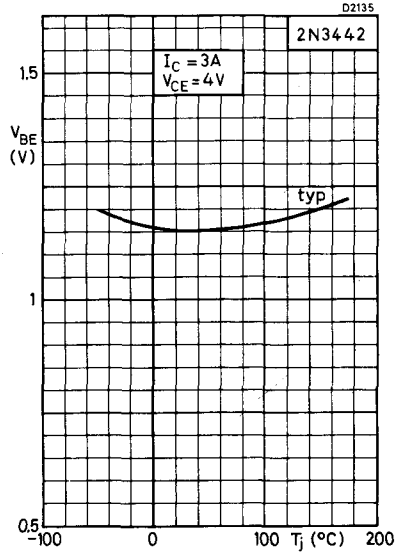

D2130
10
1
10^{-1}
10^{-2}
10^{-3}
I_{CEX} (mA)
$V_{CE} = V_{CEO\ max}$
$-V_{BE} = 1.5V$
2N4347
2N3442
max
typ
0
100
200
T_j (°C)
300

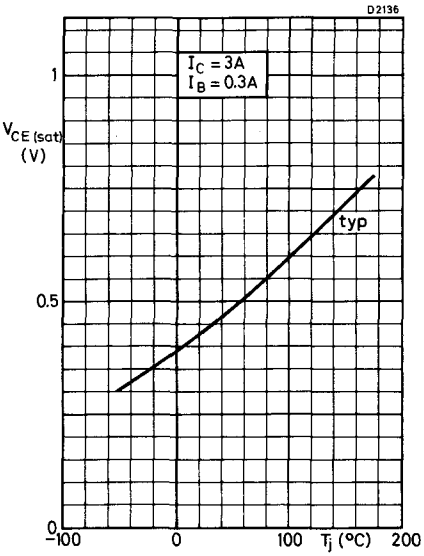

D2131
$R_{th(j-mb)}$
(deg C/W)
2
1
0
2N4347
2N3442
10^{-4}
10^{-3}
10^{-2}
10^{-1}
1
10
t(s)
10^{2}

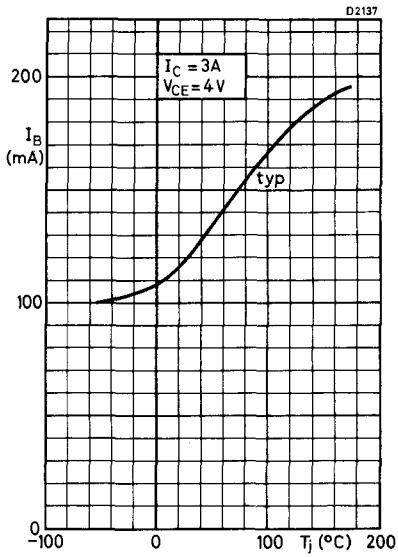

D2132
typical curves
T_j = 25°C
I_C
(A)
10
5
0
I_B=2A
1A
0.8A
0.6A
0.4A
0.3A
0.2A
0.1A
50mA
20mA
0
2
V_{CE} (V)
4

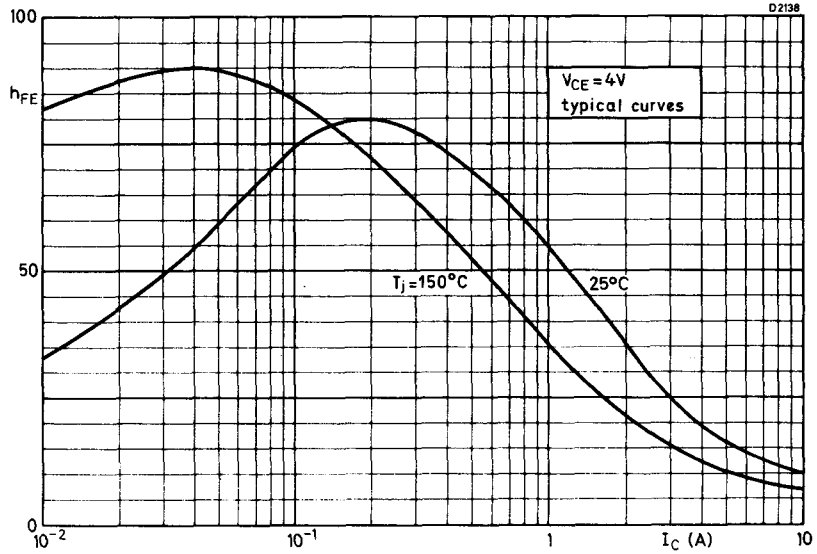

D2133
V_{CE}=4V
T_j =25°C
f=0.5MHz
f_T
(MHz)
1
0.5
0
typ
0
2.5
5
I_C (A)
7.5

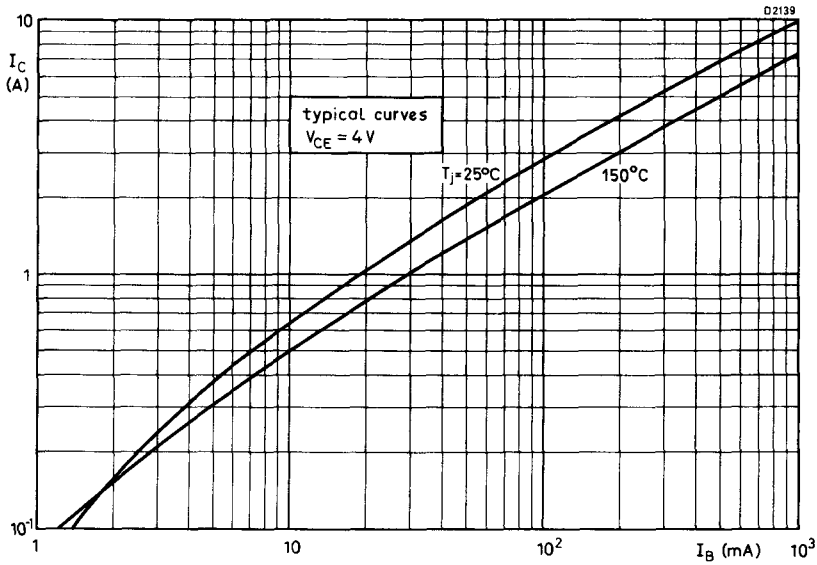

D2134
V_{CE} = 4V
T_j = 25°C
2N3442
typ
max V_{BE}
2N4347
max V_{BE}
I_C (A)
10
5
0
0
2.5
5
V_{BE} (V)
7.5

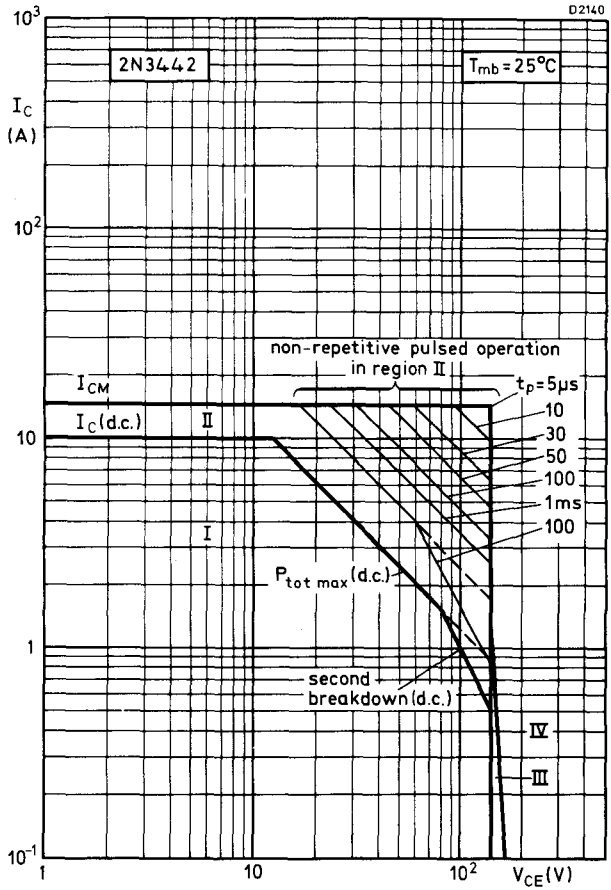

D2135
2N3442
I_C = 3A
V_{CE} = 4V
typ
V_{BE} (V)
1.5
1
0.5
−100
0
100
T_j (°C)
200


D2136
I_C = 3A
I_B = 0.3A
typ
$V_{CE(sat)}$ (V)
1
0.5
0
−100
0
100
T_j (°C)
200


D2137
I_C = 3A
V_{CE} = 4V
typ
I_B (mA)
200
100
0
−100
0
100
T_j (°C)
200


D2138
100
h_{FE}
50
0
10^{-2}
10^{-1}
1
10
I_C (A)
V_{CE} = 4V
typical curves
T_j = 150°C
25°C


D2139
10
I_C
(A)
1
10^{-1}
1
10
10^2
I_B (mA)
10^3
typical curves
V_{CE} = 4 V
T_j = 25°C
150°C

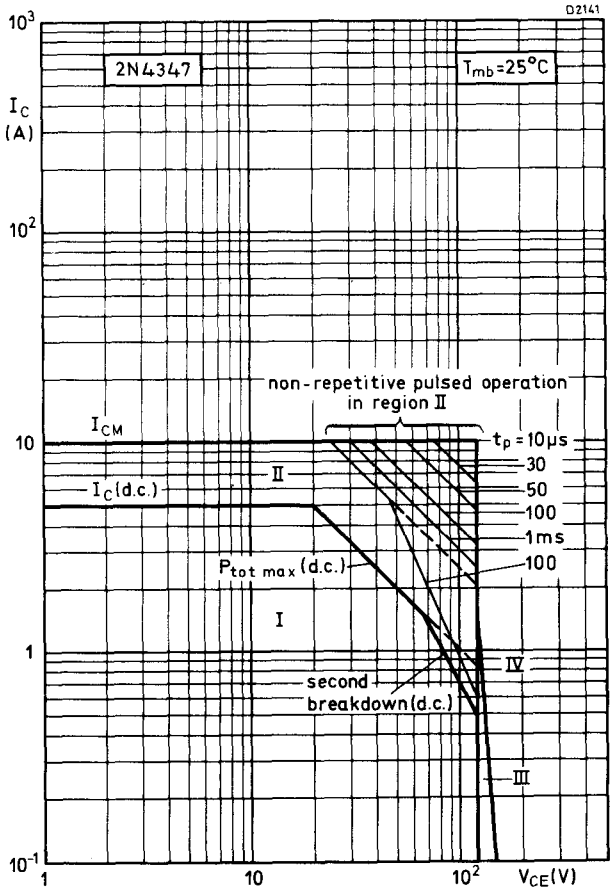


I Region of permissible operation under all base-emitter conditions and at all frequencies, including d.c.

II Permissible extension for repetitive pulsed operation and non-repetitive pulsed operation. For sinusoidal operation care must be taken to reduce the d.c. adjustment to region I before removing the a.c. signal. This may be achieved by an appropriate bias in class A, B or C.

III Operation during switching off in this region is allowed, provided the transistor is cut-off with $-V_{BE} \leq 1.5$; $I_{CM} < 1.5$A.

IV Operation during switching off is allowed provided the transistor is cut-off with $-V_{BE} \leq 1.5$V and the transient energy does not exceed 30mWs.



I Region of permissible operation under all base-emitter conditions and at all frequencies, including d.c.

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III Operation during switching off in this region is allowed, provided the transistor is cut-off with $-V_{BE} \leq 1.5V$; $I_{CM} < 1.5A$.

IV Operation during switching off is allowed provided the transistor is cut-off with $-V_{BE} \leq 1.5V$ and the transient energy does not exceed 30mWs.

N-P-N SILICON V.H.F. POWER TRANSISTORS

2N3553
2N3632

For details see data sheet for type 2N3375

N-CHANNEL SILICON FIELD-EFFECT TRANSISTOR

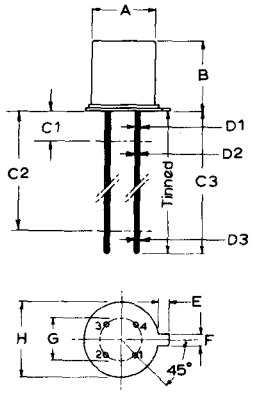
2N3823

N-channel, depletion-type, silicon planar epitaxial field-effect transistor intended for v.h.f. amplifier and mixer applications in industrial service.

QUICK REFERENCE DATA		
V_{DS} max.	30	V
$-V_{GSS}$ max.	30	V
I_{DSS} (V_{DS} = 15V, V_{GS} = 0)	4.0 - 20	mA
P_{tot} max. ($T_{amb} \leq 25^{o}C$)	300	mW
C_{rss} max. (V_{DS} = 15V, V_{GS} = 0, f = 1.0MHz)	2.0	pF
$\|y_{fs}\|$ min. (V_{DS} = 15V, V_{GS} = 0, f = 200MHz)	3.2	mmho
N max. (V_{DS} = 15V, V_{GS} = 0, f = 100MHz, R_G = 1.0kΩ)	2.5	dB

OUTLINE AND DIMENSIONS

Conforms to B.S. 3934 SO-12A/SB4-3
J.E.D.E.C. TO-72



	Millimetres		
	Min.	Nom.	Max.
A	4.53	-	4.8
B	4.66	-	5.33
C1	-	-	0.51
C2	12.7	-	-
C3	12.7	-	15
D1	-	-	1.01
D2	0.41	-	0.48
D3	-	-	0.53
E	0.84	-	1.17
F	0.92	-	1.16
G	-	2.54	-
H	5.31	-	5.84

Viewed from underside

All electrodes are electrically insulated from the case

Connections

1. Source
2. Drain
3. Gate
4. Case

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{DS} max.	30	V
V_{DG} max.	30	V
$-V_{GSS}$ max. ($-I_G = 1.0\mu A$, $V_{DS} = 0$)	30	V
I_G max.	10	mA
P_{tot} max. ($T_{amb} \leq 25^oC$)	300	mW

Temperature

T_{stg} range	-65 to +200	^oC
T_j max.	200	^oC

THERMAL CHARACTERISTICS

$R_{th(j-amb)}$	0.59	degC/mW

ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^oC$ unless otherwise stated)

The fourth lead (case) is connected to the source for all measurements.

		Min.	Max.	
Static				
$-I_{GSS}$	Gate cut-off current $-V_{GS} = 20V$, $V_{DS} = 0$	-	0.5	nA
	$-V_{GS} = 20V$, $V_{DS} = 0$, $T_{amb} = 150^oC$	-	0.5	μA
I_{DSS}	Zero-gate-voltage drain current *$V_{DS} = 15V$, $V_{GS} = 0$	4.0	20	mA
$-V_{(BR)GSS}$	Gate-source breakdown voltage $-I_G = 1.0\mu A$, $V_{DS} = 0$	30	-	V
$-V_{GS}$	Gate-source voltage $V_{DS} = 15V$, $I_D = 400\mu A$	1.0	7.5	V
$-V_{GS(off)}$	Gate-source cut-off voltage $V_{DS} = 15V$, $I_D = 0.5nA$	-	8.0	V

*Pulse measurements, pulse width = 100ms, duty cycle $\leq$ 10%.

ELECTRICAL CHARACTERISTICS (cont'd)

Small signal y-parameters

Common source, V_{DS}=15V, V_{GS}=0

		Min.	Max.	
*f=1.0kHz				
$\|y_{fs}\|$	Transfer admittance	3.5	6.5	mmho
$\|y_{os}\|$	Output admittance	-	35	μmho
f=1.0MHz				
C_{rss}	Feedback capacitance	-	2.0	pF
C_{iss}	Input capacitance	-	6.0	pF
f=200MHz				
$\|y_{fs}\|$	Transfer admittance	3.2	-	mmho
g_{is}	Input conductance	-	800	μmho
g_{os}	Output conductance	-	200	μmho
Noise				
N	Spot noise figure f=100MHz, R_G=1.0kΩ, V_{DS}=15V, V_{GS}=0	-	2.5	dB

*Pulse measurements, pulse width=100ms, duty cycle≤10%.

N-P-N SILICON PLANAR EPITAXIAL U.H.F. TRANSISTOR

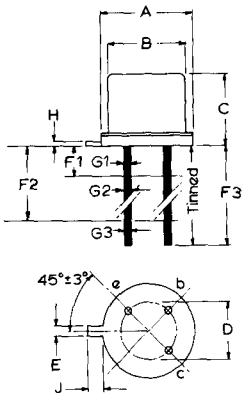
2N3866

N-P-N silicon planar epitaxial transistor primarily intended for use in the output, driver and pre-driver stages of class A, B or C amplifiers, frequency multipliers and oscillators of v.h.f. and u.h.f. equipment.
Encapsulated in a metal TO-39 envelope with the collector connected to the case.

QUICK REFERENCE DATA		
V_{CER} max.	55	V
V_{CEO} max.	30	V
I_C max.	400	mA
P_{tot} max. ($T_{case} \leq 25^oC$)	5.0	W
T_j max.	200	^oC
f_T typ. (I_C = 25mA, V_{CE} = 15V, f = 100MHz)	700	MHz
P_o typ. (P_i < 100mW, V_{CE} = 28V, f = 400MHz)	1.0	W
η min. (P_o = 1.0W, V_{CE} = 28V, f = 400MHz)	45	%

OUTLINE AND DIMENSIONS

Conforms to B.S. 3934 SO-3/SB3-3B
J.E.D.E.C. TO-39



	Millimetres		
	Min.	Typ.	Max.
A	9.10	-	9.40
B	8.2	-	8.5
C	6.15	-	6.60
D	-	5.08	-
E	0.71	-	0.86
F1	-	-	0.51
F2	12.7	-	-
F3	12.7	-	15
G1	-	-	1.01
G2	0.41	-	0.48
G3	-	-	0.53
H	-	0.4	-
J	0.74	-	1.01

Collector connected to case

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{CBO} max.	55	V
V_{CER} max. (R_{BE} = 10Ω)	55	V
V_{CEO} max.	30	V
V_{EBO} max.	3.5	V
I_C max.	400	mA
I_{CM} max.	400	mA
P_{tot} max. ($T_{case} \leq 25^oC$)	5.0	W

Temperature

T_{stg} min.	-65	^oC
T_{stg} max.	200	^oC
T_j max.	200	^oC

THERMAL CHARACTERISTICS

$R_{th(j-amb)}$	In free air	200	degC/W
$R_{th(j-case)}$		35	degC/W
$R_{th(case-h)}$	Mounted with a top clamping washer of accessory 56218	1.0	degC/W
$R_{th(case-h)}$	Mounted with a top clampling washer of accessory 56218 and a boron nitride washer for electrical insulation	1.2	degC/W

ELECTRICAL CHARACTERISTICS ($T_j = 25^oC$ unless otherwise stated)

		Min.	Typ.	Max.	
I_{CEO}	Collector cut-off current V_{CE} = 28V, I_B = 0	-	-	20	μA
$V_{(BR)CBO}$	Collector-base breakdown voltage I_C = 100μA, I_E = 0	55	-	-	V
	Collector-emitter breakdown voltages				
$V_{(BR)CER}$	I_C = 5.0mA, R_{BE} = 10Ω	55	-	-	V
$V_{(BR)CEO}$	I_C = 5.0mA, I_B = 0	30	-	-	V
$V_{(BR)EBO}$	Collector-base breakdown voltage I_E = 100μA, I_C = 0	3.5	-	-	V

ELECTRICAL CHARACTERISTICS (cont'd)

		Min.	Typ.	Max.	
$V_{CE(sat)}$	Collector-emitter saturation voltage $I_C = 100mA$, $I_B = 20mA$	-	-	1.0	V
h_{FE}	Static forward current transfer ratio $I_C = 50mA$, $V_{CE} = 5.0V$	10	-	200	
	$I_C = 360mA$, $V_{CE} = 5.0V$	5	-	-	
f_T	Transition frequency $I_C = 25mA$, $V_{CE} = 15V$, $f = 100MHz$	-	700	-	MHz
C_{tc}	Collector capacitance $V_{CB} = 28V$, $I_E = I_e = 0$, $f = 1.0MHz$	-	-	3.0	pF

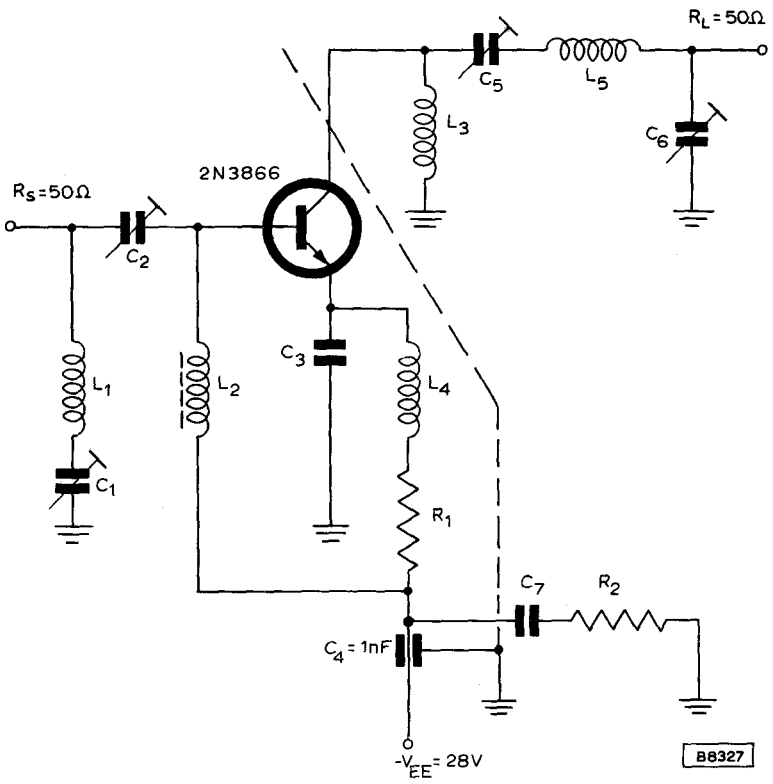
Typical r.f. performance

$V_{CE} = 28V$, $T_{case} = 25^oC$

f	Frequency	100	250	400*	MHz
P_i	Input power	50	100	<100	mW
I_C	Collector current	<107	<107	<79	mA
P_o	Output power	1.8	1.5	1.0	W
η	Efficiency	>60	>50	>45	%

*The transistor can withstand a load mismatch having a v.s.w.r. of 3, varied through all phases for conditions as given above (see also test circuit)

Common emitter test circuit (f = 400MHz)



Components

C_1, C_2, C_5 = 4 to 29pF air trimmers

C_3 = 12pF

C_6 = 4 to 14pF air trimmer

C_7 = 12nF

R_1 = 5.6Ω

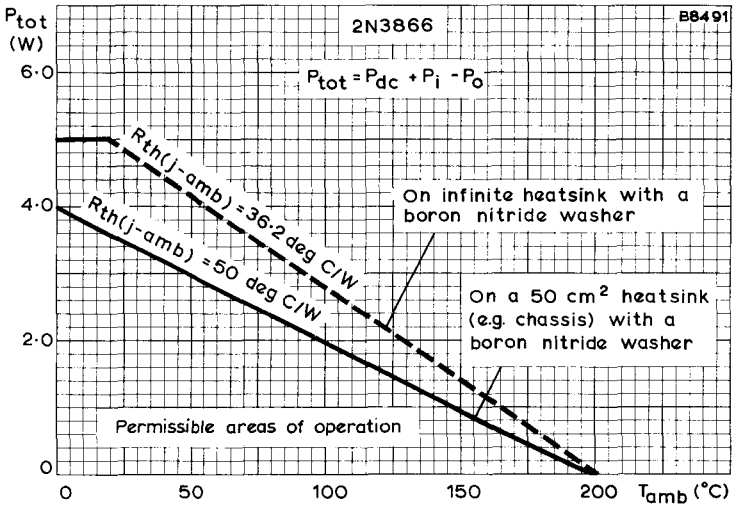
R_2 = 10Ω

L_1 = 2 turns of 1mm Cu wire, int. dia. 6mm, winding pitch 3mm

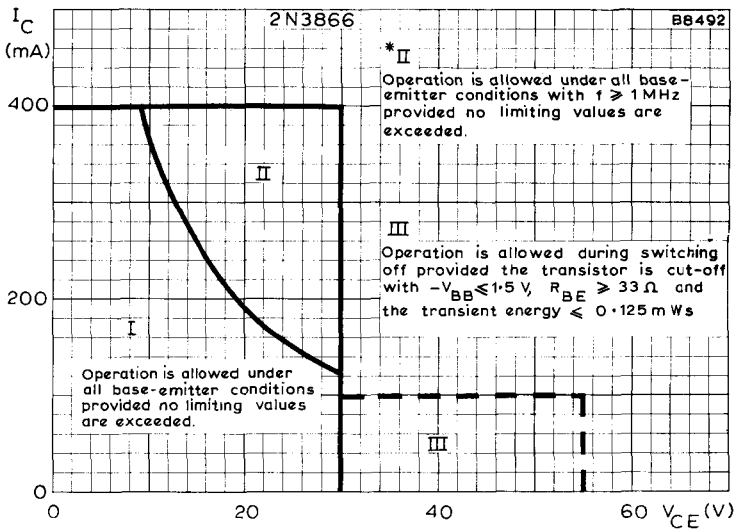
L_2 = ferroxcube choke coil (Z = 450Ω at 250MHz)

L_3, L_4 = 6 turns of 0.5mm en. Cu wire, int. dia. 3.5mm (100nH)

L_5 = 2 turns of 1mm Cu wire, int. dia. 7mm, winding pitch 2.5mm, leads 2 × 15mm

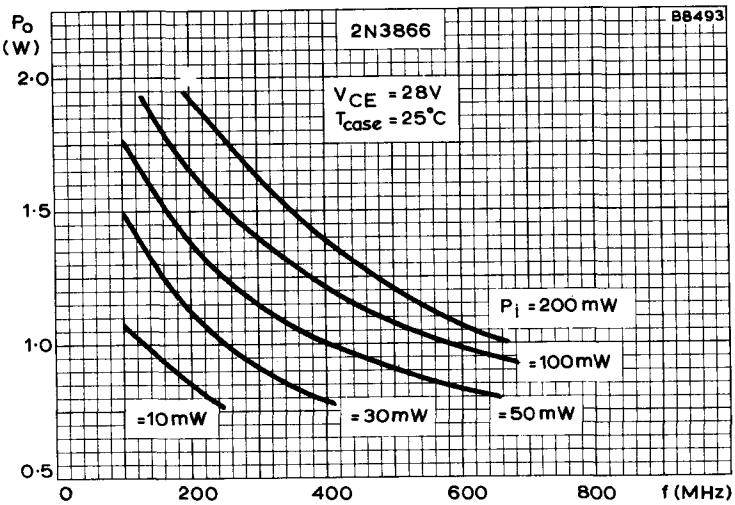


MAXIMUM TOTAL DISSIPATION PLOTTED AGAINST AMBIENT TEMPERATURE

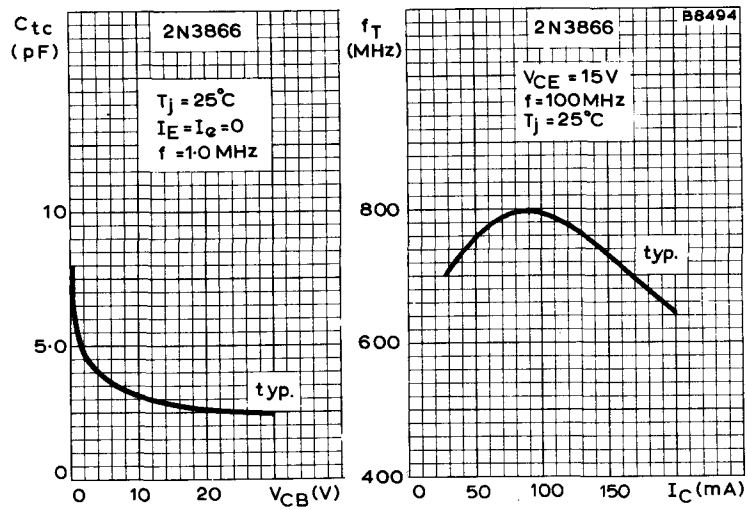


AREAS OF SAFE OPERATION

*II Care must be taken to reduce the steady state current to region I before removing the a.c. signal. This may be achieved by appropriate bias in class A, B or C.



TYPICAL VARIATION OF OUTPUT POWER WITH FREQUENCY AND INPUT POWER



Collector capacitance versus collector-base voltage

Transition frequency versus collector current

N-CHANNEL SILICON FIELD-EFFECT TRANSISTOR

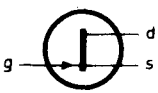
2N3966

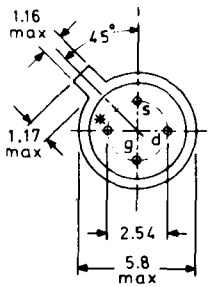
Silicon n-channel planar epitaxial junction field-effect transistor intended for low power switching applications, e.g., in multiplexing systems.

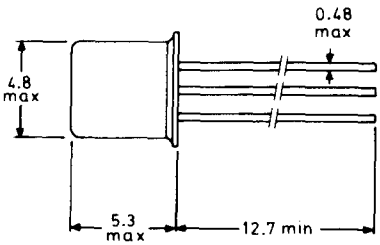
QUICK REFERENCE DATA			
$\pm V_{DS}$ max.	Drain-source voltage	30	V
$-V_{GSO}$ max.	Gate-source voltage	30	V
P_{tot} max.	Total power dissipation ($T_{amb} \leq 25^{o}C$)	300	mW
I_{DSS} min.	Drain current ($V_{DS}=20V$, $V_{GS}=0$)	2.0	mA
$-V_{(P)GS}$	Gate-source cut-off voltage ($I_D=10nA$, $V_{DS}=10V$)	4 to 6	V
$-C_{rs}$ max.	Feedback capacitance ($V_{DS}=0$, $V_{GS}=7V$, $f=1MHz$)	1.5	pF
$r_{DS(on)}$ max.	Drain-source 'on' resistance ($V_{GS}=0$, $I_D=0$, $f=1kHz$)	220	Ω

OUTLINE AND DIMENSIONS

Conforms to B.S.3934 SO-12A/SB4-3
J.E.D.E.C. TO-72
} Insulated electrodes







All dimensions in mm

D2967

*shield lead (connected to case)

Accessories available: 56246, 56263

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

$\pm V_{DS}$ max.	Drain-source voltage	30	V
V_{DGO} max.	Drain-gate voltage (open source)	30	V
$-V_{GSO}$ max.	Gate-source voltage (open drain)	30	V
I_G max.	Gate current	10	mA
P_{tot} max.	Total power dissipation ($T_{amb} \leq 25^oC$)	300	mW

Temperature

T_{stg}	Storage temperature	-55 to +200	^oC
T_j max.	Junction temperature	200	^oC

THERMAL CHARACTERISTIC

$R_{th(j-amb)}$	Thermal resistance from junction to ambient	0.59	$^oC/mW$

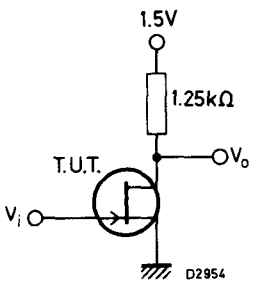
ELECTRICAL CHARACTERISTICS ($T_j = 25^oC$ unless otherwise stated)

		Min.	Max.	
$-I_{GSS}$	Gate cut-off current $-V_{GS} = 20V$, $V_{DS} = 0$	-	0.1	nA
I_{DGO}	Drain current $V_{DG} = 20V$, $I_S = 0$	-	0.1	nA
	$V_{DG} = 20V$, $I_S = 0$, $T_{amb} = 150^oC$	-	0.2	μA
I_{DSS}	Drain current $V_{DS} = 20V$, $V_{GS} = 0$	2.0	-	mA
$-V_{(BR)GS}$	Gate-source breakdown voltage $-I_G = 1.0\mu A$, $V_{DS} = 0$	30	-	V
$-V_{(P)GS}$	Gate-source voltage $I_D = 10nA$, $V_{DS} = 10V$	4.0	6.0	V
V_{DS}	Drain-source voltage $I_D = 1.0mA$, $V_{GS} = 0$	-	0.25	V

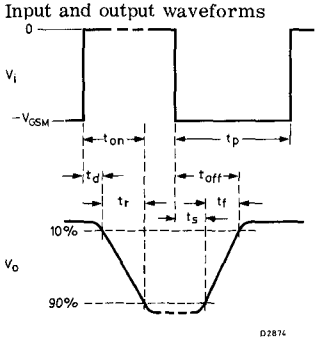
ELECTRICAL CHARACTERISTICS (contd.)

		Min.	Max.	
I_D	Drain cut-off current V_{DS} = 10V, $-V_{GS}$ = 7V	-	1.0	nA
	V_{DS} = 10V, $-V_{GS}$ = 7V, T_{amb} = 150°C	-	2.0	μA
$r_{DS(on)}$	Drain-source 'on' resistance V_{GS} = 0, I_D = 0, f = 1kHz	-	220	Ω
C_{is}	Input capacitance V_{DS} = 20V, V_{GS} = 0, f = 1MHz	-	6.0	pF
$-C_{rs}$	Feedback capacitance V_{DS} = 0, V_{GS} = 7V, f = 1MHz	-	1.5	pF
Switching times				
	V_{DD} = 1.5V, $I_{D(on)}$ = 1.0mA $V_{GS(on)}$ = 0, $-V_{GS(off)}$ = 6.0V			
t_d	Delay time	-	20	ns
t_r	Rise time	-	100	ns
t_{off}	Turn-off time	-	100	ns

Test circuit



Input and output waveforms



Pulse generator:

t_r < 1.0 ns
t_f < 1.0 ns
t_p = 1.0 μs
d < 0.5
R_S = 50 Ω

Oscilloscope:

t_r < 10 ns
R_i > 5 MΩ
C_i < 10 pF

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

2N4091
2N4092
2N4093

Silicon n-channel, depletion type, junction field-effect transistors intended for low power switching applications.

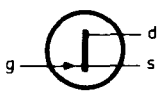
QUICK REFERENCE DATA

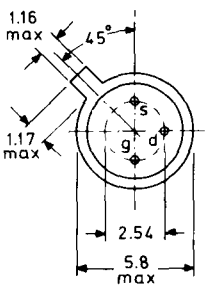
		2N4091	2N4092	2N4093	
$\pm V_{DS}$ max.	Drain-source voltage	40	40	40	V
P_{tot} max.	Total power dissipation ($T_{case} \leq 25^{\circ}C$)	1.8	1.8	1.8	W
I_{DSS} min.	Drain current ($V_{DS} = 20V$, $V_{GS} = 0$)	30	15	8.0	mA
$-V_{(P)GS}$	Gate-source cut-off voltage ($I_D = 1nA$, $V_{DS} = 20V$)	5 to 10	2 to 7	1 to 5	V
$r_{DS(on)}$ max.	Drain-source 'on' resistance ($I_D = 0$, $V_{GS} = 0$, f = 1kHz)	30	50	80	Ω
$-C_{rs}$ max.	Feedback capacitance ($V_{DS} = 0$, $-V_{GS} = 20V$, f = 1MHz)	5.0	5.0	5.0	pF
t_{off} max.	Turn-off time ($V_{GS} = 0$, $V_{DD} = 3V$)				
	($I_D = 6.6mA$, $-V_{GSM} = 12V$)	40	-	-	ns
	($I_D = 4.0mA$, $-V_{GSM} = 8V$)	-	60	-	ns
	($I_D = 2.5mA$, $-V_{GSM} = 6V$)	-	-	80	ns

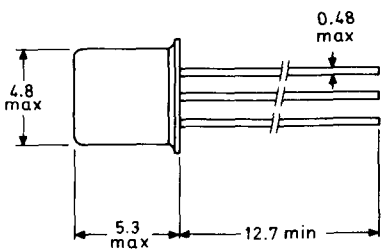
Unless otherwise stated data are applicable to all types

OUTLINE AND DIMENSIONS

Conforms to BS 3934 SO-12A/SB3-6A
J.E.D.E.C. TO-18
} Gate connected to case







All dimensions in mm

D2872

Accessories supplied on request: 56246, 56263

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

$\pm V_{DS}$ max.	Drain-source voltage	40	V
V_{DGO} max.	Drain-gate voltage (open source)	40	V
$-V_{GSO}$ max.	Gate-source voltage (open drain)	40	V
I_G max.	Forward gate current (d.c.)	10	mA
P_{tot} max.	Total power dissipation ($T_{case} \leq 25^oC$)	1.8	W

Temperature

T_{stg}	Storage temperature	-65 to +200	^oC
T_j max.	Junction temperature	200	^oC

THERMAL CHARACTERISTIC

$R_{th(j-c)}$	Thermal resistance from junction to case in free air	0.1	$^oC/mW$

ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^oC$ unless otherwise stated)

			Min.	Typ.	Max.
I_{DGO}	Drain current				
	$V_{DG} = 20V$, $I_S = 0$		-	-	0.2 nA
	$V_{DG} = 20V$, $I_S = 0$, $T_{amb} = 150^oC$		-	-	0.4 μA
I_{SGO}	Source current				
	$V_{SG} = 20V$, $I_D = 0$		-	-	0.2 nA
I_D	Drain cut-off current				
	$V_{DS} = 20V$, $-V_{GS} = 12V$	2N4091	-	-	0.2 nA
	$V_{DS} = 20V$, $-V_{GS} = 8V$	2N4092	-	-	0.2 nA
	$V_{DS} = 20V$, $-V_{GS} = 6V$	2N4093	-	-	0.2 nA
	$V_{DS} = 20V$, $-V_{GS} = 12V$, $T_{amb} = 150^oC$	2N4091	-	-	0.4 μA
	$V_{DS} = 20V$, $-V_{GS} = 8V$, $T_{amb} = 150^oC$	2N4092	-	-	0.4 μA
	$V_{DS} = 20V$, $-V_{GS} = 6V$, $T_{amb} = 150^oC$	2N4093	-	-	0.4 μA

ELECTRICAL CHARACTERISTICS (contd.)

			Min.	Typ.	Max.	
$-V_{(BR)GSS}$	Gate-source breakdown voltage $-I_G = 1.0\mu A$, $V_{DS} = 0$		40	-	-	V
I_{DSS}	Drain current (measured under pulsed conditions, $t_p \leq 300\mu s$, $d \leq 0.03$) $V_{DS} = 20V$, $V_{GS} = 0$	2N4091	30	-	-	mA
		2N4092	15	-	-	mA
		2N4093	8.0	-	-	mA
$-V_{GS}$	Gate-source voltage $I_D = 1mA$, $V_{DS} = 20V$	2N4091	5.0	-	10	V
		2N4092	2.0	-	7.0	V
		2N4093	1.0	-	5.0	V
$V_{DS(on)}$	Drain-source 'on' voltage $I_D = 6.6mA$, $V_{GS} = 0$	2N4091	-	-	0.2	V
	$I_D = 4.0mA$, $V_{GS} = 0$	2N4092	-	-	0.2	V
	$I_D = 2.5mA$, $V_{GS} = 0$	2N4093	-	-	0.2	V
$r_{DS(on)}$	Drain-source 'on' resistance $I_D = 1mA$, $V_{GS} = 0$	2N4091	-	-	30	Ω
		2N4092	-	-	50	Ω
		2N4093	-	-	80	Ω
	$I_D = 0$, $V_{GS} = 0$, $f = 1kHz$	2N4091	-	-	30	Ω
		2N4092	-	-	50	Ω
		2N4093	-	-	80	Ω
y-parameters (common source) $V_{DS} = 20V$, $V_{GS} = 0$, $f = 1MHz$						
C_{is}	Input capacitance		-	-	16	pF
$-C_{rs}$	Feedback capacitance		-	-	5.0	pF

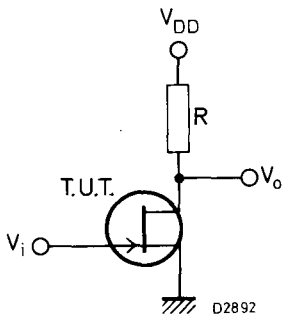
ELECTRICAL CHARACTERISTICS (contd.)

Switching times

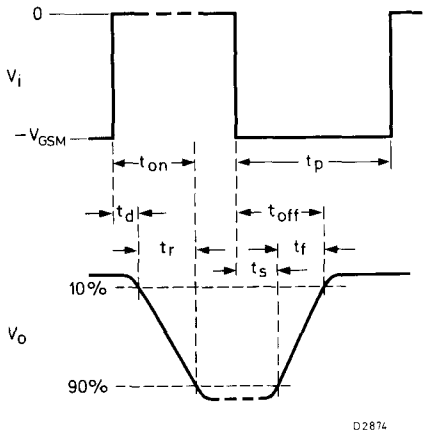
$V_{DD} = 3.0V$, $V_{GS} = 0$

			2N4091	2N4092	2N4093	
		I_D =	6.6	4.0	2.5	mA
		$-V_{GSM}$ =	12	8.0	6.0	V
t_d	Delay time	max.	15	15	20	ns
t_r	Rise time	max.	10	20	40	ns
t_{off}	Turn-off time	max.	40	60	80	ns

Test circuit



Input and output waveforms



$$R = \frac{2.8}{I_D}\ \Omega$$

Pulse generator:

$t_r < 1ns$

$t_f < 1ns$

$t_p = 1\mu s$

$d = 0.1$

$R_S = 50\Omega$

Oscilloscope:

$t_r < 0.4ns$

$R_i > 9.8M\Omega$

$Z_i < 1.7pF$

N-P-N SILICON DIFFUSED POWER TRANSISTOR

2N4347

For details see data sheet for type 2N3442

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

2N4391
2N4392
2N4393

Silicon n-channel, depletion type, junction field-effect transistors intended for low power chopper or switching applications.

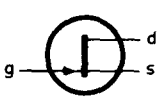
QUICK REFERENCE DATA

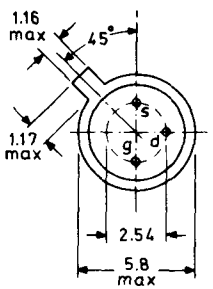
		2N4391	2N4392	2N4393	
$\pm V_{DS}$ max.	Drain-source voltage	40	40	40	V
P_{tot} max.	Total power dissipation ($T_{case} \leq 25^{o}C$)	1.8	1.8	1.8	W
I_{DSS} min.	Drain current ($V_{DS}=20V$, $V_{GS}=0$)	50	25	5.0	mA
$-V_{(P)GS}$	Gate-source cut-off voltage ($I_D=1nA$, $V_{DS}=20V$)	4 to 10	2 to 5	0.5 to 3	V
$r_{DS(on)}$ max.	Drain-source 'on' resistance ($I_D=0$, $V_{GS}=0$, $f=1kHz$)	30	60	100	Ω
$-C_{rs}$ max.	Feedback capacitance ($V_{DS}=0$, $-V_{GS}=12V$, $f=1MHz$)	3.5	-	-	pF
	($V_{DS}=0$, $-V_{GS}=7V$, $f=1MHz$)	-	3.5	-	pF
	($V_{DS}=0$, $-V_{GS}=5V$, $f=1MHz$)	-	-	3.5	pF
t_{off} max.	Turn-off time ($V_{GS}=0$, $V_{DD}=10V$)				
	($I_D=12mA$, $-V_{GSM}=12V$)	20	-	-	ns
	($I_D=6mA$, $-V_{GSM}=7V$)	-	35	-	ns
	($I_D=3mA$, $-V_{GSM}=5V$)	-	-	50	ns

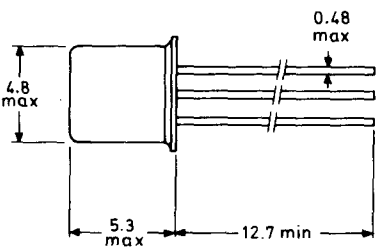
Unless otherwise stated data are applicable to all types

OUTLINE AND DIMENSIONS

Conforms to BS 3934 SO-12A/SB3-6A
J.E.D.E.C. TO-18
} Gate connected to case







All dimensions in mm

D2872

Accessories supplied on request: 56246, 56263

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

$\pm V_{DS}$ max.	Drain-source voltage	40	V
V_{DGO} max.	Drain-gate voltage (open source)	40	V
$-V_{GSO}$ max.	Gate-source voltage (open drain)	40	V
I_G max.	Gate current	50	mA
P_{tot} max.	Total power dissipation ($T_{case} \leq 25^oC$)	1.8	W

Temperature

T_{stg}	Storage temperature	-65 to +200	^oC
T_j max.	Junction temperature	200	^oC

THERMAL CHARACTERISTIC

$R_{th(j-c)}$	Thermal resistance from junction to case in free air	0.1	$^oC/mW$

ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^oC$ unless otherwise stated)

			Min.	Typ.	Max.	
$-I_{GSS}$	Gate cut-off current					
	$-V_{GS} = 20V$, $V_{DS} = 0$		-	-	0.1	nA
	$-V_{GS} = 20V$, $V_{DS} = 0$, $T_{amb} = 150^oC$		-	-	0.2	μA
I_{DSX}	Drain cut-off current					
	$V_{DS} = 20V$, $-V_{GS} = 12V$	2N4391	-	-	0.1	nA
	$V_{DS} = 20V$, $-V_{GS} = 7V$	2N4392	-	-	0.1	nA
	$V_{DS} = 20V$, $-V_{GS} = 5V$	2N4393	-	-	0.1	nA
	$V_{DS} = 20V$, $-V_{GS} = 12V$, $T_{amb} = 150^oC$	2N4391	-	-	0.2	μA
	$V_{DS} = 20V$, $-V_{GS} = 7V$, $T_{amb} = 150^oC$	2N4392	-	-	0.2	μA
	$V_{DS} = 20V$, $-V_{GS} = 5V$, $T_{amb} = 150^oC$	2N4393	-	-	0.2	μA
I_{DSS}	Drain current (pulse measurement, $t_p = 100\mu s$, $d = 0.01$)					
	$V_{DS} = 20V$, $V_{GS} = 0$	2N4391	50	-	150	mA
	$V_{DS} = 20V$, $V_{GS} = 0$	2N4392	25	-	75	mA
	$V_{DS} = 20V$, $V_{GS} = 0$	2N4393	5.0	-	30	mA

ELECTRICAL CHARACTERISTICS (contd.)

			Min.	Typ.	Max.	
$-V_{(BR)GSS}$	Gate-source breakdown voltage $-I_G = 1\mu A$, $V_{DS} = 0$		40	-	-	V
$V_{GS(on)}$	Gate-source 'on' voltage $I_G = 1mA$, $V_{DS} = 0$		-	-	1.0	V
$-V_{(P)GS}$	Gate-source cut-off voltage $I_D = 1nA$, $V_{DS} = 0$	2N4391	4.0	-	10	V
		2N4392	2.0	-	5.0	V
		2N4393	0.5	-	3.0	V
$V_{DS(on)}$	Drain-source 'on' voltage $I_D = 12mA$, $V_{GS} = 0$	2N4391	-	-	0.4	V
	$I_D = 6mA$, $V_{GS} = 0$	2N4392	-	-	0.4	V
	$I_D = 3mA$, $V_{GS} = 0$	2N4393	-	-	0.4	V
$r_{DS(on)}$	Drain-source 'on' resistance $I_D = 1mA$, $V_{GS} = 0$	2N4391	-	-	30	Ω
		2N4392	-	-	60	Ω
		2N4393	-	-	100	Ω
	$I_D = 0$, $V_{GS} = 0$, $f = 1kHz$	2N4391	-	-	30	Ω
		2N4392	-	-	60	Ω
		2N4393	-	-	100	Ω
y-parameters (common source)						
C_{is}	Input capacitance $V_{DS} = 20V$, $V_{GS} = 0$, $f = 1MHz$		-	-	14	pF
$-C_{rs}$	Feedback capacitance $-V_{GS} = 12V$, $V_{DS} = 0$, $f = 1MHz$	2N4391	-	-	3.5	pF
	$-V_{GS} = 7V$, $V_{DS} = 0$, $f = 1MHz$	2N4392	-	-	3.5	pF
	$-V_{GS} = 5V$, $V_{DS} = 0$, $f = 1MHz$	2N4393	-	-	3.5	pF

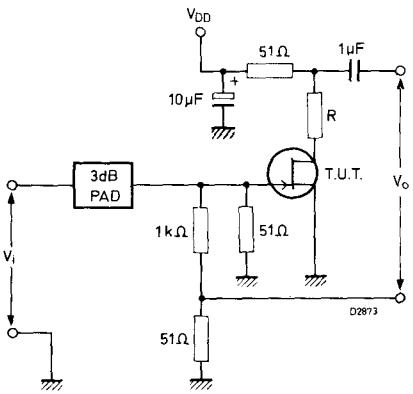
ELECTRICAL CHARACTERISTICS (contd.)

Switching times

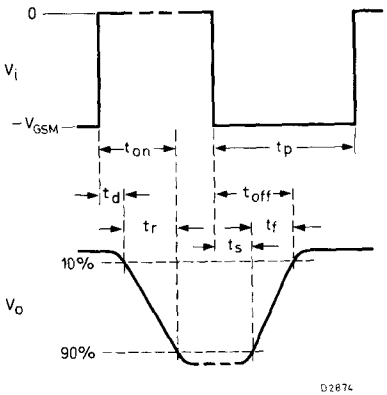
$V_{DD} = 10V$, $V_{GS} = 0$

			2N4391	2N4392	2N4393	
		I_D =	12	6.0	3.0	mA
		$-V_{GSM}$ =	12	7.0	5.0	V
t_r	Rise time	max.	5.0	5.0	5.0	ns
t_{on}	Turn-on time	max.	15	15	15	ns
t_f	Fall time	max.	15	20	30	ns
t_{off}	Turn-off time	max.	20	35	50	ns

Test circuit



Input and output waveforms



$$R = \frac{9.6}{I_D} - 51\Omega$$

Pulse generator:

$t_r < 0.5ns$

$t_f < 0.5ns$

$t_p = 100\mu s$

$d = 0.01$

Oscilloscope:

$R_i = 50\Omega$

N-P-N SILICON PLANAR EPITAXIAL U.H.F. TRANSISTOR

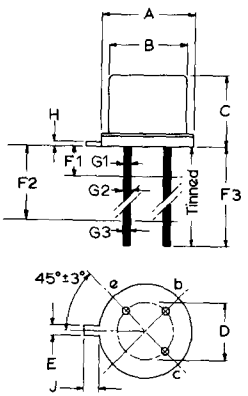
2N4427

N-P-N silicon planar epitaxial transistor primarily intended for use in the output, driver and pre-driver stages of class A, B or C amplifiers, frequency multipliers and oscillators of v.h.f. and u.h.f. equipment.
Encapsulated in a metal TO-39 envelope with the collector connected to the case.

QUICK REFERENCE DATA		
V_{CER} max.	40	V
V_{CEO} max.	20	V
I_C max.	400	mA
P_{tot} max. ($T_{case} \leq 25^oC$)	3.5	W
T_j max.	200	^oC
f_T typ. ($I_C = 25mA$, $V_{CE} = 10V$, $f = 100MHz$)	700	MHz
P_o typ. ($P_i < 100mW$, $V_{CE} = 12V$, $f = 175MHz$)	1.0	W
η min. ($P_o = 1.0W$, $V_{CE} = 12V$, $f = 175MHz$)	50	%

OUTLINE AND DIMENSIONS

Conforms to B.S. 3934 SO-3/SB3-3B
J.E.D.E.C. TO-39



	Millimetres		
	Min.	Typ.	Max.
A	9.10	-	9.40
B	8.2	-	8.5
C	6.15	-	6.60
D	-	5.08	-
E	0.71	-	0.86
F1	-	-	0.51
F2	12.7	-	-
F3	12.7	-	15
G1	-	-	1.01
G2	0.41	-	0.48
G3	-	-	0.53
H	-	0.4	-
J	0.74	-	1.01

Collector connected to case

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

V_{CBO} max.	40	V
V_{CER} max. (R_{BE}=10Ω)	40	V
V_{CEO} max.	20	V
V_{EBO} max.	2.0	V
I_C max.	400	mA
I_{CM} max.	400	mA
P_{tot} max. ($T_{case} \leq 25^oC$)	3.5	W

Temperature

T_{stg} min.	-65	^oC
T_{stg} max.	200	^oC
T_j max.	200	^oC

THERMAL CHARACTERISTICS

$R_{th(j-amb)}$	In free air	200	degC/W
$R_{th(j-case)}$		35	degC/W
$R_{th(case-h)}$	Mounted with a top clamping washer of accessory 56218	1.0	degC/W
$R_{th(case-h)}$	Mounted with a top clamping washer of accessory 56218 and a boron nitride washer for electrical insulation	1.2	degC/W

ELECTRICAL CHARACTERISTICS (T_j=25°C unless otherwise stated)

		Min.	Typ.	Max.	
I_{CEO}	Collector cut-off current V_{CE}=12V, I_B=0	-	-	20	μA
$V_{(BR)CBO}$	Collector-base breakdown voltage I_C=100μA, I_E=0	40	-	-	V
	Collector-emitter breakdown voltages				
$V_{(BR)CER}$	I_C=5.0mA, R_{BE}=10Ω	40	-	-	V
$V_{(BR)CEO}$	I_C=5.0mA, I_B=0	20	-	-	V
$V_{(BR)EBO}$	Collector-base breakdown voltage I_E=100μA, I_C=0	2.0	-	-	V

ELECTRICAL CHARACTERISTICS (cont'd)

		Min.	Typ.	Max.	
$V_{CE(sat)}$	Collector-emitter saturation voltage I_C = 100mA, I_B = 20mA	-	-	0.5	V
h_{FE}	Static forward current transfer ratio I_C = 100mA, V_{CE} = 5.0V	10	-	200	
	I_C = 360mA, V_{CE} = 5.0V	5	-	-	
f_T	Transition frequency I_C = 25mA, V_{CE} = 10V, f = 100MHz	-	700	-	MHz
C_{tc}	Collector capacitance V_{CB} = 12V, I_E = I_e = 0, f = 1.0MHz	-	-	4.0	pF

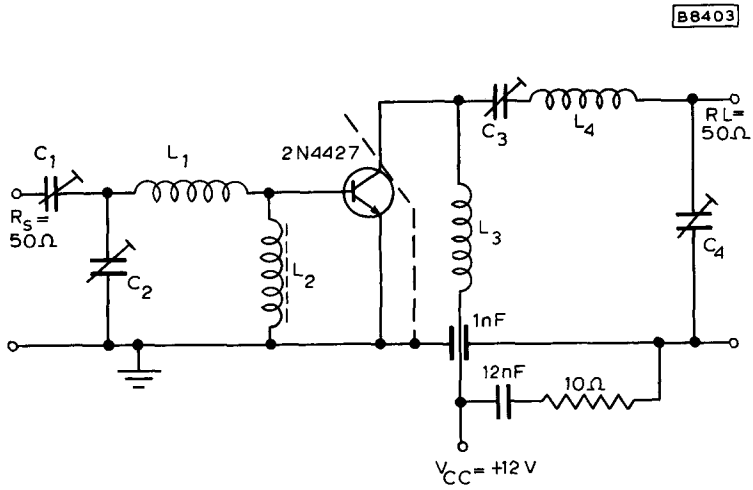
Typical r.f. performance

V_{CE} = 12V, T_{case} = 25°C

f	Frequency	175*	470	MHz
P_i	Input power	< 100	100	mW
I_C	Collector current	< 167	67	mA
P_o	Output power	1.0	0.4	W
η	Efficiency	> 50	50	%

*The transistor can withstand a load mismatch having a v.s.w.r. of 3, varied through all phases for conditions as given above (see also test circuit)

Common emitter test circuit (f = 175MHz)



Components

C_1, C_2, C_3, C_4 = 4 to 29pF air trimmers

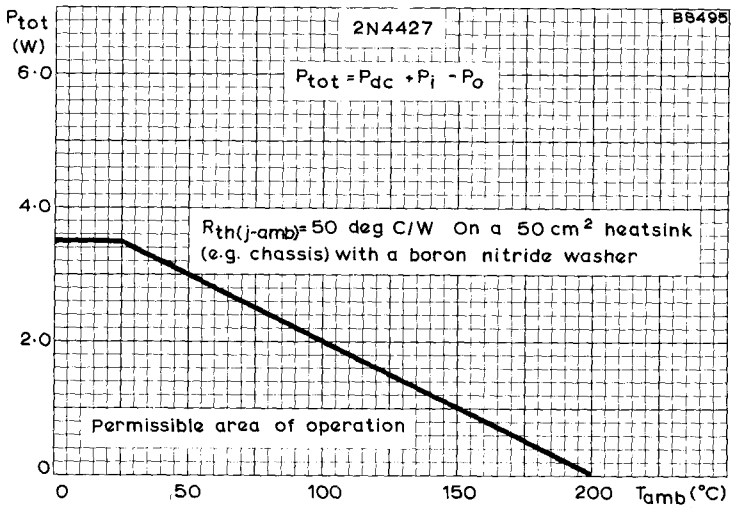
L_1 = 2 turns of 1mm Cu wire, int. dia. 6mm, winding pitch 2mm, leads 2 × 10mm

L_2 = ferroxcube choke coil (Z = 550Ω at 175MHz)

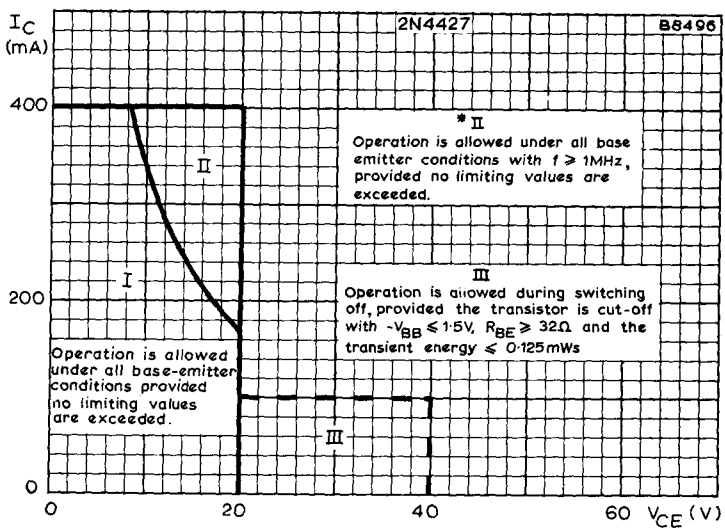
L_3 = 2 turns of 1mm Cu wire, int. dia. 5mm, winding pitch 2mm, leads 2 × 10mm

L_4 = 3 turns of 1.5mm Cu wire, int. dia. 10mm, winding pitch 2mm, leads 2 × 15mm

The length of the external emitter wire of the 2N4427 is 1.6mm

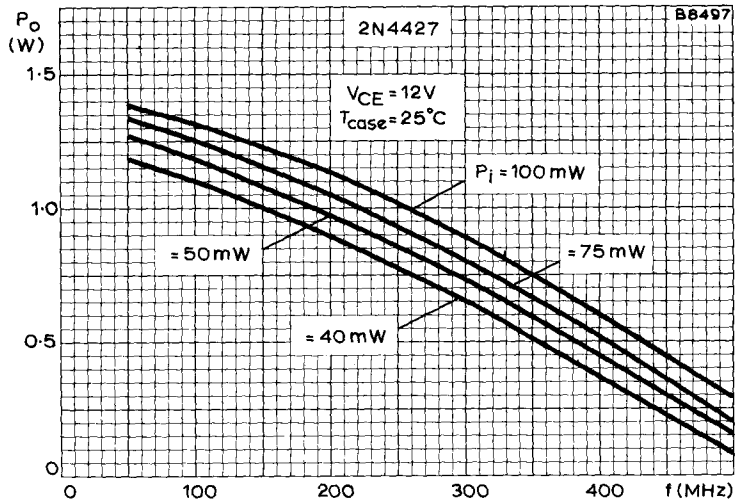


MAXIMUM TOTAL DISSIPATION PLOTTED AGAINST AMBIENT TEMPERATURE

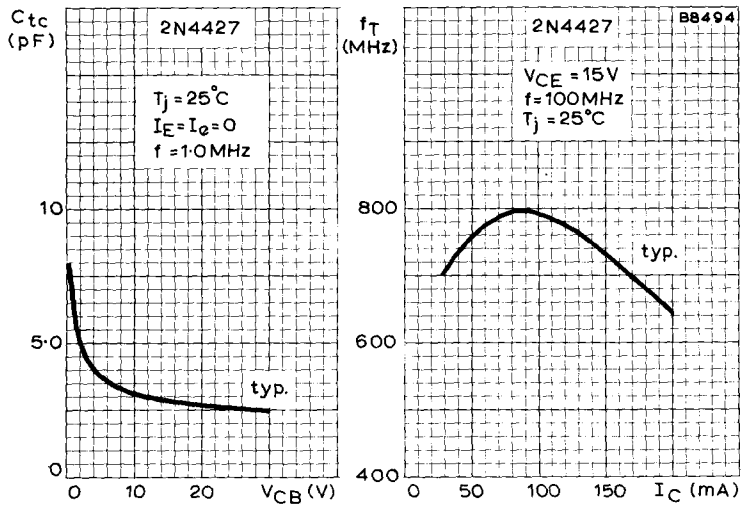


AREAS OF SAFE OPERATION

*II Care must be taken to reduce the steady state current to region I before removing the a.c. signal. This may be achieved by appropriate bias in class A. B or C.



TYPICAL VARIATION OF OUTPUT POWER WITH FREQUENCY AND INPUT POWER



Collector capacitance versus collector-base voltage

Transition frequency versus collector current

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

2N4856 to 2N4861

Silicon n-channel, depletion type, junction field-effect transistors intended for low power chopper or switching applications.

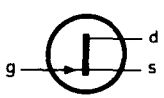
QUICK REFERENCE DATA

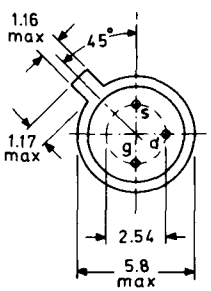
$\pm V_{DS}$ max.	Drain-source voltage	2N4856 to 2N4858		40	V
		2N4859 to 2N4861		30	V
P_{tot} max.	Total power dissipation ($T_{amb} \leq 25^{o}C$)		360		mW
		2N4856 2N4859	2N4857 2N4860	2N4858 2N4861	
I_{DSS} min.	Drain current ($V_{DS}=15V$, $V_{GS}=0$)	50	20	8	mA
$-V_{(P)GS}$	Gate-source cut-off voltage ($I_D=0.5nA$, $V_{DS}=15V$)	4-10	2-6	0.8-4	V
$r_{DS(on)}$ max.	Drain-source 'on' resistance ($I_D=0$, $V_{GS}=0$, f=1kHz)	25	40	60	Ω
$-C_{rs}$ max.	Feedback capacitance ($V_{DS}=0$, $-V_{GS}=10V$, f=1MHz)	8	8	8	pF
t_{off} max.	Turn-off time ($V_{DD}=10V$, $V_{GS}=0$)				
	$I_D=20mA$, $-V_{GSM}=10V$	25	-	-	ns
	$I_D=10mA$, $-V_{GSM}=6V$	-	50	-	ns
	$I_D=5mA$, $-V_{GSM}=4V$	-	-	100	ns

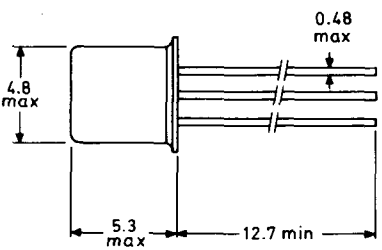
Unless otherwise stated data are applicable to all types

OUTLINE AND DIMENSIONS

Conforms to B.S. 3934 SO-12A/SB3-6A
J.E.D.E.C. TO-18
} Gate connected to the case







All dimensions in mm

D2872

Accessories supplied on request: 56246; 56263

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

		2N4856 2N4857 2N4858	2N4859 2N4860 2N4861	
$\pm V_{DS}$ max.	Drain-source voltage	40	30	V
V_{DGO} max.	Drain-gate voltage (open source)	40	30	V
$-V_{GSO}$ max.	Gate-source voltage (open drain)	40	30	V
I_G max.	Gate current (d.c.)	50		mA
P_{tot} max.	Total power dissipation ($T_{amb} \leq 25^oC$)	360		mW
Temperature				
T_{stg}	Storage temperature	-65 to +200		^oC
T_j	Junction temperature	200		^oC

THERMAL CHARACTERISTICS

$R_{th(j-amb)}$	Thermal resistance from junction to ambient in free air	0.49	$^oC/mW$

ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^oC$ unless otherwise stated)

			Min.	Max.	
$-I_{GSS}$	Gate cut-off current				
	$-V_{GS} = 20V$, $V_{DS} = 0$	2N4856 to 2N4858	-	0.25	nA
	$-V_{GS} = 15V$, $V_{DS} = 0$	2N4859 to 2N4861	-	0.25	nA
	$-V_{GS} = 20V$, $V_{DS} = 0$, $T_{amb} = 150^oC$	2N4856 to 2N4858	-	0.5	μA
	$-V_{GS} = 15V$, $V_{DS} = 0$, $T_{amb} = 150^oC$	2N4859 to 2N4861	-	0.5	μA
I_{DSX}	Drain cut-off current				
	$V_{DS} = 15V$, $-V_{GS} = 10V$		-	0.25	nA
	$V_{DS} = 15V$, $-V_{GS} = 10V$, $T_{amb} = 150^oC$		-	0.5	μA
I_{DSS}	Drain current (pulse measurement, $t_p = 100ms$, $d \leq 0.1$)				
	$V_{DS} = 15V$, $V_{GS} = 0$	2N4856, 2N4859	50	-	mA
		2N4857, 2N4860	20	100	mA
		2N4858, 2N4861	8.0	80	mA

ELECTRICAL CHARACTERISTICS (contd.)

			Min.	Max.	
$-V_{(BR)GSS}$	Gate-source breakdown voltage $-I_G = 1\mu A$, $V_{DS} = 0$	2N4856 to 2N4858	40	-	V
		2N4859 to 2N4861	30	-	V
$-V_{(P)GS}$	Gate-source cut-off voltage $I_D = 0.5nA$, $V_{DS} = 15V$	2N4856, 2N4859	4.0	10	V
		2N4857, 2N4860	2.0	6.0	V
		2N4858, 2N4861	0.8	4.0	V
$V_{DS(on)}$	Drain-source 'on' voltage $I_D = 20mA$, $V_{GS} = 0$	2N4856, 2N4859	-	0.75	V
	$I_D = 10mA$, $V_{GS} = 0$	2N4857, 2N4860	-	0.50	V
	$I_D = 5mA$, $V_{GS} = 0$	2N4858, 2N4861	-	0.50	V
$r_{DS(on)}$	Drain-source 'on' resistance $I_D = 0$, $V_{GS} = 0$, $f = 1kHz$	2N4856, 2N4859	-	25	Ω
		2N4857, 2N4860	-	40	Ω
		2N4858, 2N4861	-	60	Ω
y-parameters (common source) $-V_{GS} = 10V$, $V_{DS} = 0$, $f = 1MHz$					
C_{is}	Input capacitance		-	18	pF
$-C_{rs}$	Feedback capacitance		-	8.0	pF

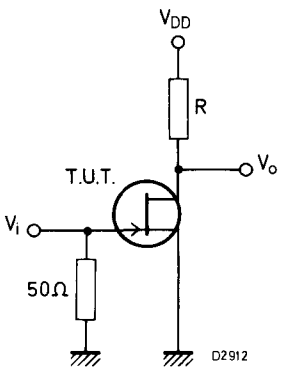
ELECTRICAL CHARACTERISTICS (contd.)

Switching times

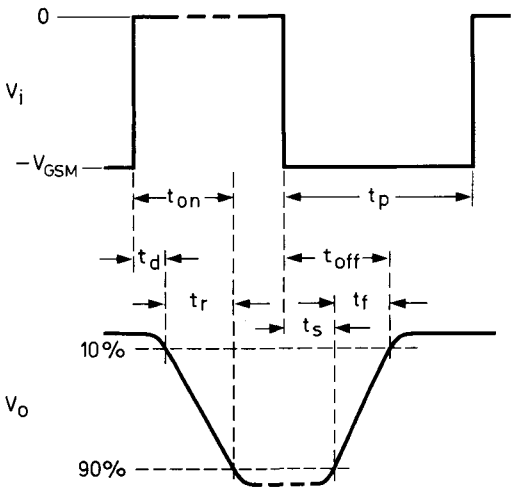
V_{DD} = 10V, V_{GS} = 0

			2N4856 2N4859	2N4857 2N4860	2N4858 2N4861	
		I_D =	20	10	5.0	mA
		$-V_{GSM}$ =	10	6.0	4.0	V
t_d	Delay time	max.	6.0	6.0	10	ns
t_r	Rise time	max.	3.0	4.0	10	ns
t_{off}	Turn-off time	max.	25	50	100	ns

Test circuit:



Input and output waveforms



	2N4856 2N4859	2N4857 2N4860	2N4859 2N4861	
R =	464	953	1910	Ω

Pulse generator:

t_p = 200 ns

$t_r \leq$ 1 ns

$t_f \leq$ 1 ns

d = 0.02

Z_o = 50 Ω

Oscilloscope:

$t_r \leq$ 0.75 ns

$R_i \geq$ 1 MΩ

$C_i \leq$ 2.5 pF

ACCESSORIES

C

ACCESSORIES FOR TRANSISTORS

Section 1 Cooling Clips

PART NUMBER	FOR USE ON OUTLINES		PAGE
	J.E.D.E.C.	BS 3934	
56200*	TO–1	SO–21/SB3–10	3
56207*	TO–7	SO–23/SB4–4	4
56209*	TO–1	SO–21/SB3–10	5
56226	TO–1	SO–21/SB3-10	6
56227	TO–1	SO–21/SB3–10	7
56263	TO–18	SO–12A/SB3–6A	8
	TO–71	SO–12A/SB8–1B	
	TO–72	SO–12A/SB4–3	
56265	TO–5	SO–3/SB3–3A	9
	TO–12	SO–3/SB4–1	
	TO–33	SO–3/SB4–1	
	TO–39	SO–3/SB3–3B	

*These devices are supplied on a maintenance basis only, they are not recommended for current design

Section 2 Mounting Accessories

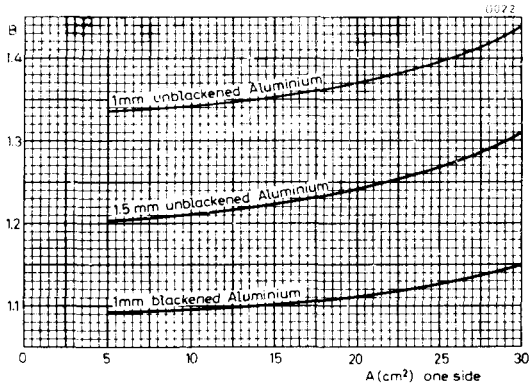
PART NUMBER	DESCRIPTION	FOR USE ON OUTLINES		PAGE
56201A	**Insulating bush**	TO–3 3.15mm (thick or medium with 56300)		10
56201B	**Mica washer**	TO–3 all		10
56239A	**Insulating bush**	TO–3 1.6mm (medium)		16
56336A	**Insulating bush (2kV)**	TO–3 3.15mm (thick)		17
56336B	**Mica washer (2kV)**	TO–3 all		17
56214	**Lead washer**	TO–3 all		10
56300	**Steel spacer**	TO–3 0.9 or 1.6mm (thin or medium)		11
56218	**Top and bottom clamping washer and Mylar washer**	TO–5, TO–39 (and TO–12, TO–33 for non-insulated mounting)		12
56245	**Insulated distance disc**	TO–5, TO–12, TO–33, TO–39		13
56246	**Insulated distance disc**	TO–18, TO–72		13
56301B	**Mica washer**	TO–126		14–15
56326	**Flat metal washer**	TO–126		14–15
56325	**Mica washer**	TO–220		18
56338	**Insulating bush**	TO–220		18
56239A	**Insulating bush**	—	SO–55 (BS 3934)	16
56239B	**Mica washer**	—	SO–55 (BS 3934)	16

All information on thermal resistance of the accessories combined with flat heatsinks is valid for **square** heatsinks of **blackened aluminium.**

For a few variations the thermal resistance may be derived as follows:

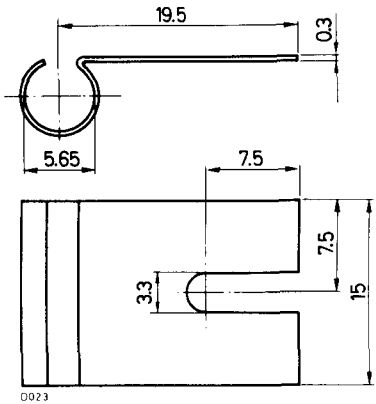
a. **Rectangular heatsinks** (sides a and 2a)
When mounted with long side horizontal, multiply by 0.95.
When mounted with short side horizontal, multiply by 1.10.

b. **Unblackened or thicker heatsinks**
Multiply by the factor B given below as a function of the heatsink size A.



COOLING CLIP

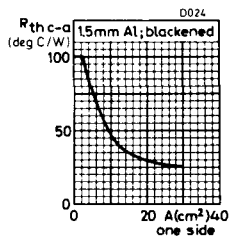
MECHANICAL DATA (Dimensions in mm)



Clip material: brass, nickel plated

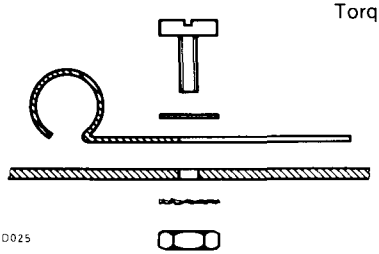
THERMAL CHARACTERISTICS

$R_{th(case-amb)}$	Thermal resistance case to ambient, cooling clip only	100 degC/W
	with heatsink	see graph



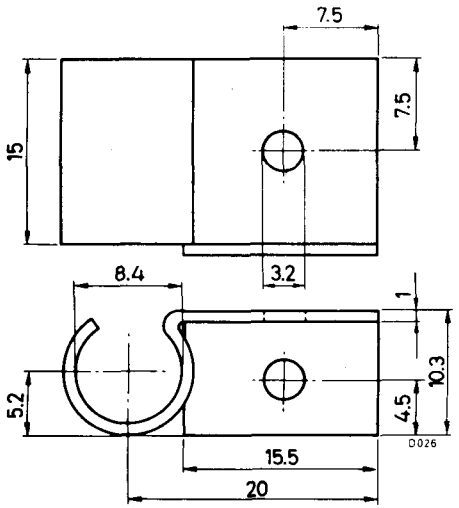
MOUNTING INSTRUCTIONS

Torque on nut for good heat transfer: 5kg cm



COOLING CLIP

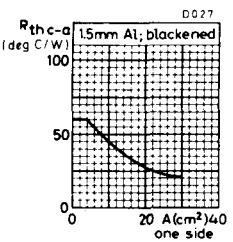
MECHANICAL DATA (Dimensions in mm)



Clip material: aluminium, blackened

THERMAL CHARACTERISTICS

$R_{th(case-amb)}$	Thermal resistance case to ambient, cooling clip only	60 degC/W
	with heatsink	see graph



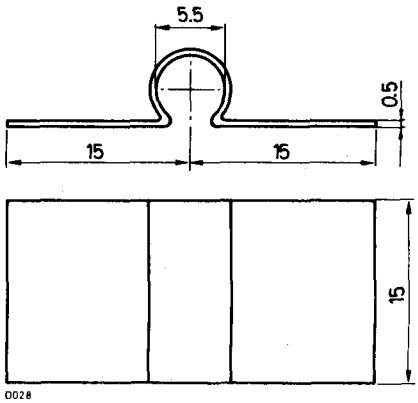
MOUNTING INSTRUCTIONS

Torque on M3 bolts for good heat transfer: 5kg cm

56209

COOLING CLIP

MECHANICAL DATA (Dimensions in mm)



Clip material: brass, nickel plated

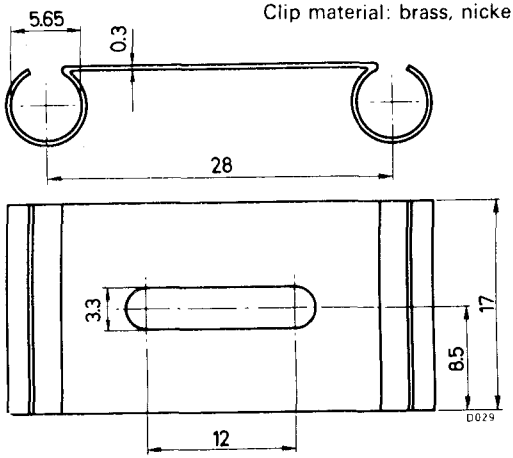
THERMAL CHARACTERICTIC

$R_{th(case-amb)}$	Thermal resistance case to ambient, cooling clip only	75 degC/W

COOLING CLIP

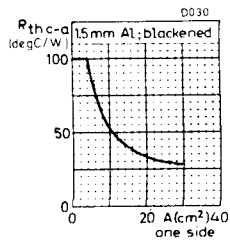
MECHANICAL DATA (Dimensions in mm)

Clip material: brass, nickel plated



THERMAL CHARACTERISTICS

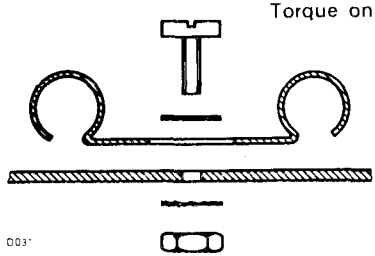
$R_{th\,case\text{-}amb}$	Thermal resistance case to ambient, cooling clip only	100 degC/W
	with heatsink	see graph



The thermal resistance values apply to each transistor, provided the two transistors have been mounted so that the heat flow from each one is equal.

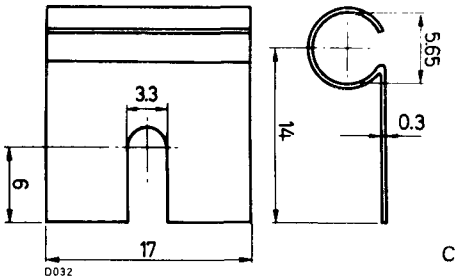
MOUNTING INSTRUCTIONS

Torque on nut for good heat transfer: 5kg cm.



COOLING CLIP

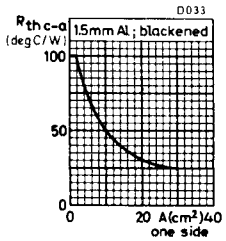
MECHANICAL DATA (Dimensions in mm)



Clip material: brass, nickel plated

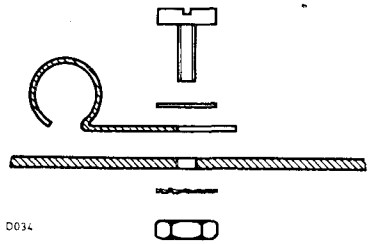
THERMAL CHARACTERISTICS

$R_{th(case-amb)}$	Thermal resistance case to ambient, cooling clip only	100 degC/W
	with heatsink	see graph



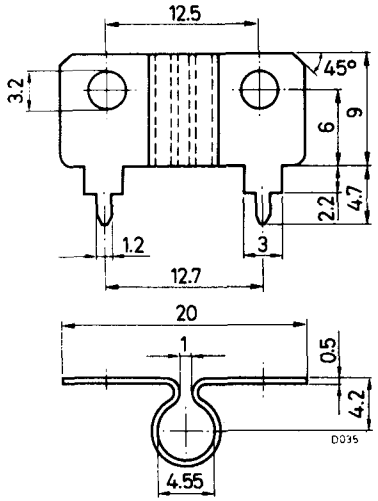
MOUNTING INSTRUCTIONS

Torque on nut for good heat transfer: 5kg cm



COOLING CLIP

MECHANICAL DATA (Dimensions in mm)



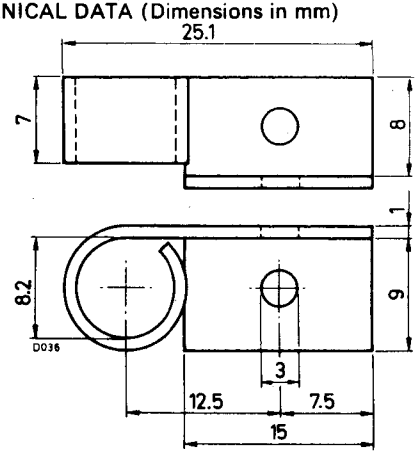
Clip material: copper, tin plated

THERMAL CHARACTERISTIC

$R_{th(case-amb)}$	Thermal resistance case to ambient	100 degC/W

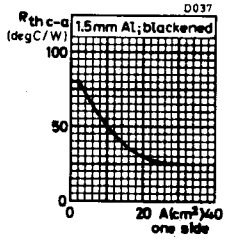
COOLING CLIP

MECHANICAL DATA (Dimensions in mm)



Clip material: aluminium, blackened

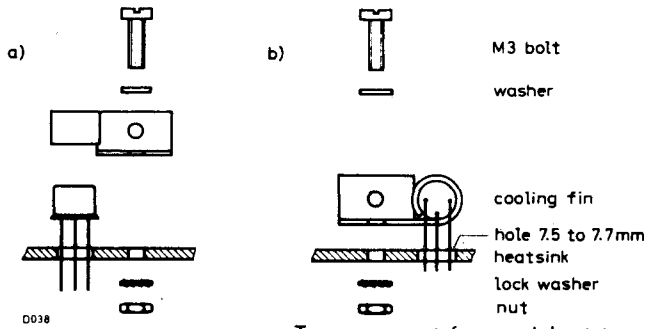
THERMAL CHARACTERISTICS



$R_{th(case-amb)}$ Thermal resistance case to ambient, cooling clip only with heatsink

80 degC/W
see graph

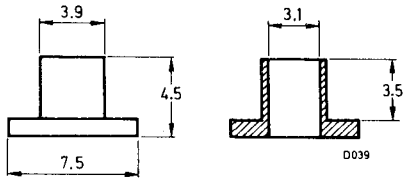
MOUNTING INSTRUCTIONS



Torque on nut for good heat transfer: 5kg cm.

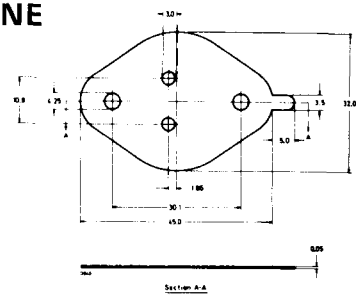
MOUNTING ACCESSORIES FOR TO-3 OUTLINE

MECHANICAL DATA (Dimensions in mm)



Insulating bush

56201A



Mica washer

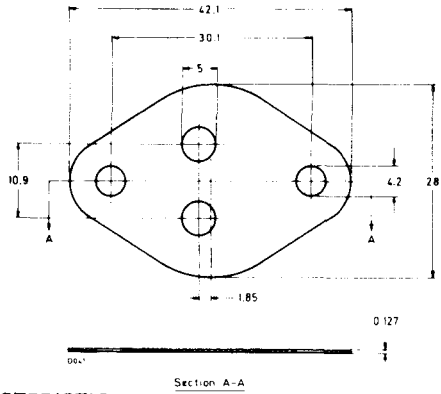
56201B

THERMAL CHARACTERISTIC

$R_{th(mb-h)}$	Thermal resistance mounting-base to heatsink	1 degC/W

56214 Lead washer

MECHANICAL DATA (Dimensions in mm)



THERMAL CHARACTERISTIC

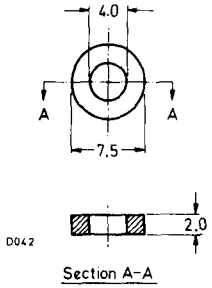
$R_{th(mb-h)}$	Thermal resistance mounting-base to heatsink, with mica washer and lead washer	0·75 degC/W

TEMPERATURE

T_{max}	Max. allowable temperature	150 °C

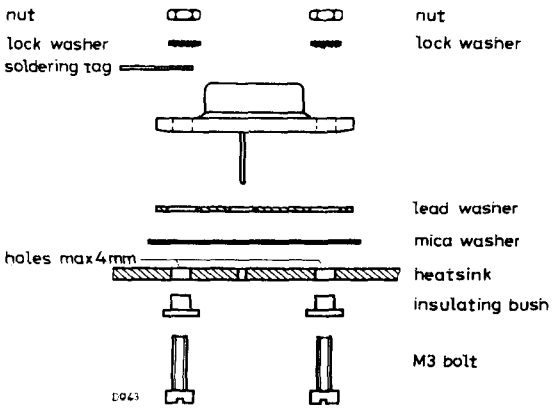
MOUNTING ACCESSORIES FOR TO-3 OUTLINE

56300 Steel spacer



For use with thin-base devices only.

MOUNTING INSTRUCTIONS

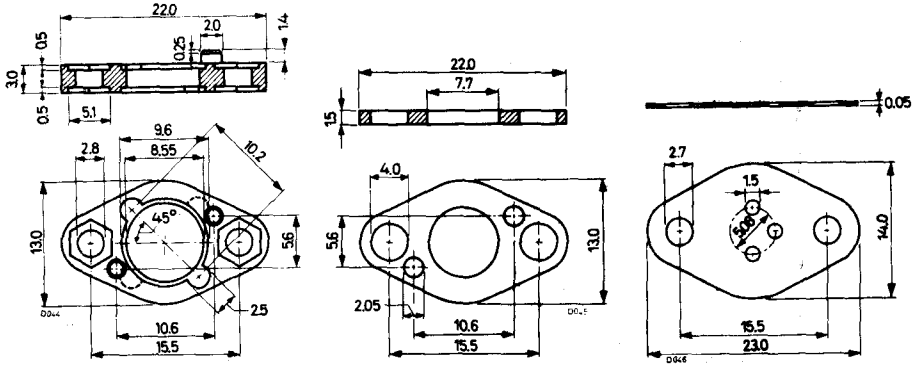


Torque on nut for good heat transfer: 5kg cm

MOUNTING ACCESSORIES FOR TO-5, TO-12, TO-33, TO-39 OUTLINES

56218 Top and bottom clamping washers and Mylar washer

MECHANICAL DATA (Dimensions in mm)



Top clamping washer of insulating material

Bottom clamping washer material: brass, tin plated

Mylar washer

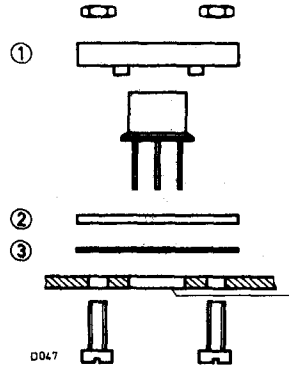
THERMAL CHARACTERISTICS

$R_{th(mb-h)}$	Thermal resistance mounting-base to heatsink,	
	non-insulated mounting	1 degC/W
	insulated mounting	6 degC/W

TEMPERATURE

T_{max}	Max. allowable temperature	100 °C

MOUNTING INSTRUCTIONS

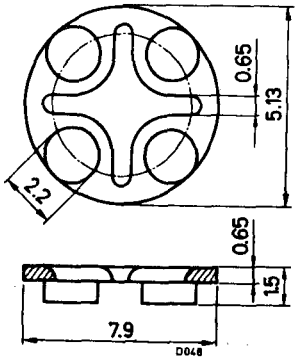


Non-insulated: without items 2 and 3
Note: Item 1 must then be mounted upside down.

MOUNTING ACCESSORIES FOR TO-5, TO-12, TO-33, TO-39 OUTLINES (cont'd)

56245 Distance disc

MECHANICAL DATA (Dimensions in mm)

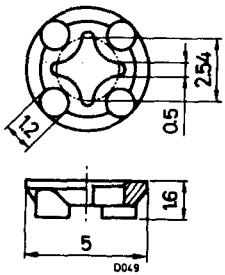


Insulating material

TEMPERATURE

T_{max}	Max. allowable temperature	100 °C

56246 Distance disc



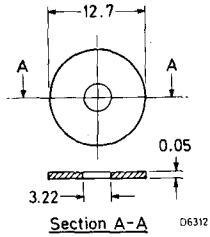
Insulating material

TEMPERATURE

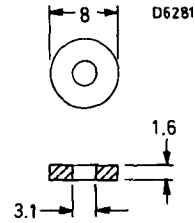
T_{max}	Max. allowable temperature	100 °C

MOUNTING ACCESSORIES FOR TO-126 OUTLINE

56301B Mica washer
56326 Steel washer
MECHANICAL DATA (Dimensions in mm)



Mica washer

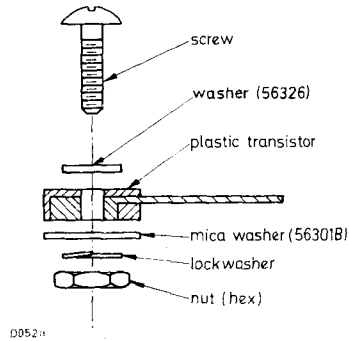


Steel washer

THERMAL CHARACTERISTICS

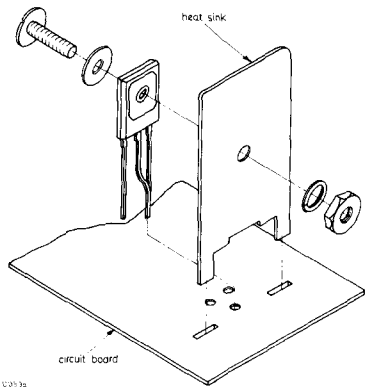
$R_{th(mb-h)}$	Thermal resistance mounting-base to heatsink,	
	without insulating material	1 degC/W
	with mica washer (56301B)	4 degC/W

MOUNTING INSTRUCTIONS

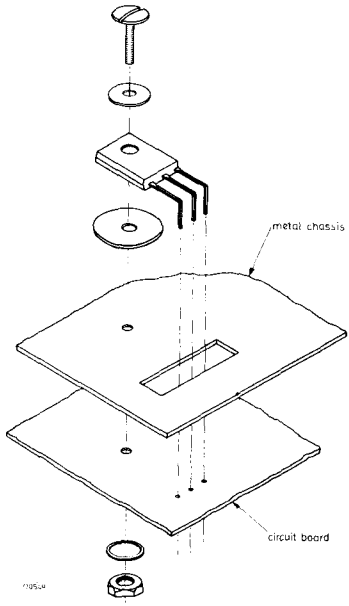


MOUNTING DETAILS
TO-126 OUTLINE

METHOD 1

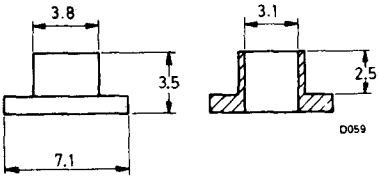


METHOD 2

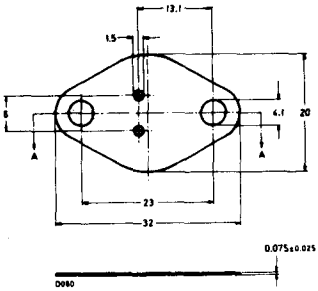


MOUNTING ACCESSORIES FOR BS 3934 SO-55B OUTLINE

MECHANICAL DATA (Dimensions in mm)



Insulating bush
56239A



Mica washer
56239B

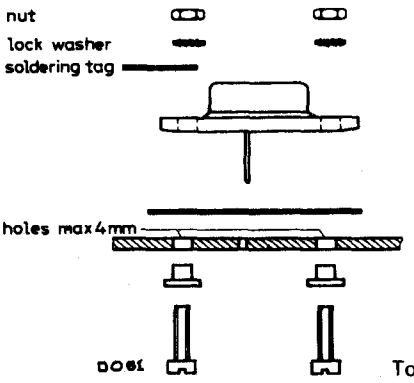
THERMAL CHARACTERISTIC

$R_{th(mb-h)}$	Thermal resistance mounting-base to heatsink	1·5 degC/W

TEMPERATURE

T_{max}	Max. allowable temperature	150 °C

MOUNTING INSTRUCTIONS

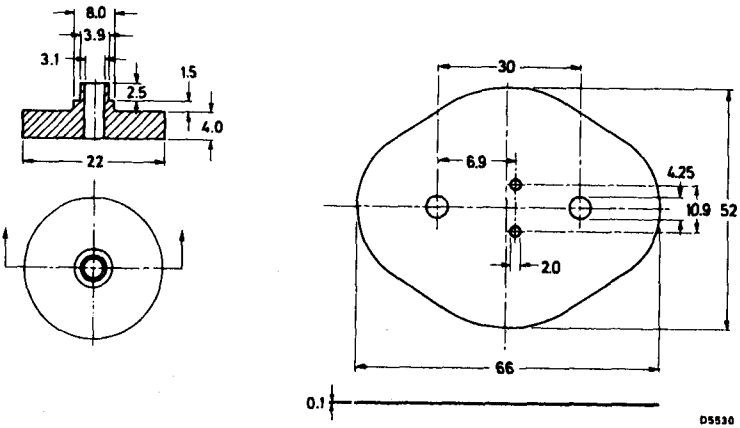


Torque on nut for good heat transfer: 5kg cm.

MOUNTING ACCESSORIES FOR TO-3 OUTLINE

(High Voltage Application, up to 2kV)

56336A **Insulating bush**
56336B **Mica washer**



Dimensions in mm

THERMAL CHARACTERISTICS

$R_{th(mb-h)}$	Thermal resistance, mounting-base to heatsink	1°C/W

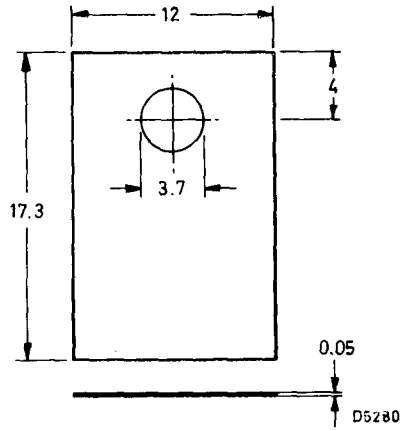
The use of a heatsink compound is essential.
When the mica washer is used, the compound must be applied to both sides of the washer.

MOUNTING ACCESSORIES FOR TO-220

→ 56325 Mica washer

MECHANICAL DATA

Dimensions in mm



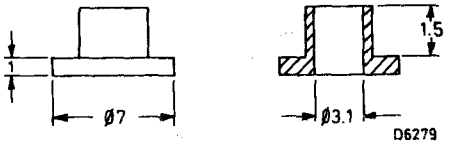
THERMAL RESISTANCE

From mounting base to heatsink $R_{th(mb-h)}$ = 2.5°C/W.

→ 56338 Insulating bush

MECHANICAL DATA

Dimension in mm



ABRIDGED DATA FOR EARLIER TYPES

D

ABRIDGED DATA FOR EARLIER TYPES

Abridged data only are given in these tables. Full data for these types are available on request

GERMANIUM TRANSISTORS

Type No.	Polarity	Outline	Maximum Ratings					P_{tot} at 25°C	h_{fe}		at	f_T	$V_{CE(sat)}$	at		Typical power gain at f	
			V_{CB}	V_{CE}	I_{CM}	$I_{C(AV)}$	T_j		min.	max.	I_C	min.	max.	I_C	I_B		
			(V)	(V)	(mA)	(mA)	(°C)	(mW)			(mA)	(MHz)	(V)	(mA)	(mA)	(dB)	(MHz)
ACY17	p-n-p	TO–5	–70	–60	2A	500	90	260	50**	150	300	1*	–0·35	500	25	—	—
ACY18	p-n-p	TO–5	–50	–40	2A	500	90	260	40**	120	300	1*	–0·35	500	25	—	—
ACY19	p-n-p	TO–5	–50	–40	2A	500	90	260	80**	250	300	1·3*	–0·35	500	25	—	—
ACY20	p-n-p	TO–5	–40	–32	2A	500	90	260	50**	145	50	1*	–0·2	50	1·3	—	—
ACY21	p-n-p	TO–5	–40	–32	2A	500	90	260	90**	250	50	1·3*	–0·2	50	1·3	—	—
ACY22	p-n-p	TO–5	–20	–20	2A	500	90	260	30**	300	300	1*	–0·35	500	25	—	—
ACY39	p-n-p	TO–5	–110	–75	2A	500	90	260	50**	150	300	1*	–0·35	500	25	—	—
ACY40	p-n-p	TO–5	–32	–32	2A	500	90	260	30**	70	300	0·8*	–0·35	500	25	—	—
ACY41	p-n-p	TO–5	–32	–32	2A	500	90	260	50**	250	300	0·6*	–0·35	500	25	—	—
ACY44	p-n-p	TO–5	–50	–40	2A	500	90	260	30	100	1	1*	–0·2	50	1·3	—	—
ADY26	p-n-p	TO–36	–80	–60	30A	25A	90	100W	40**	120	5A	—	–0·5	25A	2·5A	—	—
ADZ11	p-n-p	TO–36	–50	–40	20A	15A	90	45W	40**	120	1·2A	80kHz	–1·0	15A	2A	—	—
ADZ12	p-n-p	TO–36	–80	–60	20A	15A	90	45W	40**	120	1·2A	100kHz	–1·0	15A	2A	—	—
AF114	p-n-p	TO–7	–20	–20	10	10	75	85	40	—	1	75*	—	—	—	14	100
AF115	p-n-p	TO–7	–20	–20	10	10	75	85	40	—	1	75*	—	—	—	13	100
AF116	p-n-p	TO–7	–20	–20	10	10	75	85	40	—	1	75*	—	—	—	25	10·7
AF117	p-n-p	TO–7	–20	–20	10	10	75	85	40	—	1	75*	—	—	—	42	0·4
ASY26	p-n-p	TO–5	–30	–15	300	200	85	150	30**	80	20	4	–0·2	10	0·3	—	—
ASY27	p-n-p	TO–5	–25	–15	300	200	85	150	50**	150	20	6	–0·2	10	0·2	—	—
ASY28	n-p-n	TO–5	30	15	300	200	85	150	30**	80	20	4	0·2	10	0·3	—	—

*typical **h_{FE}

GERMANIUM TRANSISTORS (cont.)

Type No.	Polarity	Outline	Maximum Ratings V_{CB} (V)	V_{CE} (V)	I_{CM} (mA)	$I_{C(AV)}$ (mA)	T_j (°C)	P_{tot} at 25°C (mW)	h_{fe} min.	h_{fe} max.	at I_C (mA)	f_T min. (MHz)	$V_{CE(sat)}$ max. (V)	at I_C (mA)	at I_B (mA)	Typical Power gain at f (dB)	(MHz)
ASY29	n-p-n	TO–5	25	15	300	200	85	150	50**	150	20	10	0·2	10	0·2	—	—
ASZ21	p-n-p	TO–18	–20	–15	50	30	85	120	35	—	10	300	–0·35	10	1·0	—	—
OC20	p-n-p	TO–3	–100	–75	10A	8A	90	30W‡	25	75	1A	0·25	—	—	—	—	—
OC22	p-n-p	TO–3	–47	–32	2A	1A	90	22·5W†	50**	—	1A	2	–0·6*	1A	30	—	—
OC23	p-n-p	TO–3	–55	–40	2A	1A	90	22·5W†	50**	—	1A	2·5	–0·4*	1A	30	—	—
OC24	p-n-p	TO–3	–47	–40	2A	1A	90	22·5W†	50**	—	1A	2·5	–0·4*	1A	30	—	—
OC25	p-n-p	TO–3	–40	–40	4A	4A	90	22·5W†	15**	80	1A	0·25	—	—	—	—	—
OC41	p-n-p	SO–2	–16	–15	150	50	75	112	20	90	10	3	–0·2	50	3	—	—
OC42	p-n-p	SO–2	–16	–15	150	50	75	112	40	—	10	5·5	–0·2	50	1·5	—	—
OC43	p-n-p	SO–2	–15	–15	150	50	75	112	50	200	50	12	–0·28	125	7	—	—
OC44	p-n-p	SO–2	–15	–15	10	5	75	70	40	225	1	7·5	–0·15	8	0·5	—	—
OC45	p-n-p	SO–2	–15	–15	10	5	75	70	25	125	1	3	–0·15	8	0·5	—	—
OC70	p-n-p	SO–2	–30	–30	50	10	75	125	20	40	0·5	5kHz	–0·33	9	0·5	—	—
OC71	p-n-p	SO–2	–30	–30	50	10	75	125	41	—	1	5kHz	–0·21	9	0·5	—	—
OC72	p-n-p	SO–2	–32	–32	250	125	75	125	45	120	10	0·33	—	—	—	—	—
OC75	p-n-p	SO–2	–30	–30	50	10	75	125	60	130	3	0·9	–0·21	9	0·5	—	—
OC76	p-n-p	SO–2	–32	–32	250	125	75	125	45	—	10	0·35	—	—	—	—	—
OC77	p-n-p	SO–2	–60	–60	250	125	75	125	45	—	10	0·35	—	—	—	—	—
OC139	n-p-n	SO–2	20	20	250	250	75	145	20	84	15	3·5	0·22	50	3	—	—
OC140	n-p-n	SO–2	20	20	400	400	75	145	50	150	15	4·5	0·22	50	1·2	—	—
OC141	n-p-n	SO–2	20	20	400	400	75	145	80	200	15	9·0	0·22	50	0·7	—	—
OC170	p-n-p	TO–7	–20	–20	10	10	75	85	40	—	1	75*	—	—	—	25	10
OC171	p-n-p	TO–7	–20	–20	10	10	75	85	40	—	1	75*	—	—	—	14	100

*typical **h_{FE} †$T_{case} \leqslant 25°C$ ‡$T_{case} \leqslant 45°C$

SILICON TRANSISTORS

Type No.	Polarity	Outline	Maximum Ratings					P_{tot} at 25°C	h_{FE}		at I_C	f_T	$V_{CE(sat)}$	at		t_{on}	t_{off}	at
			V_{CBO}	V_{CEO}	I_{CM}	$I_{C(AV)}$	T_j		min.	max.		min.	max.	I_C	I_B			
			(V)	(V)	(mA)	(mA)	(°C)	(mW)			(mA)	(MHz)	(V)	(mA)	(mA)	(ns)	(ns)	(mA)
BC146	n-p-n	μ min.	20	20	50	50	125	50	80	550	0.2	150*	0·18*	2·0	—	—	—	—
BC186	p-n-p	TO–18	–40	–25	200	100	175	300	40	200	2·0	50	–0·5	50	5	—	—	—
BC187	p-n-p	TO–18	–30	–25	200	100	175	300	100	500	2·0	50	–0·5	50	5	—	—	—
BC200	p-n-p	μ min.	–20	–20	50	50	125	50	50	400	0·2	90*	–0·2*	2·0	—	—	—	—
§**BCY55**	n-p-n	Block	45	45	60	30	125	300	200	600	10	50	1·0	10	0·5	—	—	—
BCZ11	p-n-p	SO–2	–30	–25	100	50	150	250	15	50	20	0·9	–0·55	20	3	—	—	—
BD115	n-p-n	TO–39	245	180	200	150	200	6†	22	—	50	145*	9·0	100	10	—	—	—
BD121	n-p-n	TO–3	60	35	5A	5A	175	45W	30	—	1A	60	0·65	1A	100	—	—	—
BD123	n-p-n	TO–3	90	60	5A	5A	175	45W	30	—	1A	60	0·65	1A	100	—	—	—
BD124	n-p-n	SO–55	70	45	4A	2A	175	15W	35	—	500	60	0·50	2A	200	—	—	—
BDY10	n-p-n	TO–3	50	40	4A	2A	175	150W†	10	50	2A	1·0	0·7	2A	400	—	—	—
BDY11	n-p-n	TO–3	100	70	4A	2A	175	150W†	10	50	2A	1·0	0·7	2A	400	—	—	—
BDY60	n-p-n	TO–3	120	60	10A	5A	175	15W	45	450	500	100*	0·7	5A	500	120	350	5A
BDY61	n-p-n	TO–3	100	60	10A	5A	175	15W	45	450	500	100*	0·9	5A	500	120	350	5A
BDY62	n-p-n	TO–3	60	30	10A	5A	175	15W	45	450	500	100*	0·9	5A	500	120	350	5A
BF115	n-p-n	TO–72	50	30	30	30	175	145	48	—	1	230*	—	—	—	—	—	—
BF167	n-p-n	TO–72	40	30	25	25	175	130	—	—	—	350*	—	—	—	—	—	—
BF173	n-p-n	TO–72	40	25	25	25	175	260	—	—	—	550*	—	—	—	—	—	—
BF177	n-p-n	TO–5	100	50	60	50	200	600	20	—	15	120*	—	—	—	—	—	—
BF178	n-p-n	TO–5	160	115	50	50	200	600	20	—	30	120*	—	—	—	—	—	—

*typical †$T_{mb} \leqq 25°C$ §Dual transistor

SILICON TRANSISTORS (cont.)

Type No.	Polarity	Outline	Maximum Ratings					P_{tot} at 25°C	h_{FE}		at	f_T	$V_{CE(sat)}$	at		t_{on}	t_{off}	at
			V_{CBO}	V_{CEO}	I_{CM}	$I_{C(AV)}$	T_j		min.	max.	I_C	min.	max.	I_C	I_B			
			(V)	(V)	(mA)	(mA)	(°C)	(mW)			(mA)	(MHz)	(V)	(mA)	(mA)	(ns)	(ns)	(mA)
BF179	n-p-n	TO–5	250	115	50	50	200	500	20	—	20	120*	—	—	—	—	—	—
BF182	n-p-n	TO–72	25	20	15	15	175	150	—	—	—	650*	—	—	—	—	—	—
BF183	n-p-n	TO–72	25	20	15	15	175	150	—	—	—	800*	—	—	—	—	—	—
BF262	n-p-n	T pack	30	20	20	20	125	120	—	—	—	650*	—	—	—	—	—	—
BF263	n-p-n	T pack	30	20	20	20	125	120	—	—	—	525	—	—	—	—	—	—
BF264	n-p-n	T pack	30	20	20	20	125	120	—	—	—	400	—	—	—	—	—	—
BFS18R	n-p-n	μ min.	30	20	30	30	125	110	35	125	1·0	200*	—	—	—	—	—	—
BFS19R	n-p-n	μ min.	30	20	30	30	125	110	65	225	1·0	260*	—	—	—	—	—	—
BFS92	p-n-p	TO–39	–100	–60	1A	1A	200	5W†	30	—	150	70*	–1·0	500	50	—	—	—
BFS93	p-n-p	TO–39	–100	–60	1A	1A	200	5W†	70	—	150	70*	–1·0	500	50	—	—	—
BFS94	p-n-p	TO–39	–80	–40	1A	1A	200	5W†	40	—	150	70*	–0·7	500	50	—	—	—
BFS95	p-n-p	TO–39	–40	–35	1A	1A	200	5W†	70	—	150	70*	–0·7	500	50	—	—	—
BFW16	n-p-n	TO–5	40	25	300	150	200	1·5W‡	25	—	150	1200*	—	—	—	—	—	—
BFW17	n-p-n	TO–5	40	25	300	150	200	1·5W‡	25	—	150	1100*	—	—	—	—	—	—
BFW45	n-p-n	TO–39	165	130	100	50	200	2·5W‡	20	120	50	80	3·0	10	1	—	—	—
BFW57	n-p-n	Lock-fit	80	60	1A	500	125	350	80	—	100	80	0·7	500	50	—	—	—
BFW58	n-p-n	Lock-fit	80	60	1A	500	125	350	50	—	100	80	0·7	500	50	—	—	—
BFW59	n-p-n	Lock-fit	40	35	1A	500	125	350	80	—	100	80	0·7	500	50	—	—	—
BFW60	n-p-n	Lock-fit	40	35	1A	500	125	350	50	—	100	80	0·7	500	50	—	—	—
BFW87	p-n-p	Lock-fit	–60	–60	500	500	125	300	80	320	150	100	–0·4	150	15	50	290	100

*typical ‡$T_{case} \leqslant 125°C$ †$T_{mb} \leqslant 50°C$

SILICON TRANSISTORS (cont.)

Type No.	Polarity	Outline	Maximum Ratings					P_{tot} at 25°C	h_{FE}		at	f_T	$V_{CE(sat)}$	at		t_{on}	t_{off}	at
			V_{CBO}	V_{CEO}	I_{CM}	$I_{C(AV)}$	T_j		min.	max.	I_C	min.	max.	I_C	I_B			
			(V)	(V)	(mA)	(mA)	(°C)	(mW)			(mA)	(MHz)	(V)	(mA)	(mA)	(ns)	(ns)	(mA)
BFW88	p-n-p	Lock-fit	–60	–60	500	500	125	300	40	130	150	100	–0·4	150	15	50	290	100
BFW89	p-n-p	Lock-fit	–40	–40	500	500	125	300	80	320	150	100	–0·4	150	15	50	290	100
BFW90	p-n-p	Lock-fit	–40	–40	500	500	125	300	40	120	150	100	–0·4	150	15	50	290	100
BFW91	p-n-p	Lock-fit	–20	–20	500	500	125	300	40	125*	150	100	–0·4	150	15	50	290	100
BFW92	n-p-n	T pack	25	15	50	25	125	130	20	150	2·0	1600*	0·75	20	—	—	—	—
BFX12	p-n-p	TO–18	–20	–15	140	100	200	300	20	60	10	150	–0·25	10	1	—	—	—
BFX13	p-n-p	TO–18	–20	–15	140	100	200	300	50	250	10	150	–0·25	10	1	—	—	—
BFX34	n-p-n	TO–39	120	60	5A	2A	200	870	40	150	2A	70	1·0	5A	500	210	340	5A
BFX37	p-n-p	TO–18	–60	–60	50	50	200	360	100	170*	10	—	–0·25	10	0·5	—	—	—
BLY17	n-p-n	TO–36	100	100**	10A	10A	175	100W†	5	—	5A	50	2·0	10A	2A	—	—	—
BSS27	n-p-n	TO–39	70	45	1A	1A	200	800	25	—	500	400*	0·4	500	35	25	40	500
BSS28	n-p-n	TO–39	50	30	1A	1A	200	800	30	—	500	400*	0·5	500	35	25	45	500
BSS29	n-p-n	TO–39	50	30	1A	1A	200	800	20	—	500	400*	0·5	500	35	30	50	500
BSW41	n-p-n	TO–18	40	25	500	300	200	1W	20	—	500	250	0·5	150	15	50	100	300
BSW65	n-p-n	TO–5	80	80	2A	1A	200	800	40	—	100	80*	0·4	500	5·0	—	—	—
BSW69	n-p-n	Plastic	150	150	50	50	125	125	30	—	4	130*	4·0	20	1·0	—	—	—
BSX12	n-p-n	TO–39	25	12	1A	1A	200	3W‡	30	120	300	450	0·33	300	30	11	19	1A
BSX12A	n-p-n	TO–39	25	15	1A	1A	200	3W‡	30	120	300	450	0·33	300	30	11	19	1A
BSX44	n-p-n	TO–18	15	6	200	—	200	300	30	150	20	600	0·45	50	5·0	20	15	20
BSX76	n-p-n	TO–18	20	20	400	200	200	350	35	—	10	50	0·35	50	2·5	40	80	100

*typical **V_{CER} ($R_{BE} \leqslant 10\Omega$) †$T_{mb} \leqslant 25°C$ ‡$T_{case} \leqslant 95°C$

SILICON TRANSISTORS (cont.)

Type No.	Polarity	Outline	Maximum Ratings					P_{tot} at 25°C	h_{FE}		at	f_T	$V_{CE(sat)}$	at		t_{on}	t_{off}	at
			V_{CBO}	V_{CEO}	I_{CM}	$I_{C(AV)}$	T_j		min.	max.	I_C	min.	max.	I_C	I_B			
			(V)	(V)	(mA)	(mA)	(°C)	(mW)			(mA)	(MHz)	(V)	(mA)	(mA)	(ns)	(ns)	(mA)
BSX77	n-p-n	TO–18	40	20	400	200	200	350	40	120	10	100	0·35	50	2·5	40	80	100
BSX78	n-p-n	TO–18	40	20	400	200	200	350	80	240	10	100	0·35	50	2·5	40	80	100
BSY26	n-p-n	TO–18	20	15	200	100	175	300	20	60	10	200	0·35	10	1	27	130	10
BSY27	n-p-n	TO–18	20	15	200	100	175	300	40	120	10	200	0·35	10	1	27	130	10
BSY38	n-p-n	TO–18	20	15	200	100	175	300	15	45	100	350*	0·6	100	10	14	45	100
BSY39	n-p-n	TO–18	20	15	200	100	175	300	20	70	100	350*	0·6	100	10	14	45	100
BSY40	p-n-p	TO–18	–25	–20	140	100	200	300	25	60	10	140	–0·2	10	1	25	100	50
BSY41	p-n-p	TO–18	–25	–20	140	100	200	300	50	200	10	140	–0·2	10	1	25	100	50
BSY95	n-p-n	TO–18	20	15	200	100	140	150	50	200	10	200	–0·35	10	0·2	—	—	—
BU105	n-p-n	TO–3	1500	1500	2·5A	2·5A	115	10W	—	—	—	7·5*	5·0	2·5A	1·5A	—	750	2A
OC200	p-n-p	SO–2	–30	–25	100	50	150	250	10	50	20	0·45	–0·55	20	3	—	—	—
OC201	p-n-p	SO–2	–25	–20	100	50	150	250	10	70	20	2·0	–0·55	20	3	—	—	—
OC202	p-n-p	SO–2	–15	–10	100	50	150	250	24	125	20	1·4	–0·55	20	3	—	—	—
OC203	p-n-p	SO–2	–60	–50	100	50	150	250	10	50	20	0·3	–0·55	20	3	—	—	—
OC204	p-n-p	SO–2	–32	–32	500	250	150	125	10	30	150	0·45	–0·56	125	17	—	—	—
OC205	p-n-p	SO–2	–60	–60	500	250	150	125	10	50	150	0·45	–0·56	125	17	—	—	—
OC206	p-n-p	SO–2	–32	–32	500	250	150	125	16	120	150	0·85	–0·55	125	17	—	—	—
OC207	p-n-p	SO–2	–50	–50	500	250	150	310	12	70	150	2·0	–0·56	150	17	—	—	—

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BC157/8/9	1B		BDY20/2-BDY20	1B	
BC186/7	D*	BCY70	BDY38/2-BDY38	1B	
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*Not recommended for the design of new equipment.
Full data for these types are available on request.

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*Not recommended for the design of new equipment.
Full data for these types are available on request.

Type Number	Part/ Section	Suggested alternative	Type Number	Part/ Section	Suggested alternative
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TRANSISTORS

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